BUK9Y38-100E

N-channel 100 V, 38 mΩ logic level MOSFET in LFPAK56

9 May 2013

Product data sheet

1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V_{GS(th)} rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	100	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	30	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	94.9	W
Static chara	cteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	31.3	38	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 5 A; V _{DS} = 80 V; Fig. 13; Fig. 14		-	8.3	-	nC



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D I
2	S	source		
3	S	source	[q]j	G 4
4	G	gate	وققق	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK9Y38-100E	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669		

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y38-100E	93810E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	100	V
V _{GS}	gate-source voltage	T _j ≤ 175 °C; DC		-10	10	V
		T _j ≤ 175 °C; Pulsed	[1][2]	-15	15	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; <u>Fig. 1</u>		-	30	Α
		T _{mb} = 100 °C; V _{GS} = 5 V; <u>Fig. 1</u>		-	21.3	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 4		-	120	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	94.9	W

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Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drai	n diode		'			
I _S	source current	T _{mb} = 25 °C		-	30	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$		-	120	Α
Avalanche r	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 30 A; $V_{sup} \le$ 100 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3	[3][4]	-	45.1	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_i and or V_{GS}
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

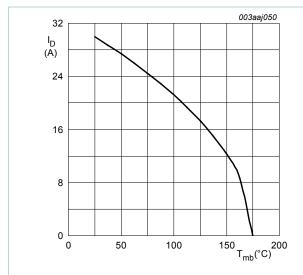


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 10V$$

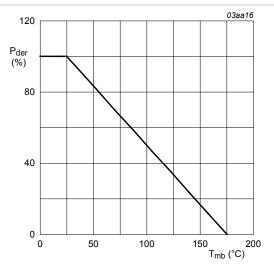


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

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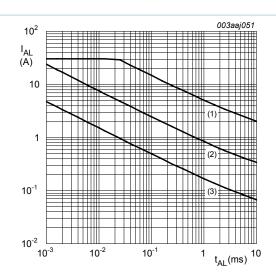
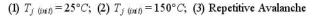


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time



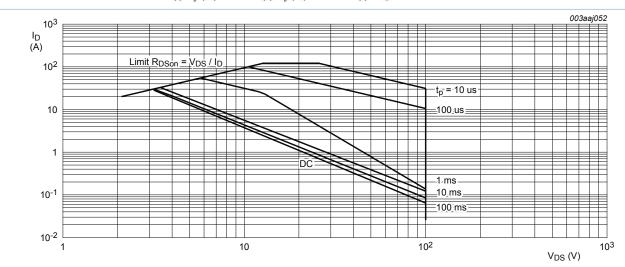


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

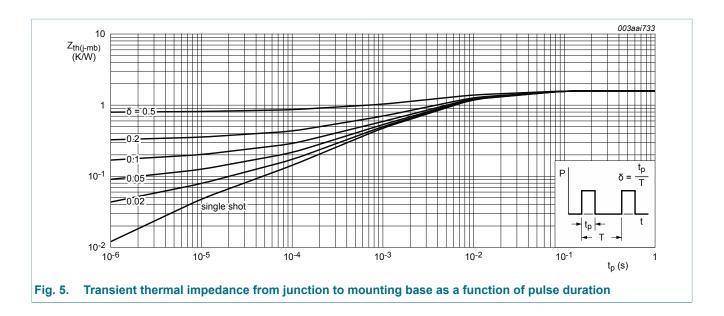
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	1.58	K/W

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10. Characteristics

Table 7. **Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					_
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	100	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^{\circ}C$	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	2.45	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; Fig. 9	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μΑ
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state	V _{GS} = 5 V; I _D = 5 A; T _j = 25 °C; <u>Fig. 11</u>	-	31.3	38	mΩ
	resistance	V _{GS} = 10 V; I _D = 5 A; T _j = 25 °C; <u>Fig. 11</u>	-	30.2	37.5	mΩ
		V _{GS} = 5 V; I _D = 5 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	105	mΩ
Dynamic ch	naracteristics		'			_
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 80 V; V _{GS} = 5 V;	-	21.6	-	nC
Q_{GS}	gate-source charge	Fig. 13; Fig. 14	-	3.8	-	nC
Q_{GD}	gate-drain charge		-	8.3	-	nC
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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; <u>Fig. 15</u>	-	1905	2541	pF
C _{oss}	output capacitance		-	137	165	pF
C _{rss}	reverse transfer capacitance		-	90	123	pF
t _{d(on)}	turn-on delay time	V_{DS} = 80 V; R_{L} = 10 Ω ; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω	-	10	-	ns
t _r	rise time		-	18	-	ns
t _{d(off)}	turn-off delay time		-	31	-	ns
t _f	fall time		-	18	-	ns
Source-dra	ain diode	1				
V_{SD}	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}; Fig. 16$	-	0.78	1.2	V
t _{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/ μ s; V_{GS} = 0 V; V_{DS} = 25 V	-	31	-	ns
Q _r	recovered charge		-	44	-	nC

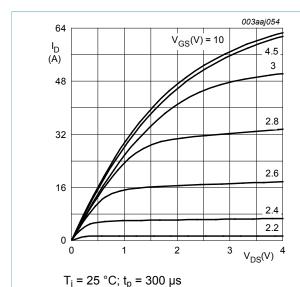


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

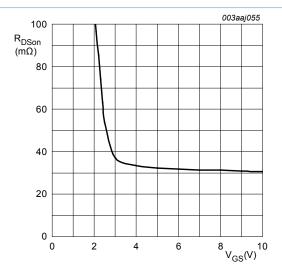


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 5A$$

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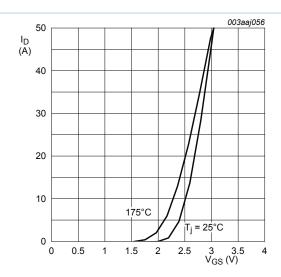


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



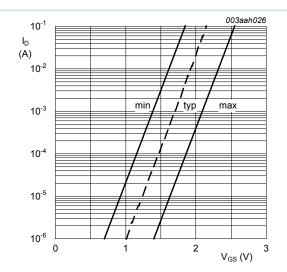


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25$$
°C; $V_{DS} = 5V$

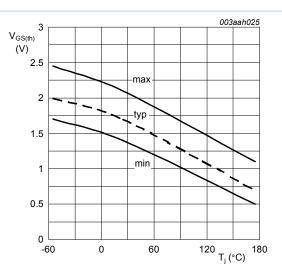
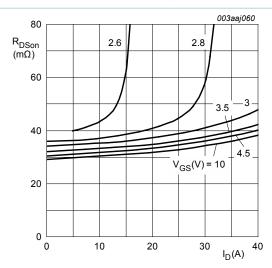


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$



 $T_j = 25 \, ^{\circ}\text{C}; t_p = 300 \, \mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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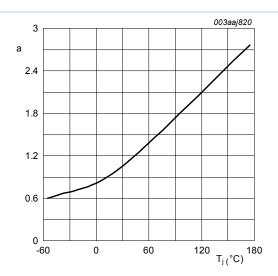


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon (25^{\circ}\text{C})}}$$

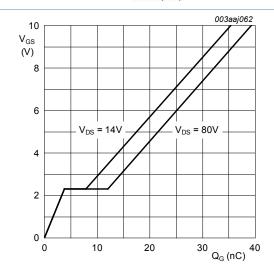


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25$$
°C; $I_D = 5A$

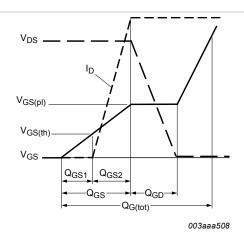


Fig. 13. Gate charge waveform definitions

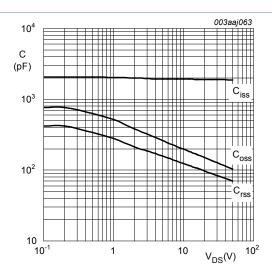


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V; f = \mathbf{1}MHz$$

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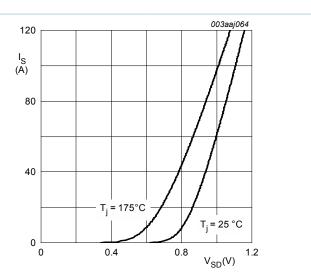


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

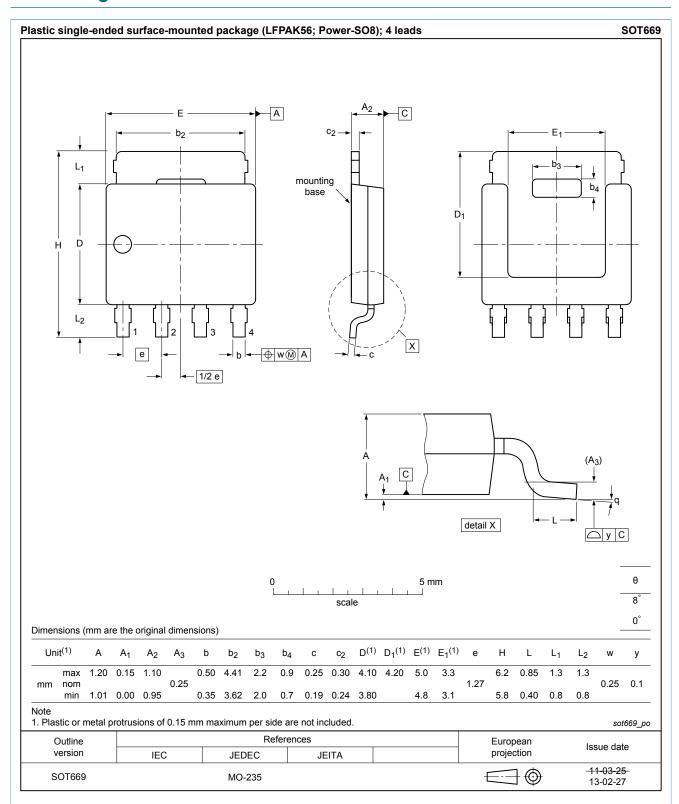


Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

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