74LVC8T595

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Rev. 2 — 29 August 2023 Product data sheet

1. General description

The 74LVC8T595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. Data is shifted on the positive-going transitions of the SHCP input. The data in the shift register is transferred to the storage register on a positive-going transition of the STCP input. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

$V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.1 V and 5.5 V making the device suitable for translating between any of the voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins $\overline{MR}$, SHCP, STCP, $\overline{OE}$, DS and Q7S are referenced to $V_{CC(A)}$ and pins Qn are referenced to $V_{CC(B)}$.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when $V_{CC(A)}$ is at GND level, the Qn outputs are in the high-impedance OFF-state.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.1 V to 5.5 V
  - $V_{CC(B)}$: 1.1 V to 5.5 V
- High noise immunity
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- ±24 mA output drive ($V_{CC(A)}$ = $V_{CC(B)}$ = 3.0 V)
- Inputs accept voltages up to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
  - JESD8-12A (1.1 V to 1.3 V)
  - JESD8-11A (1.4 V to 1.6 V)
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (3.0 V to 3.6 V)
  - JESD12-6 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC8T595PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC8T595BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

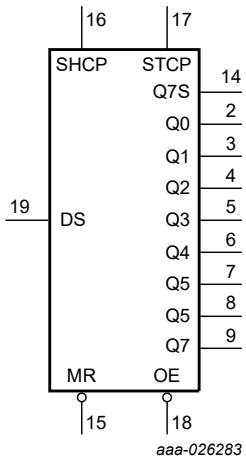


Fig. 1. Logic symbol

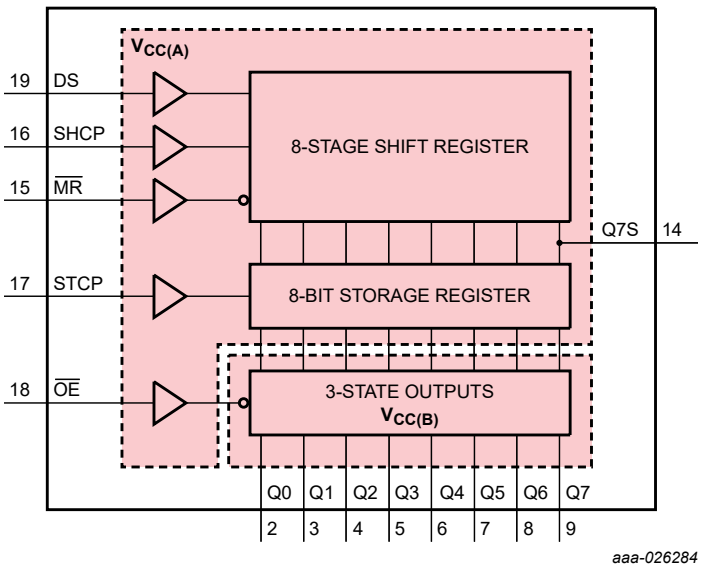


Fig. 2. Functional diagram

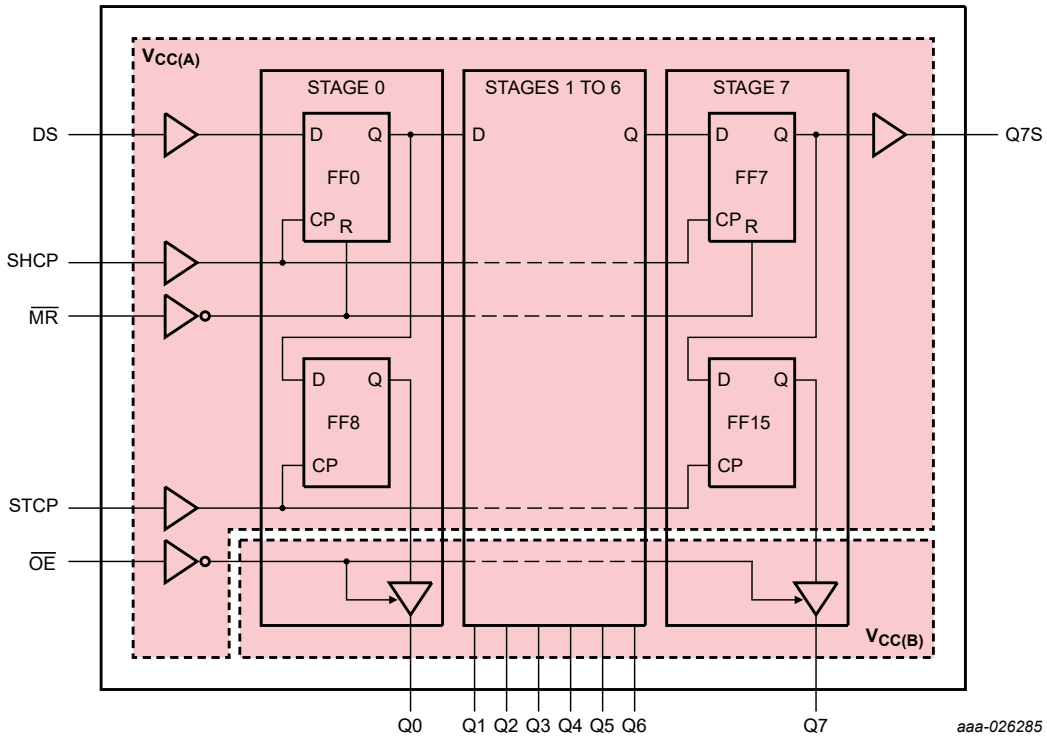


Fig. 3. Logic diagram

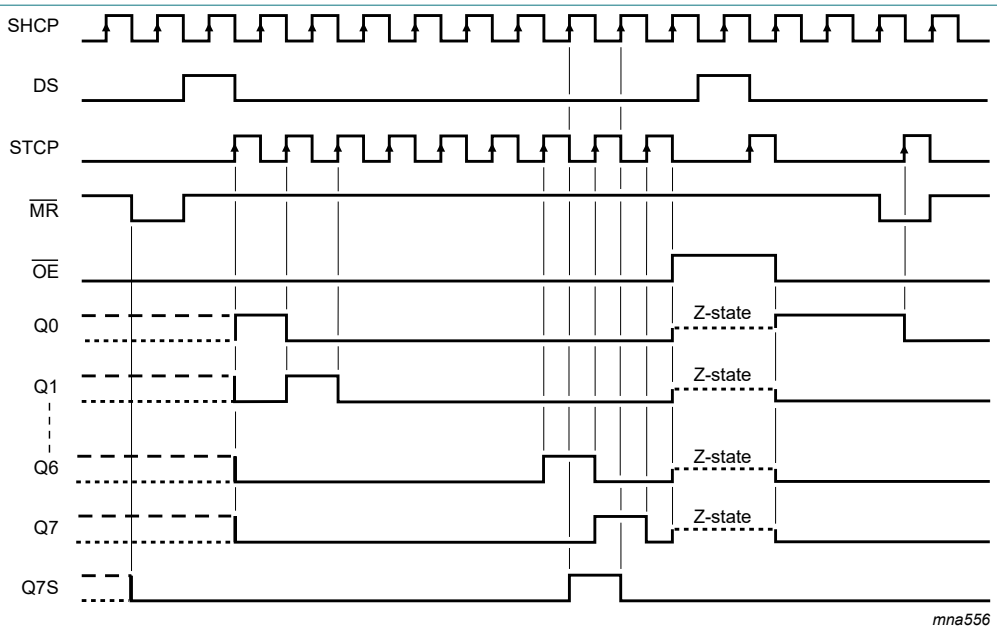
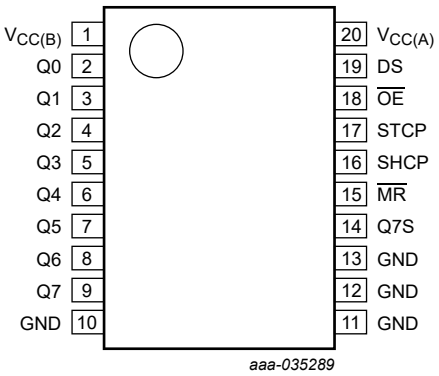


Fig. 4. Timing diagram

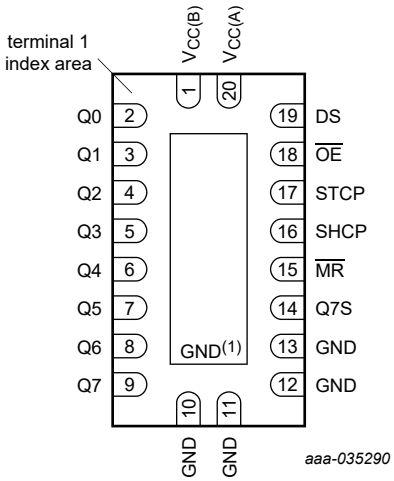
5. Pinning information

5.1. Pinning

PW package
SOT360-1 (TSSOP20)



BQ package
SOT764-1 (DHVQFN20)



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(B)}$	1	supply voltage B (Qn outputs)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 3, 4, 5, 6, 7, 8, 9	data output
GND	10, 11, 12, 13	ground (0 V)
Q7S	14	serial data output
$\overline{MR}$	15	master reset input (active LOW)
SHCP	16	shift register clock input
STCP	17	storage register clock input
$\overline{OE}$	18	output enable input (active LOW)
DS	19	serial data input
$V_{CC(A)}$	20	supply voltage A ($\overline{MR}$, SHCP, STCP, $\overline{OE}$, DS inputs and Q7S output)

6. Functional description

Table 3. Function table

H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition; X = don't care; NC = no change; Z = high-impedance OFF-state.

Supply voltage	Input					Output		Function
$V_{CC(A)}$, $V_{CC(B)}$	SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
1.2 V to 5.5 V	X	X	L	L	X	L	NC	a LOW-state on $\overline{MR}$ only affects the shift register
1.2 V to 5.5 V	X	↑	L	L	X	L	L	empty shift register loaded into storage register
1.2 V to 5.5 V	X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
1.2 V to 5.5 V	↑	X	L	H	H	Q6S	NC	logic HIGH-state shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
1.2 V to 5.5 V	X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
1.2 V to 5.5 V	↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages
GND[1]	X	X	X	X	X	X	Z	suspend mode

[1] When $V_{CC(A)}$ is at GND level, the device goes into suspend mode.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	V_O < 0 V	-50	-	mA
V_O	output voltage	Active mode [1] [2] [3]	-0.5	V_{CCO} + 0.5	V
		Suspend or 3-state mode [1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CCO} [2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output.
[3] V_{CCO} + 0.5 V should not exceed 6.5 V
[4] For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			1.1	5.5	V
$V_{CC(B)}$	supply voltage B			1.1	5.5	V
V_I	input voltage			0	5.5	V
V_O	output voltage	Active mode	[1]	0	V_{CCO}	V
		Suspend or 3-state mode		0	5.5	V
T_{amb}	ambient temperature			-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)}$ = 1.1 V to 1.3 V		-	20	ns/V
		$V_{CC(A)}$ = 1.4 V to 1.95 V		-	20	ns/V
		$V_{CC(A)}$ = 2.3 V to 2.7 V		-	20	ns/V
		$V_{CC(A)}$ = 3 V to 3.6 V		-	10	ns/V
		$V_{CC(A)}$ = 4.5 V to 5.5 V		-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output.

9. Static characteristics

Table 6. Typical static characteristics at T_{amb} = 25 °C

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -3 mA; V_{CCO} = 1.2 V	[1]	-	1.09	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 3 mA; V_{CCO} = 1.2 V	[1]	-	0.07	-	V
I_I	input leakage current	$\overline{MR}$, SHCP, STCP, $\overline{OE}$ and DS inputs; V_I = 0 V to 5.5 V; $V_{CC(A)}$ = 1.1 V to 5.5 V		-	-	±1	µA
I_{OZ}	OFF-state output current	Qn outputs; V_O = 0 V or $V_{CC(B)}$					
		$V_{CC(B)}$ = 1.1 V to 5.5 V		-	-	±1	µA
		suspend mode; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	-	±1	µA
I_{OFF}	power-off leakage current	inputs, Q7S output; V_I or V_O = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 1.1 V to 5.5 V	[1]	-	-	±1	µA
		Qn outputs; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 1.1 V to 5.5 V		-	-	±1	µA
C_I	input capacitance	$\overline{MR}$, SHCP, STCP, $\overline{OE}$ and DS inputs; V_I = 0 V or 3.3 V; $V_{CC(A)}$ = $V_{CC(B)}$ = 3.3 V		-	3	-	pF

[1] V_{CCO} is the supply voltage associated with the output.

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC(A)}$ = 1.1 V to 1.3 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 1.4 V to 1.6 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 1.65 V to 1.95 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	1.7	-	1.7	-	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	2.0	-	2.0	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	$0.7V_{CC(A)}$	-	$0.7V_{CC(A)}$	-	V
V_{IL}	LOW-level input voltage	$V_{CC(A)}$ = 1.1 V to 1.3 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)}$ = 1.4 V to 1.6 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)}$ = 1.65 V to 1.95 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	-	$0.3V_{CC(A)}$	-	$0.3V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ [1]					
		I_O = -100 µA; V_{CCO} = 1.1 V to 4.5 V	V_{CCO} - 0.1	-	V_{CCO} - 0.1	-	V
		I_O = -2 mA; V_{CCO} = 1.1 V	0.825	-	0.825	-	V
		I_O = -6 mA; V_{CCO} = 1.4 V	1.0	-	1.0	-	V
		I_O = -8 mA; V_{CCO} = 1.65 V	1.2	-	1.2	-	V
		I_O = -12 mA; V_{CCO} = 2.3 V	1.9	-	1.9	-	V
		I_O = -24 mA; V_{CCO} = 3.0 V	2.4	-	2.4	-	V
		I_O = -24 mA; V_{CCO} = 4.5 V	3.85	-	3.85	-	V
		I_O = -32 mA; V_{CCO} = 4.5 V	3.8	-	3.8	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IL}$ [1]					
		I_O = 100 µA; V_{CCO} = 1.1 V to 4.5 V	-	0.1	-	0.1	V
		I_O = 2 mA; V_{CCO} = 1.1 V	-	0.275	-	0.275	V
		I_O = 6 mA; V_{CCO} = 1.4 V	-	0.3	-	0.3	V
		I_O = 8 mA; V_{CCO} = 1.65 V	-	0.45	-	0.45	V
		I_O = 12 mA; V_{CCO} = 2.3 V	-	0.3	-	0.3	V
		I_O = 24 mA; V_{CCO} = 3.0 V	-	0.55	-	0.55	V
		I_O = 24 mA; V_{CCO} = 4.5 V	-	0.50	-	0.50	V
		I_O = 32 mA; V_{CCO} = 4.5 V	-	0.55	-	0.55	V
I_I	input leakage current	V_I = 0 V to 5.5 V; $V_{CC(A)}$ = 1.1 V to 5.5 V	-	±2	-	±10	µA
I_{OZ}	OFF-state output current	Qn outputs; V_O = 0 V or $V_{CC(B)}$					
		$V_{CC(B)}$ = 1.1 V to 5.5 V	-	±2	-	±10	µA
		suspend mode; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-	±2	-	±10	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{OFF}	power-off leakage current	inputs, Q7S output; V_I or V_O = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 1.1 V to 5.5 V	-	±2	-	±10	µA
		Qn outputs; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 1.1 V to 5.5 V	-	±2	-	±10	µA
I_{CC}	supply current	$V_{CC(A)}$ domain; V_I = 0 V or $V_{CC(A)}$; I_O = 0 A					
		$V_{CC(A)}$, $V_{CC(B)}$ = 1.1 V to 5.5 V	-	2	-	5	µA
		$V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V	-	2	-	5	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-1	-	-2	-	µA
		$V_{CC(B)}$ domain; V_I = 0 V or $V_{CC(A)}$; I_O = 0 A					
		$V_{CC(A)}$, $V_{CC(B)}$ = 1.1 V to 5.5 V	-	9	-	24	µA
		$V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 0 V	-	9	-	24	µA
		$V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 5.5 V	-1	-	-2	-	µA
ΔI_{CC}	additional supply current	per input; $V_{CC(A)}$, $V_{CC(B)}$ = 3.0 V to 5.5 V					
		$\overline{MR}$, SHCP, STCP, $\overline{OE}$ inputs; one input at $V_{CC(A)}$ - 0.6 V; DS input at $V_{CC(A)}$ or GND; Qn = open	-	50	-	75	µA
		DS input at $V_{CC(A)}$ - 0.6 V; Qn = open	-	50	-	75	µA

[1] V_{CCO} is the supply voltage associated with the output.

10. Dynamic characteristics

Table 8. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
C_{PD}	power dissipation capacitance	inputs [1] [2]	31	31	32	33	36	43	pF
		outputs [1] [2]	105	104	103	101	99	98	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; R_L = ∞ Ω.

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11; for waveforms see Fig. 5 up to Fig. 10.

Symbol	Parameter	Conditions	$V_{CC(A)}$									Unit
			1.2 V ± 0.1 V			1.5 V ± 0.1 V			1.8 V ± 0.15 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T_{amb} = +25 °C; $V_{CC(B)}$ = 1.1 V to 5.5V												
t_{pd}	propagation delay	SHCP to Q7S [1]	5.8	21.3	38.9	4.5	14.2	20.9	3.7	10.9	16.7	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S	5.9	22.7	42.1	4.5	14.8	18.9	3.7	11.2	14.7	ns
t_W	pulse width	SHCP, STCP HIGH or LOW	6.9	1.9	-	3.5	1.4	-	2.6	1.1	-	ns
		$\overline{MR}$ LOW	12.4	3.5	-	5.6	2.1	-	3.9	1.5	-	ns
t_{su}	set-up time	DS to SHCP	3.0	1.1	-	2.6	0.5	-	2.3	0.3	-	ns
		$\overline{MR}$ to STCP	15.5	7.2	-	7.9	4.0	-	5.5	2.8	-	ns
		SHCP to STCP	13.5	5.4	-	6.5	3.0	-	4.9	2.1	-	ns
t_h	hold time	DS to SHCP	3.0	±0.4	-	2.0	±0.2	-	1.5	±0.1	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP	2.0	-0.4	-	1.5	-0.2	-	1.3	-0.2	-	ns
f_{max}	maximum frequency	SHCP	45	73	-	75	99	-	90	120	-	MHz

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

Table 10. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11; for waveforms see Fig. 5 up to Fig. 10.

Symbol	Parameter	Conditions	$V_{CC(A)}$									Unit
			2.5 V ± 0.2 V			3.3 V ± 0.3 V			5.0 V ± 0.5 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T_{amb} = +25 °C; $V_{CC(B)}$ = 1.1 V to 5.5V												
t_{pd}	propagation delay	SHCP to Q7S [1]	2.7	7.3	11.5	2.3	5.6	9.1	1.9	4.1	6.6	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S	2.9	7.4	10.0	2.4	5.7	7.9	2.1	4.4	6.1	ns
t_W	pulse width	SHCP, STCP HIGH or LOW	1.6	0.7	-	1.4	0.6	-	1.0	0.5	-	ns
		$\overline{MR}$ LOW	2.5	1.0	-	1.6	0.8	-	1.4	0.6	-	ns
t_{su}	set-up time	DS to SHCP	1.9	0.2	-	1.5	0.1	-	1.1	0.1	-	ns
		$\overline{MR}$ to STCP	3.2	1.7	-	2.4	1.3	-	2.2	1.1	-	ns
		SHCP to STCP	2.8	1.2	-	1.9	0.9	-	1.4	0.6	-	ns
t_h	hold time	DS to SHCP	1.5	±0.1	-	1.0	±0.1	-	1.0	±0.1	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP	1.0	-0.1	-	1.0	-0.1	-	1.0	-0.1	-	ns
f_{max}	maximum frequency	SHCP	135	160	-	175	194	-	195	250	-	MHz

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

Table 11. Dynamic characteristics for temperature +25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11; for waveforms see Fig. 5 up to Fig. 10.
t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Symbol	Parameter	Conditions	$V_{CC(B)}$									Unit
			1.2 V ± 0.1 V			1.5 V ± 0.1 V			1.8 V ± 0.15 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{CC(A)}$ = 1.2 V ± 0.1 V												
t_{pd}	propagation delay	STCP to Qn	6.2	23.7	46.4	5.3	19.1	35.4	4.8	16.9	31.6	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	3.6	12.7	25.1	3.0	9.7	15.6	3.1	9.0	14.4	ns
t_{en}	enable time	$\overline{OE}$ to Qn	5.8	20.9	40.0	4.6	15.1	26.2	3.9	12.6	21.7	ns
f_{max}	maximum frequency	STCP	35	69	-	45	88	-	45	110	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	3.0	-	-	2.3	-	-	1.9	ns
$V_{CC(A)}$ = 1.5 V ± 0.1 V												
t_{pd}	propagation delay	STCP to Qn	5.7	20.2	32.1	4.9	15.5	23.3	4.3	13.3	20.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	3.4	11.4	20.1	2.8	8.3	13.2	2.8	7.6	11.7	ns
t_{en}	enable time	$\overline{OE}$ to Qn	5.5	19.9	38.7	4.2	13.9	24.1	3.6	11.3	19.3	ns
f_{max}	maximum frequency	STCP	45	73	-	70	95	-	90	120	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	2.7	-	-	2.0	-	-	1.7	ns
$V_{CC(A)}$ = 1.8 V ± 0.15 V												
t_{pd}	propagation delay	STCP to Qn	5.4	18.7	30.3	4.5	14.0	21.4	4	11.8	18.3	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	3.2	10.8	19.4	2.6	7.8	12.6	2.6	7.0	11.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn	5.4	19.4	38.1	4.1	13.4	23.7	3.5	10.7	18.7	ns
f_{max}	maximum frequency	STCP	45	75	-	70	98	-	90	125	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	2.7	-	-	2.0	-	-	1.6	ns
$V_{CC(A)}$ = 2.5 V ± 0.2 V												
t_{pd}	propagation delay	STCP to Qn	5.1	17.3	28.3	4.2	12.6	19.5	3.6	10.4	16.3	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	3.0	10.3	18.8	2.4	7.2	11.9	2.4	6.4	10.3	ns
t_{en}	enable time	$\overline{OE}$ to Qn	5.3	18.9	37.7	4.1	13.0	23.3	3.4	10.2	18.1	ns
f_{max}	maximum frequency	STCP	45	76	-	70	100	-	90	128	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	2.6	-	-	2.0	-	-	1.6	ns
$V_{CC(A)}$ = 3.3 V ± 0.3 V												
t_{pd}	propagation delay	STCP to Qn	4.9	16.7	27.6	4.0	12.0	18.7	3.4	9.8	15.4	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	3.0	10.0	18.4	2.3	6.9	11.4	2.3	6.1	10.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn	5.3	18.8	37.6	4.1	12.9	23.0	3.4	10.1	18.0	ns
f_{max}	maximum frequency	STCP	45	76	-	70	101	-	90	130	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	2.6	-	-	2.0	-	-	1.6	ns
$V_{CC(A)}$ = 5.0 V ± 0.5 V												
t_{pd}	propagation delay	STCP to Qn	4.8	16.1	27.5	3.9	11.4	18.0	3.3	9.2	14.8	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	2.8	9.6	19.4	2.2	6.6	11.3	2.3	5.9	9.6	ns
t_{en}	enable time	$\overline{OE}$ to Qn	5.4	18.7	38.3	4.1	12.8	23.1	3.4	10.1	18.3	ns
f_{max}	maximum frequency	STCP	45	77	-	70	102	-	90	132	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	2.7	-	-	2.0	-	-	1.6	ns

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Table 12. Dynamic characteristics for temperature +25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11; for waveforms see Fig. 5 up to Fig. 10.

t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Symbol	Parameter	Conditions	$V_{CC(B)}$									Unit
			2.5 V ± 0.2 V			3.3 V ± 0.3 V			5.0 V ± 0.5 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{CC(A)}$ = 1.2 V ± 0.1 V												
t_{pd}	propagation delay	STCP to Qn	4.2	14.5	27.9	3.8	13.4	26.3	3.5	12.4	24.9	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	2.6	7.4	12.0	2.9	7.7	12.4	2.4	6.6	11.3	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.3	10.1	16.8	2.9	9.2	15.8	2.7	8.9	15.9	ns
f_{max}	maximum frequency	STCP	45	131	-	45	139	-	45	144	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	1.4	-	-	1.2	-	-	1.0	ns
$V_{CC(A)}$ = 1.5 V ± 0.1 V												
t_{pd}	propagation delay	STCP to Qn	3.7	10.9	16.2	3.3	9.7	14.5	3.0	8.7	13.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	2.2	6.0	9.2	2.6	6.2	9.4	2.1	5.0	8.1	ns
t_{en}	enable time	$\overline{OE}$ to Qn	2.9	8.6	14.1	2.6	7.5	12.1	2.4	6.7	10.6	ns
f_{max}	maximum frequency	STCP	130	144	-	130	187	-	130	224	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	1.2	-	-	1.0	-	-	0.7	ns
$V_{CC(A)}$ = 1.8 V ± 0.15 V												
t_{pd}	propagation delay	STCP to Qn	3.4	9.4	14.4	3.0	8.2	12.6	2.7	7.2	10.9	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	2.0	5.3	8.3	2.4	5.5	8.5	1.9	4.3	7.2	ns
t_{en}	enable time	$\overline{OE}$ to Qn	2.7	8.0	13.3	2.4	6.7	11.1	2.2	5.8	9.4	ns
f_{max}	maximum frequency	STCP	130	151	-	165	197	-	205	237	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	1.2	-	-	0.9	-	-	0.7	ns
$V_{CC(A)}$ = 2.5 V ± 0.2 V												
t_{pd}	propagation delay	STCP to Qn	3.0	7.9	12.4	2.6	6.7	10.5	2.3	5.7	8.8	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.9	4.6	7.5	2.2	4.8	7.5	1.7	3.5	6.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn	2.7	7.4	12.6	2.3	6.0	10.2	2.0	4.9	8.2	ns
f_{max}	maximum frequency	STCP	130	156	-	165	210	-	215	252	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	1.2	-	-	0.9	-	-	0.7	ns
$V_{CC(A)}$ = 3.3 V ± 0.3 V												
t_{pd}	propagation delay	STCP to Qn	2.8	7.3	11.5	2.4	6.1	9.6	2.1	5.0	7.9	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.8	4.4	7.1	2.1	4.5	7.1	1.6	3.2	5.5	ns
t_{en}	enable time	$\overline{OE}$ to Qn	2.6	7.2	12.3	2.3	5.8	10.0	2.0	4.6	7.8	ns
f_{max}	maximum frequency	STCP	130	159	-	165	213	-	215	255	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	1.2	-	-	0.9	-	-	0.7	ns
$V_{CC(A)}$ = 5.0 V ± 0.5 V												
t_{pd}	propagation delay	STCP to Qn	2.7	6.8	10.9	2.3	5.5	8.9	1.8	4.4	7.2	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.7	4.1	6.8	2.0	4.3	6.7	1.4	2.9	5.1	ns
t_{en}	enable time	$\overline{OE}$ to Qn	2.7	7.2	12.4	2.3	5.8	10.0	2.0	4.6	7.7	ns
f_{max}	maximum frequency	STCP	130	159	-	165	213	-	215	254	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	-	1.1	-	-	0.9	-	-	0.7	ns

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Table 13. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11; for waveforms see Fig. 5 up to Fig. 10.

Symbol	Parameter	Conditions	$V_{CC(A)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T_{amb} = -40 °C to +85 °C; $V_{CC(B)}$ = 1.1 V to 5.5V															
t_{pd}	propagation delay	SHCP to Q7S [1]	3.4	42.1	2.7	22.1	2.1	17.7	1.5	12.4	1.3	9.8	1.0	7.2	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S	3.6	43.6	2.7	20.2	2.2	16.0	1.7	11.0	1.4	8.7	1.3	6.6	ns
t_W	pulse width	SHCP, STCP; HIGH or LOW	7.8	-	4.8	-	3.3	-	2.0	-	1.7	-	1.3	-	ns
		$\overline{MR}$ LOW	12.8	-	6.2	-	4.4	-	2.8	-	2.3	-	1.4	-	ns
t_{su}	set-up time	DS to SHCP	4.5	-	3.0	-	2.6	-	2.3	-	1.9	-	1.5	-	ns
		$\overline{MR}$ to STCP	16.5	-	9.1	-	6.1	-	3.6	-	2.9	-	2.3	-	ns
		SHCP to STCP	13.5	-	7.7	-	5.4	-	3.2	-	2.3	-	1.8	-	ns
t_h	hold time	DS to SHCP	3.0	-	2.0	-	1.5	-	1.5	-	1.0	-	1.0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP	2.2	-	1.7	-	1.5	-	1.2	-	1.2	-	1.2	-	ns
f_{max}	maximum frequency	SHCP	40	-	70	-	90	-	130	-	160	-	175	-	MHz
T_{amb} = -40 °C to +125 °C; $V_{CC(B)}$ = 1.1 V to 5.5V															
t_{pd}	propagation delay	SHCP to Q7S [1]	3.4	42.1	2.7	22.7	2.1	18.3	1.5	12.9	1.3	10.3	1.0	7.6	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S	3.6	44.3	2.7	21.0	2.2	16.7	1.7	11.5	1.4	9.1	1.3	7.0	ns
t_W	pulse width	SHCP, STCP; HIGH or LOW	8.4	-	5.3	-	3.8	-	2.5	-	1.9	-	1.4	-	ns
		$\overline{MR}$ LOW	13.3	-	6.9	-	5.2	-	3.1	-	2.4	-	1.6	-	ns
t_{su}	set-up time	DS to SHCP	4.5	-	3.0	-	2.6	-	2.3	-	1.9	-	1.5	-	ns
		$\overline{MR}$ to STCP	16.5	-	9.5	-	6.8	-	4.2	-	3.1	-	2.4	-	ns
		SHCP to STCP	14.2	-	8.0	-	6.2	-	3.6	-	2.3	-	1.8	-	ns
t_h	hold time	DS to SHCP	3.5	-	2.5	-	2.0	-	2.0	-	1.5	-	1.2	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP	2.4	-	1.9	-	1.7	-	1.4	-	1.4	-	1.4	-	ns
f_{max}	maximum frequency	SHCP	40	-	70	-	85	-	120	-	150	-	170	-	MHz

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

Table 14. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11; for waveforms see Fig. 5 up to Fig. 10.

t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Symbol	Parameter	Conditions	$V_{CC(B)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.2 V ± 0.1 V															
t_{pd}	propagation delay	STCP to Qn	3.8	48.3	3.2	36.7	2.8	33.0	2.4	29.2	2.2	27.7	2.0	26.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	2.1	26.6	1.8	17.2	1.8	15.8	1.5	13.1	1.8	13.4	1.4	12.3	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.5	42.1	2.7	27.0	2.2	22.6	1.9	18.0	1.7	17.0	1.6	17.2	ns
f_{max}	maximum frequency	STCP	30	-	40	-	40	-	40	-	40	-	40	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.5	-	2.5	-	2.0	-	1.5	-	1.2	-	1.0	ns
$V_{CC(A)}$ = 1.5 V ± 0.1 V															
t_{pd}	propagation delay	STCP to Qn	3.5	34.2	2.9	25.6	2.5	22.4	2.1	18.5	1.9	16.8	1.7	15.1	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	2.0	21.6	1.7	14.8	1.7	13.1	1.3	10.3	1.6	10.4	1.3	9.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.3	38.9	2.6	25.0	2.1	20.3	1.7	15.1	1.5	13.2	1.4	11.7	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	105	-	105	-	105	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.1	-	2.2	-	1.8	-	1.3	-	1.0	-	0.8	ns
$V_{CC(A)}$ = 1.8 V ± 0.15 V															
t_{pd}	propagation delay	STCP to Qn	3.3	31.8	2.7	23.4	2.3	20.4	1.9	16.4	1.7	14.5	1.5	12.8	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.9	20.9	1.5	14.2	1.6	12.4	1.2	9.4	1.4	9.4	1.1	8.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.3	38.6	2.4	24.5	2.0	19.7	1.6	14.4	1.4	12.1	1.3	10.5	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	120	-	145	-	155	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.1	-	2.2	-	1.8	-	1.2	-	1.0	-	0.8	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 2.5 V ± 0.2 V															
t_{pd}	propagation delay	STCP to Qn	3.1	29.6	2.5	21.2	2.1	18.1	1.7	14.0	1.5	12.1	1.3	10.2	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.8	20.2	1.4	13.2	1.4	11.6	1.1	8.5	1.3	8.3	1.0	6.6	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.2	37.7	2.4	24.0	2.0	19.1	1.5	13.5	1.3	11.1	1.2	9.0	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	120	-	145	-	180	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.1	-	2.2	-	1.8	-	1.2	-	1.0	-	0.7	ns
$V_{CC(A)}$ = 3.3 V ± 0.3 V															
t_{pd}	propagation delay	STCP to Qn	3.0	29.1	2.4	20.3	2.0	17.2	1.6	13.0	1.4	11.0	1.2	9.1	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.7	19.7	1.3	13.0	1.4	11.2	1.0	8.1	1.3	7.9	0.9	6.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.2	38.1	2.4	23.7	2.0	19.0	1.5	13.3	1.3	10.7	1.2	8.5	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	120	-	145	-	190	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.0	-	2.2	-	1.8	-	1.2	-	1.0	-	0.7	ns
$V_{CC(A)}$ = 5.0 V ± 0.5 V															
t_{pd}	propagation delay	STCP to Qn	2.9	29.1	2.3	19.6	1.9	16.3	1.5	12.2	1.3	10.2	1.1	8.2	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.6	20.6	1.3	12.6	1.3	10.9	0.9	7.7	1.2	7.5	0.8	5.6	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.3	38.9	2.5	23.8	2.0	19.1	1.6	13.3	1.4	10.6	1.2	8.3	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	120	-	145	-	190	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.0	-	2.2	-	1.7	-	1.2	-	0.9	-	0.7	ns

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Table 15. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11; for waveforms see Fig. 5 up to Fig. 10.

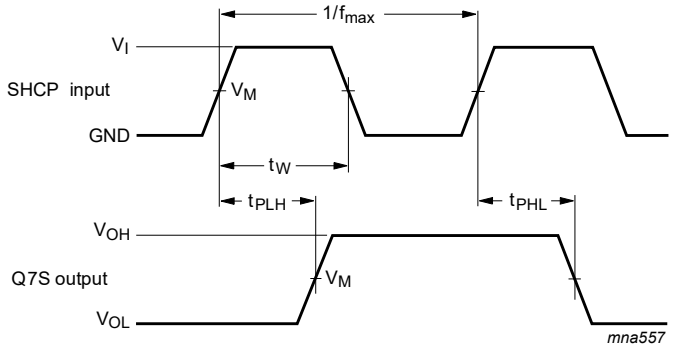
t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Symbol	Parameter	Conditions	$V_{CC(B)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V															
t_{pd}	propagation delay	STCP to Qn	3.8	48.3	3.2	37.4	2.8	34.0	2.4	30.4	2.2	28.6	2.0	27.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	2.1	27.6	1.8	18.0	1.8	16.5	1.5	13.7	1.8	14.1	1.4	12.8	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.5	42.1	2.7	27.6	2.2	23.2	1.9	18.6	1.7	17.8	1.6	18.0	ns
f_{max}	maximum frequency	STCP	30	-	40	-	40	-	40	-	40	-	40	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.6	-	2.6	-	2.1	-	1.5	-	1.3	-	1.0	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V															
t_{pd}	propagation delay	STCP to Qn	3.5	34.4	2.9	26.3	2.5	23.3	2.1	19.6	1.9	17.7	1.7	16.1	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	2.0	22.7	1.7	15.7	1.7	14.0	1.3	11.0	1.6	11.0	1.3	9.5	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.3	38.9	2.6	25.5	2.1	20.8	1.7	15.8	1.5	13.8	1.4	12.3	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	95	-	95	-	95	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.1	-	2.2	-	1.8	-	1.3	-	1.0	-	0.8	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V															
t_{pd}	propagation delay	STCP to Qn	3.3	32.1	2.7	24.1	2.3	21.1	1.9	17.3	1.7	15.3	1.5	13.6	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.9	21.9	1.5	14.9	1.6	13.2	1.2	10.1	1.4	10.0	1.1	8.4	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.3	38.6	2.4	24.8	2.0	20.3	1.6	14.9	1.4	12.7	1.3	11.0	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	105	-	140	-	140	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.1	-	2.2	-	1.8	-	1.2	-	1.0	-	0.8	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 2.3 V to 2.7 V															
t_{pd}	propagation delay	STCP to Qn	3.1	29.7	2.5	21.8	2.1	18.8	1.7	14.7	1.5	12.7	1.3	10.8	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.8	21.2	1.4	14.2	1.4	12.4	1.1	9.1	1.3	8.8	1.0	7.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.2	37.7	2.4	24.4	2.0	19.7	1.5	14.1	1.3	11.6	1.2	9.4	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	105	-	140	-	175	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.1	-	2.2	-	1.8	-	1.2	-	1.0	-	0.7	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V															
t_{pd}	propagation delay	STCP to Qn	3.0	29.1	2.4	20.8	2.0	17.7	1.6	13.5	1.4	11.6	1.2	9.6	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.7	20.9	1.3	13.8	1.4	12.1	1.0	8.7	1.3	8.3	0.9	6.4	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.2	38.1	2.4	24.3	2.0	19.5	1.5	13.7	1.3	11.2	1.2	8.9	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	105	-	140	-	175	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.0	-	2.2	-	1.8	-	1.2	-	1.0	-	0.7	ns
$V_{CC(A)}$ = 4.5 V to 5.5 V															
t_{pd}	propagation delay	STCP to Qn	2.9	29.1	2.3	20.0	1.9	16.7	1.5	12.7	1.3	10.6	1.1	9.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn	1.6	21.7	1.3	13.6	1.3	11.7	0.9	8.3	1.2	7.9	0.8	6.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn	3.3	38.9	2.5	24.3	2.0	19.5	1.6	13.8	1.4	11.0	1.2	8.6	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	105	-	140	-	175	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [1]	-	3.0	-	2.2	-	1.7	-	1.2	-	0.9	-	0.7	ns

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

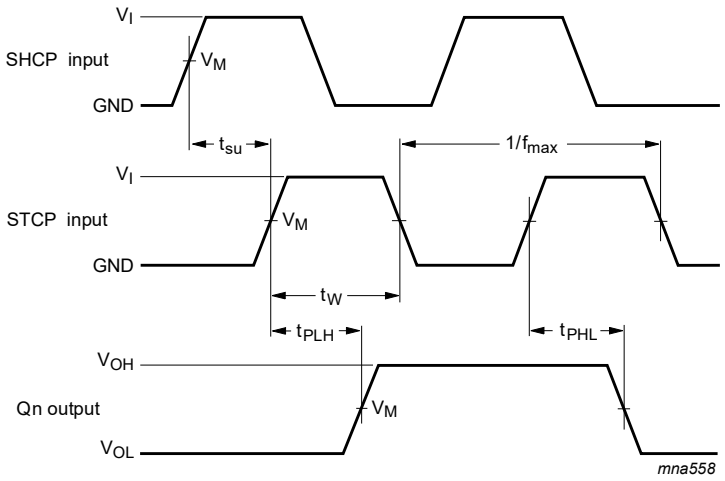
10.1. Waveforms and test circuit



Measurement points are given in Table 16.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

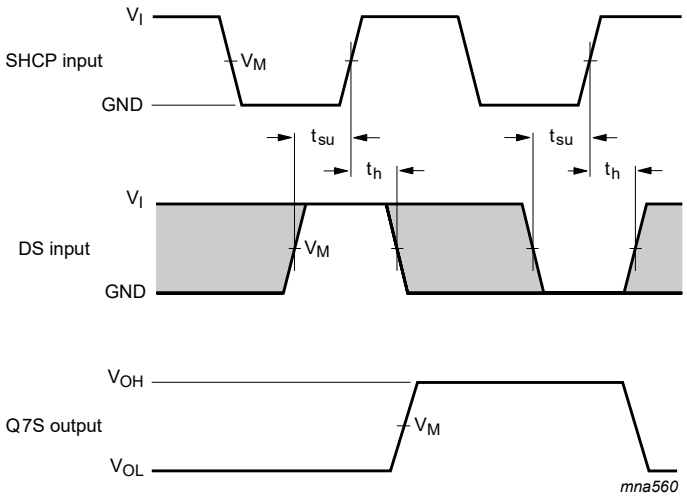
Fig. 5. The shift clock (SHCP) to serial data output (Q7S) propagation delays, the shift clock pulse width and maximum shift clock frequency



Measurement points are given in Table 16.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

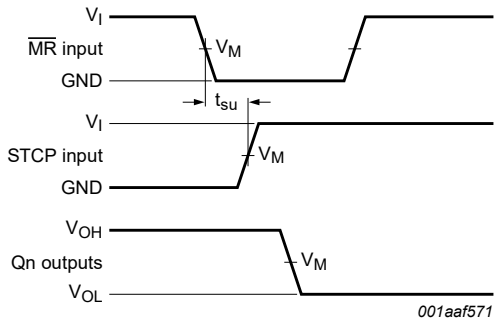
Fig. 6. The storage clock (STCP) to parallel data output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time



Measurement points are given in Table 16.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

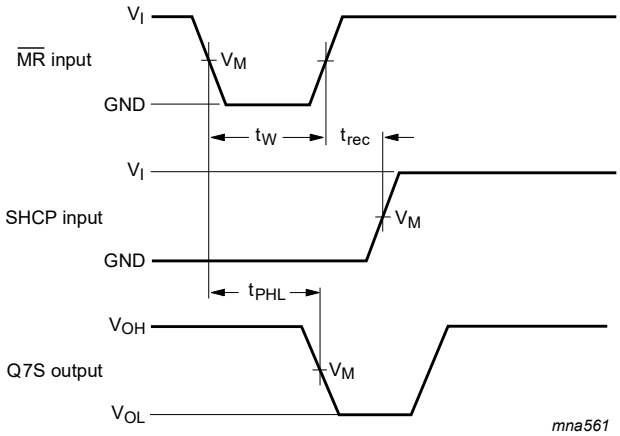
Fig. 7. The data set-up and hold times for the serial data input (DS)



Measurement points are given in Table 16.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

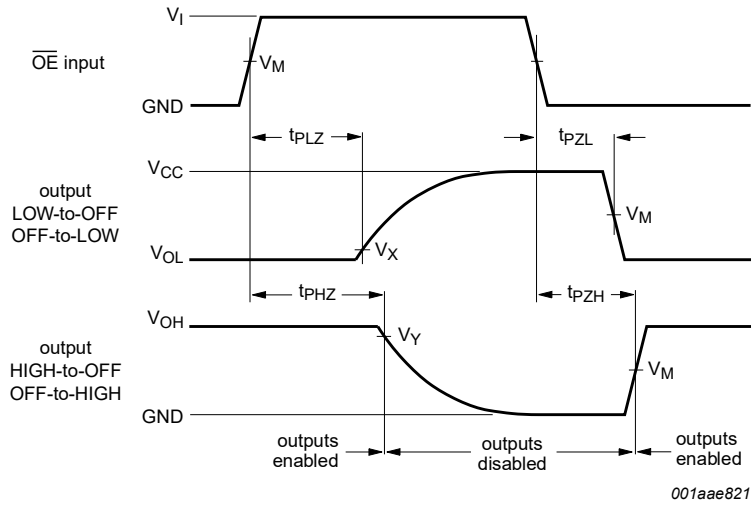
Fig. 8. The master reset ($\overline{MR}$) to storage clock (STCP) set-up time



Measurement points are given in Table 16.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. The master reset ($\overline{MR}$) pulse width, the master reset to serial data output (Q7S) propagation delays and the master reset to shift clock (SHCP) recovery time



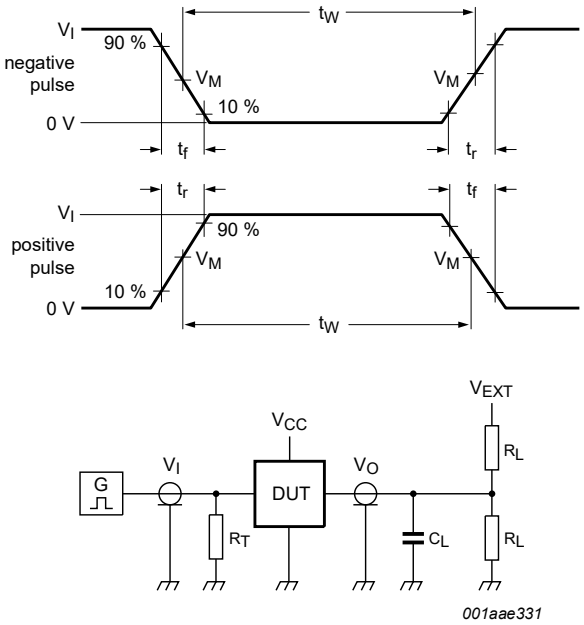
Measurement points are given in Table 16.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig. 10. 3-state enable and disable times

Table 16. Measurement points

Supply voltage	Input	Output			
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M (Qn)	V_M (Q7S)	V_X	V_Y
1.1 V to 1.6 V	$0.5V_{CC(A)}$	$0.5V_{CC(B)}$	$0.5V_{CC(A)}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.65 V to 2.7 V	$0.5V_{CC(A)}$	$0.5V_{CC(B)}$	$0.5V_{CC(A)}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 5.5 V	$0.5V_{CC(A)}$	$0.5V_{CC(B)}$	$0.5V_{CC(A)}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 17 .

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

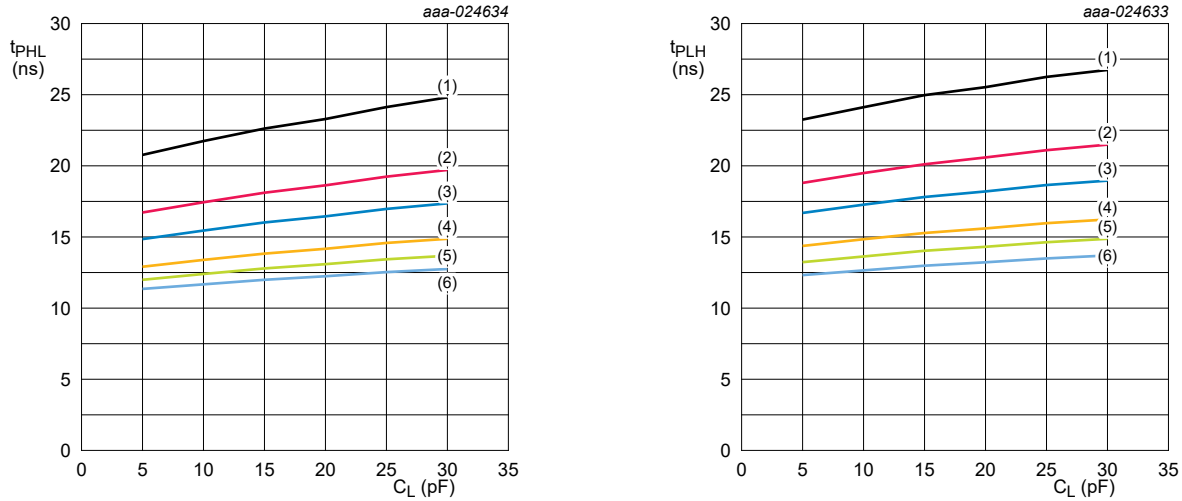
Fig. 11. Test circuit for measuring switching times

Table 17. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I	$\Delta t/\Delta V$ [1]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.1 V to 5.5 V	$V_{CC(A)}$	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CC(B)}$

[1] dV/dt ≥ 1.0 V/ns

10.2. Typical propagation delay characteristics

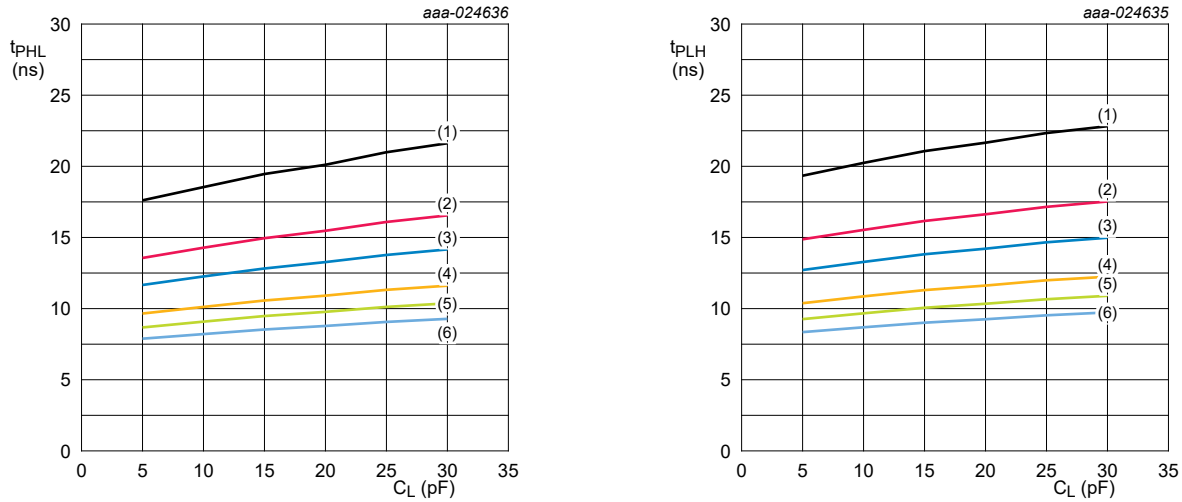


a. HIGH to LOW propagation delay (STCP to Qn)

b. LOW to HIGH propagation delay (STCP to Qn)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

Fig. 12. Typical propagation delay versus load capacitance; $V_{CC(A)}$ = 1.2 V; T_{amb} = 25 °C

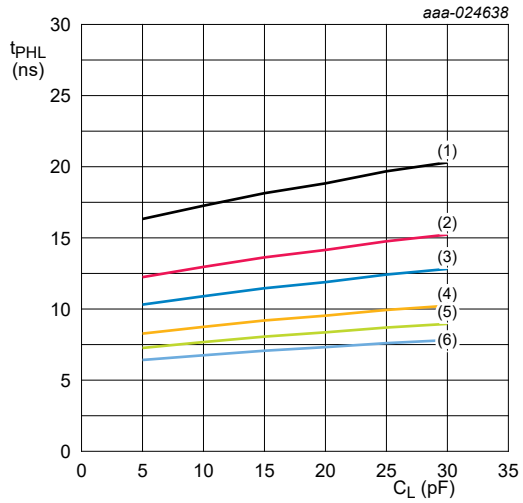


a. HIGH to LOW propagation delay (STCP to Qn)

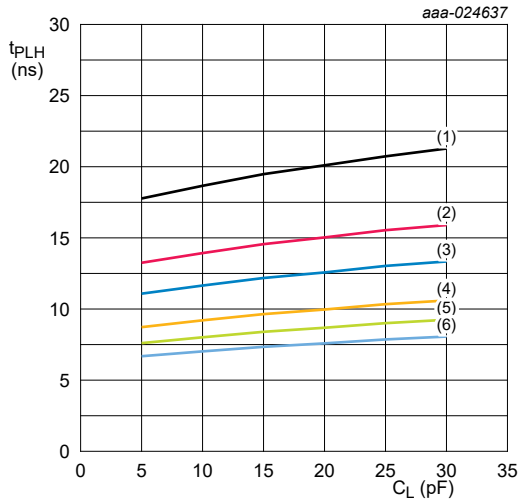
b. LOW to HIGH propagation delay (STCP to Qn)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

Fig. 13. Typical propagation delay versus load capacitance; $V_{CC(A)}$ = 1.5 V; T_{amb} = 25 °C



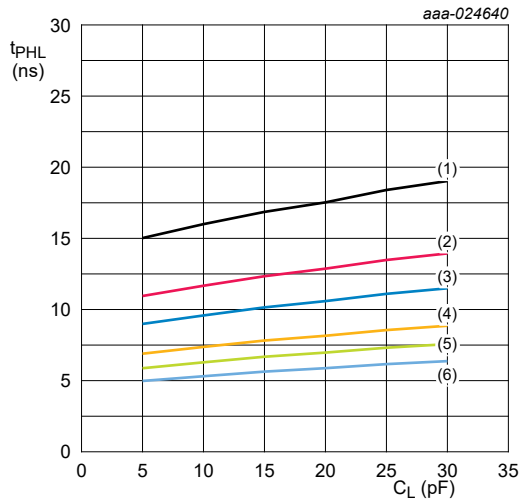
a. HIGH to LOW propagation delay (STCP to Qn)



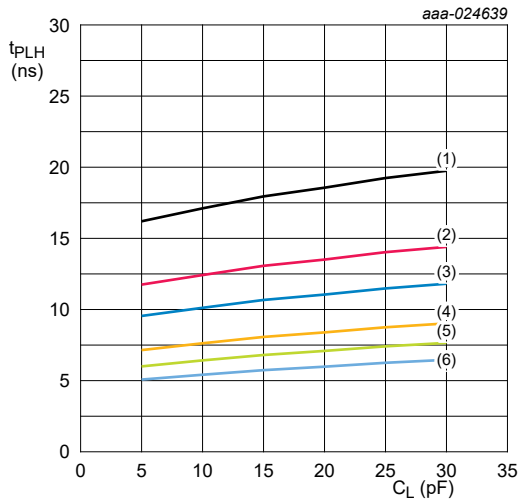
b. LOW to HIGH propagation delay (STCP to Qn)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

Fig. 14. Typical propagation delay versus load capacitance; $V_{CC(A)}$ = 1.8 V; T_{amb} = 25 °C



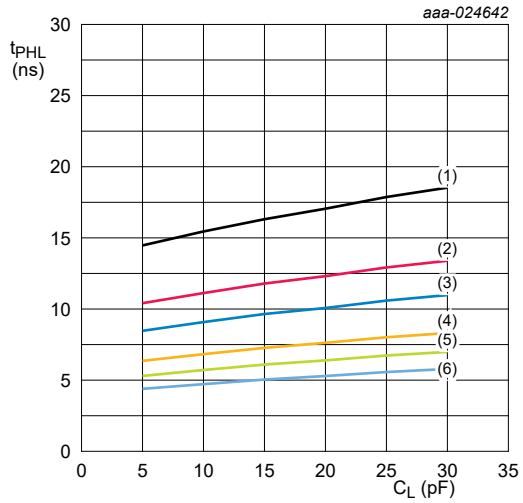
a. HIGH to LOW propagation delay (STCP to Qn)



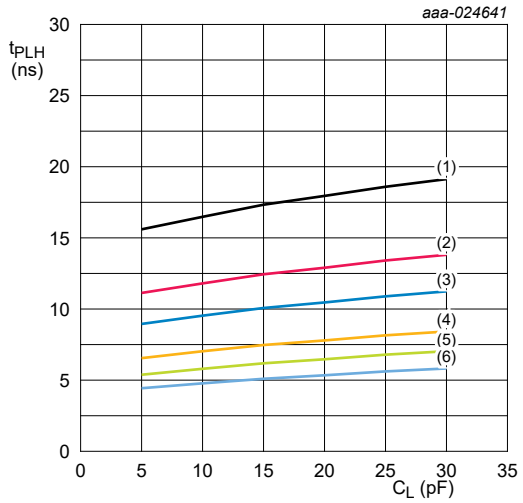
b. LOW to HIGH propagation delay (STCP to Qn)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

Fig. 15. Typical propagation delay versus load capacitance; $V_{CC(A)}$ = 2.5 V; T_{amb} = 25 °C



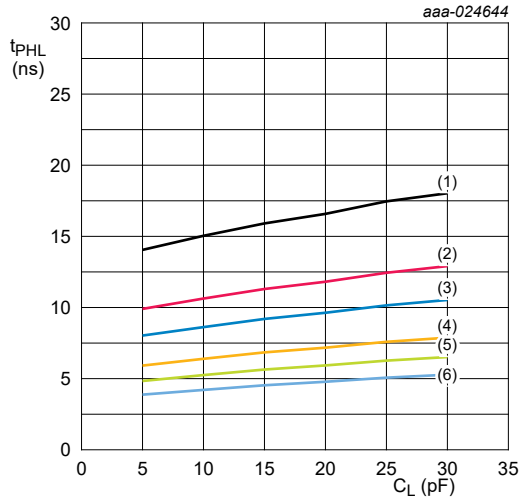
a. HIGH to LOW propagation delay (STCP to Qn)



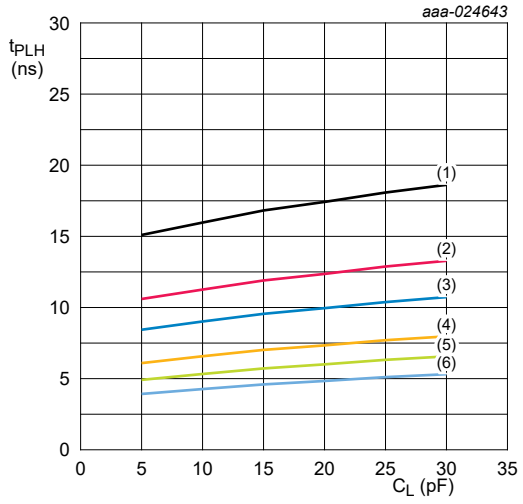
b. LOW to HIGH propagation delay (STCP to Qn)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

Fig. 16. Typical propagation delay versus load capacitance; $V_{CC(A)}$ = 3.3 V; T_{amb} = 25 °C



a. HIGH to LOW propagation delay (STCP to Qn)



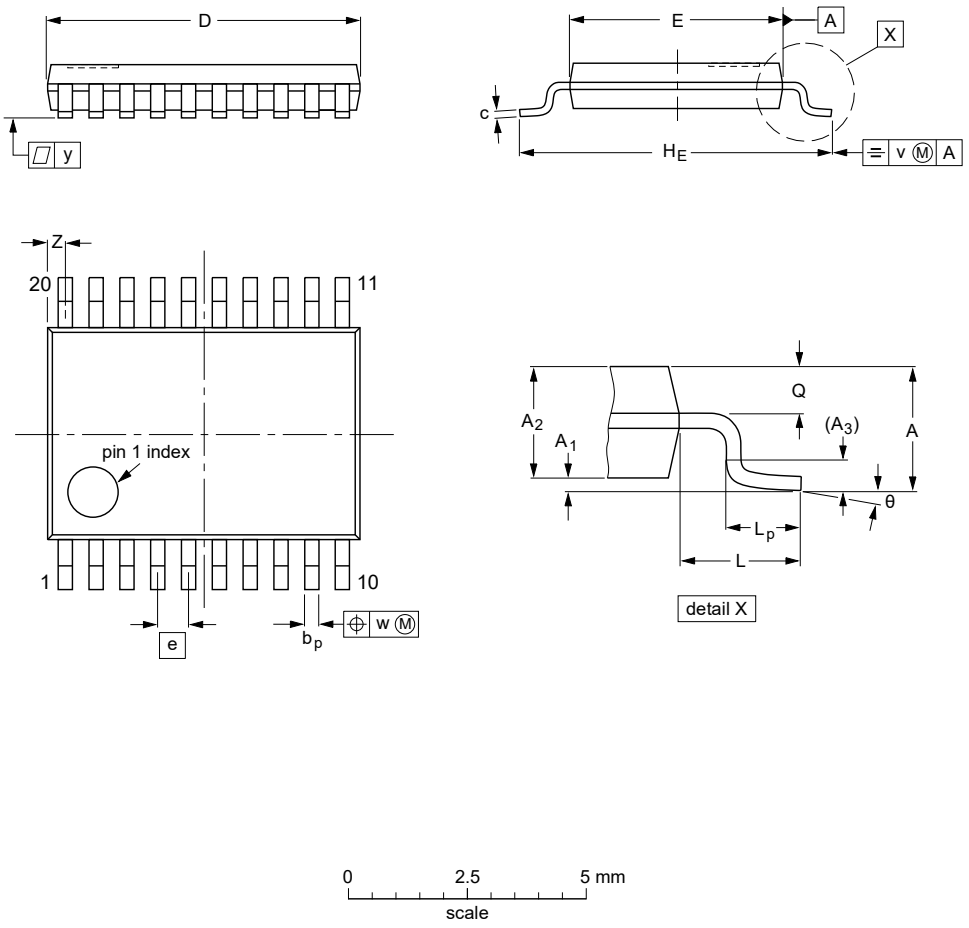
b. LOW to HIGH propagation delay (STCP to Qn)

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V
(6) $V_{CC(B)}$ = 5.0 V

Fig. 17. Typical propagation delay versus load capacitance; $V_{CC(A)}$ = 5 V; T_{amb} = 25 °C

11. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

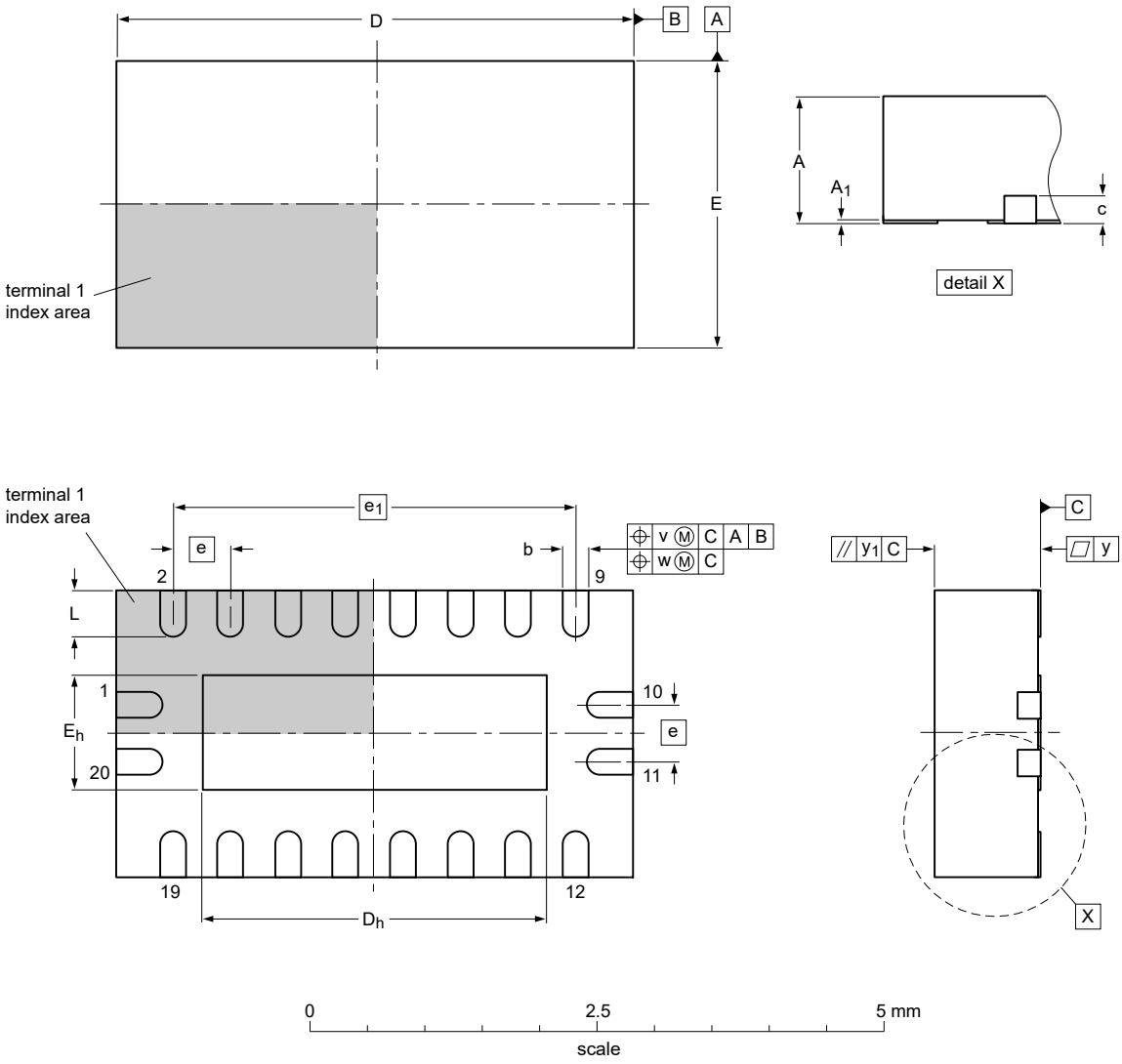
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 18. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Fig. 19. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 19. Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC8T595 v.2	20230829	Product data sheet	-	74LVC8T595 v.1
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74LVC8T595 v.1	20170509	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 29 August 2023

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