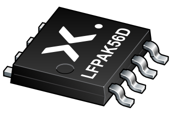


PSMN6R8-40HS

N-channel 40 V, 6.8 mOhm, standard level MOSFET in LFPAK56D using TrenchMOS technology

19 October 2022 | Product data sheet

1. General description

Dual standard level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology.

2. Features and benefits

- Dual MOSFET
- Repetitive avalanche rated
- High reliability LFPAK56D package
- Copper-clip, solder die attach
- Qualified to 175 °C

3. Applications

- Brushless DC motor control
- DC-to-DC converters
- High-performance synchronous rectification
- High performance and high efficiency server power supply

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	40	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	64	W
T_j	junction temperature			-55	-	175	°C
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 12		-	5.8	6.8	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 175 °C; Fig. 12; Fig. 13		-	11	13.4	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	I_D = 20 A; V_{DS} = 32 V; V_{GS} = 20 V; T_j = 25 °C; Fig. 14; Fig. 15		-	9.1	-	nC
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		-	28.9	-	nC
Avalanche ruggedness FET1 and FET2							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 40 A; V_{sup} ≤ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; Fig. 4	[1] [2]	-	-	130	mJ

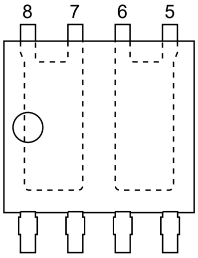
nexperia

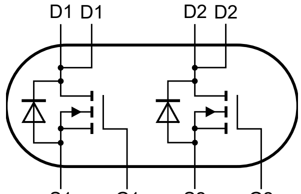
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode FET1 and FET2							
Q_r	recovered charge	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C		-	11.3	-	nC

[1] Refer to application note AN10273 for further information
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

5. Pinning information

Table 2. Pinning information

<table>
<tr><th>Pin</th><th>Symbol</th><th>Description</th><th>Simplified outline</th><th>Graphic symbol</th></tr>
<tr><td>1</td><td>S1</td><td>source1</td><td rowspan="8">

LFPAK56D; Dual LFPAK (SOT1205)</td><td rowspan="8">
</td></tr>
<tr><td>2</td><td>G1</td><td>gate1</td></tr>
<tr><td>3</td><td>S2</td><td>source2</td></tr>
<tr><td>4</td><td>G2</td><td>gate2</td></tr>
<tr><td>5</td><td>D2</td><td>drain2</td></tr>
<tr><td>6</td><td>D2</td><td>drain2</td></tr>
<tr><td>7</td><td>D1</td><td>drain1</td></tr>
<tr><td>8</td><td>D1</td><td>drain1</td></tr>
</table>

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R8-40HS	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN6R8-40HS	6R8S40H

8. Limiting values

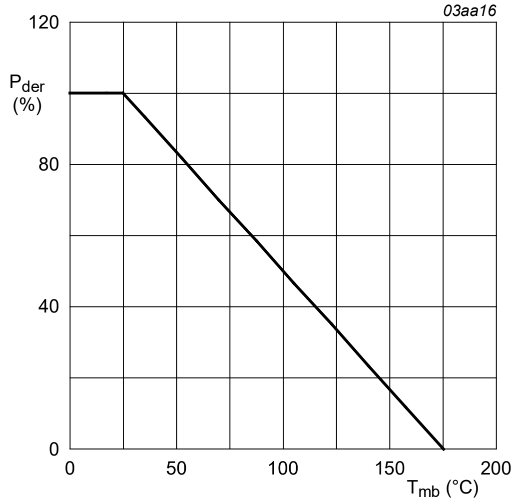
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage	DC; T_j ≤ 175 °C		-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	64	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	40	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	40	A

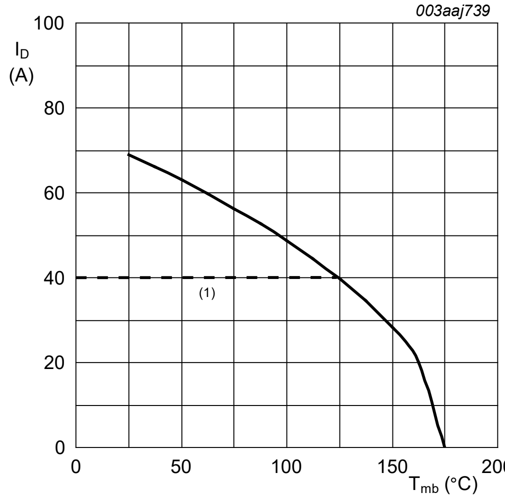
Symbol	Parameter	Conditions		Min	Max	Unit
I_{DM}	peak drain current	pulsed; $t_p \leq$ 10 μs; T_{mb} = 25 °C; Fig. 3		-	276	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode FET1 and FET2						
I_S	source current	T_{mb} = 25 °C		-	40	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 μs; T_{mb} = 25 °C		-	276	A
Avalanche ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 40 A; $V_{sup} \leq$ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; Fig. 4	[1] [2]	-	130	mJ

[1] Refer to application note AN10273 for further information
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



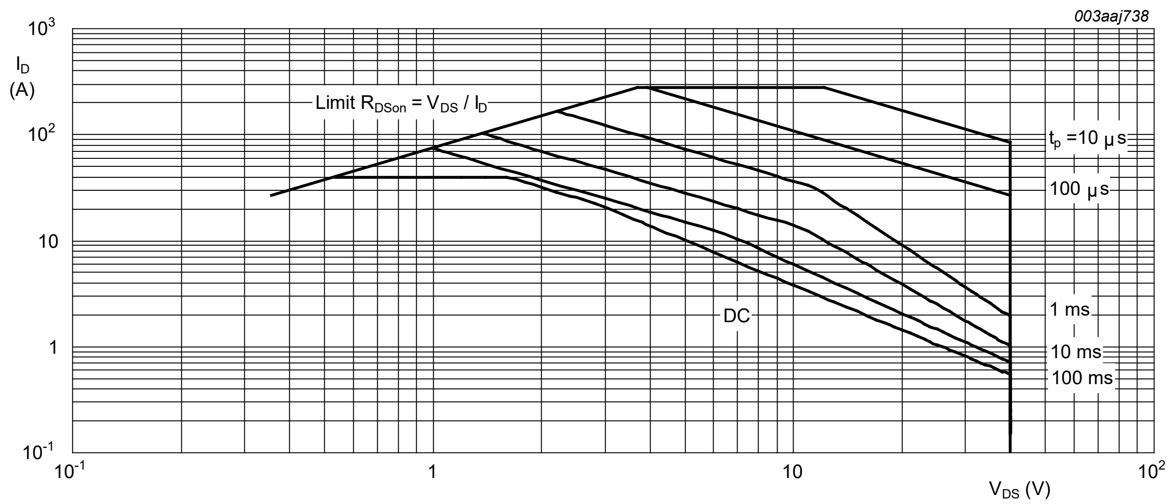
$$P_{der} = \frac{P_{tot}}{P_{tot\,(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



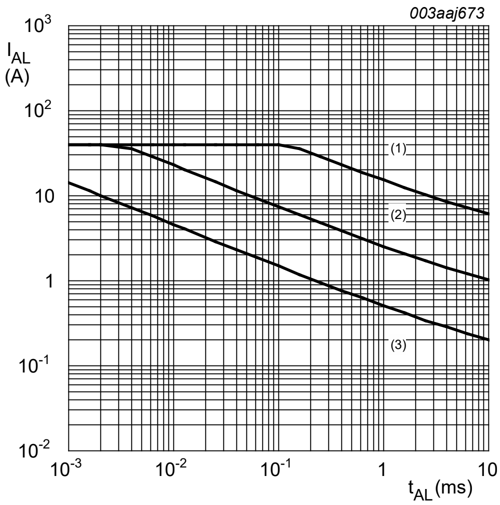
V_{GS} 10 ≥ V; (1) Capped at 40 A due to package.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse; (1) Capped at 40 A due to package.

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) single pulse, T_j = 25 °C; (2) single pulse, T_j = 150 °C; (3) repetitive.

Fig. 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	2.36	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board		-	95	-	K/W

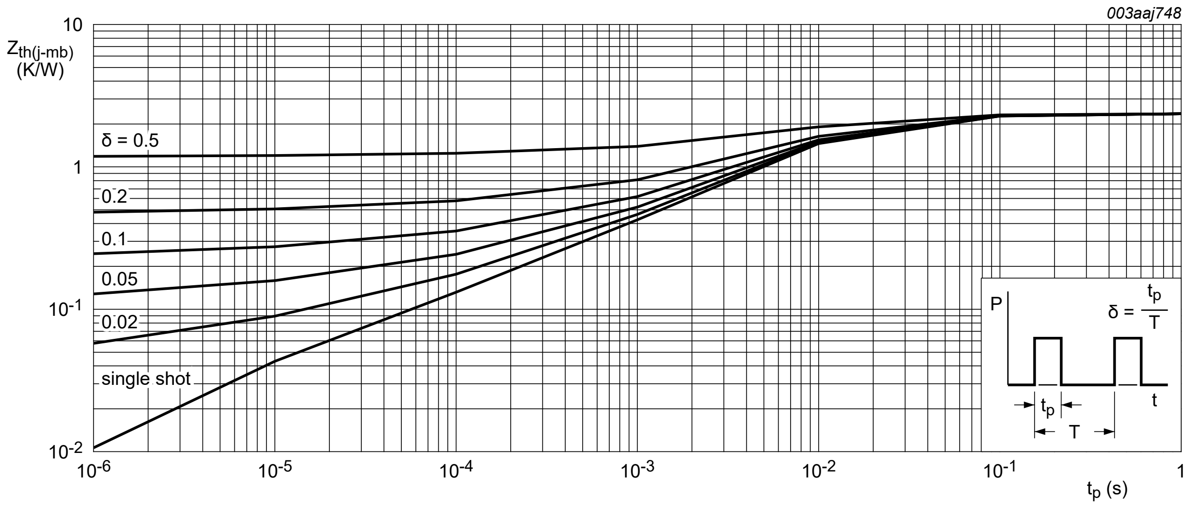
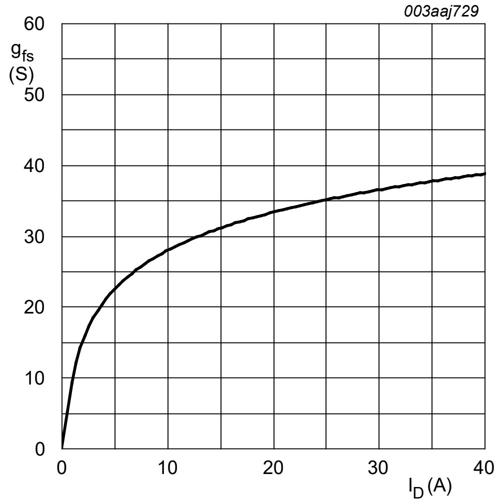


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

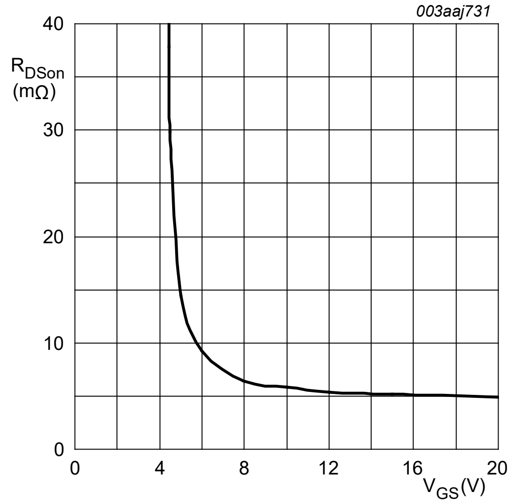
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		2.4	3	4	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 10; Fig. 11		1	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 10; Fig. 11		-	-	4.5	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.02	1	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 12		-	5.8	6.8	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 175 °C; Fig. 12; Fig. 13		-	11	13.4	mΩ
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		-	28.9	-	nC
Q_{GS}	gate-source charge			-	7	-	nC
Q_{GD}	gate-drain charge	I_D = 20 A; V_{DS} = 32 V; V_{GS} = 20 V; T_j = 25 °C; Fig. 14; Fig. 15		-	9.1	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	1460	1947	pF
C_{oss}	output capacitance			-	324	389	pF
C_{rss}	reverse transfer capacitance			-	197	270	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 32 V; R_L = 1.6 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	8.9	-	ns
t_r	rise time			-	15.4	-	ns
$t_{d(off)}$	turn-off delay time			-	19.4	-	ns
t_f	fall time			-	16.5	-	ns
Source-drain diode FET1 and FET2							
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.78	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C		-	20.6	-	ns
Q_r	recovered charge			-	11.3	-	nC



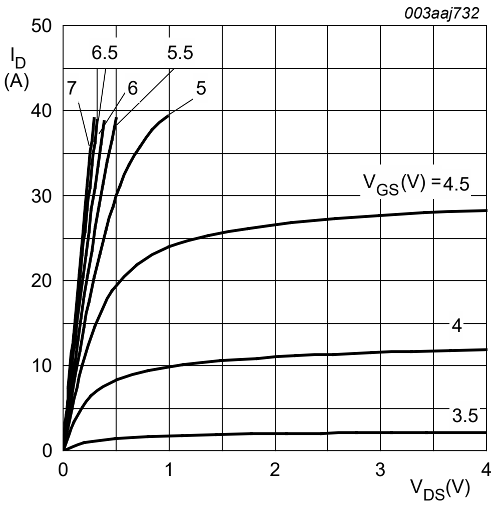
T_j = 25 °C; V_{DS} = 15 V

Fig. 6. Forward transconductance as a function of drain current; typical values



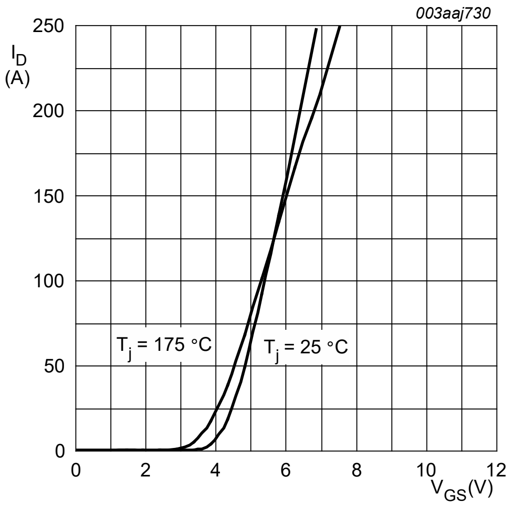
T_j = 25 °C; I_D = 20 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



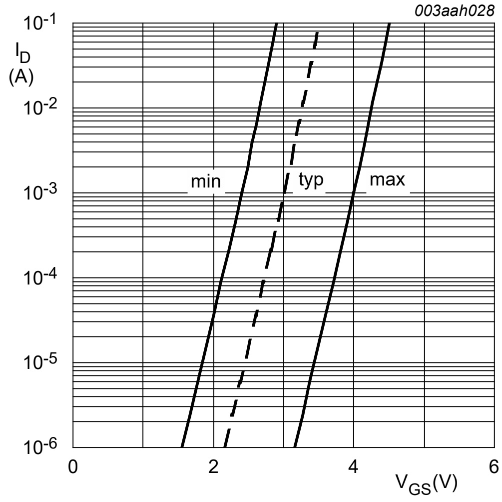
T_j = 25 °C

Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values



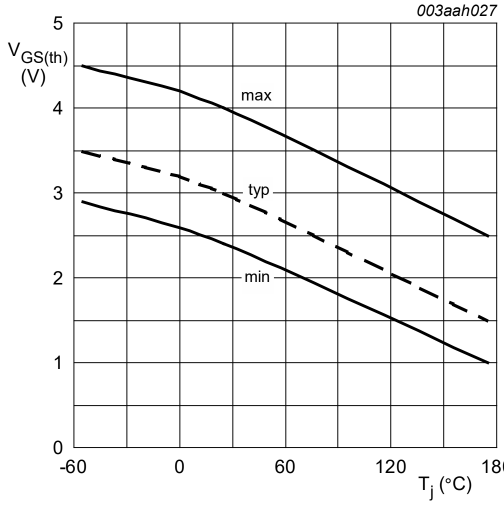
V_{DS} = 10 V

Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



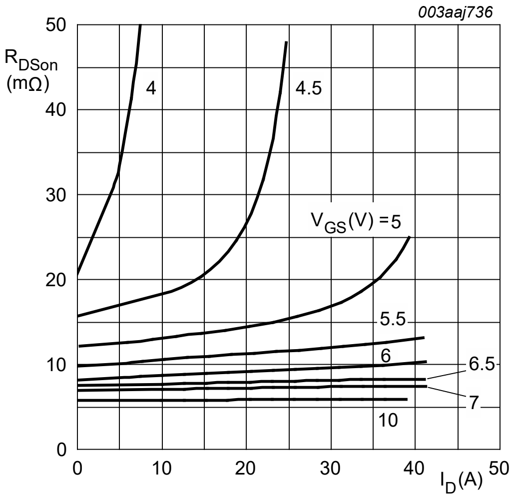
T_j = 25 °C; V_{DS} = 5 V

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



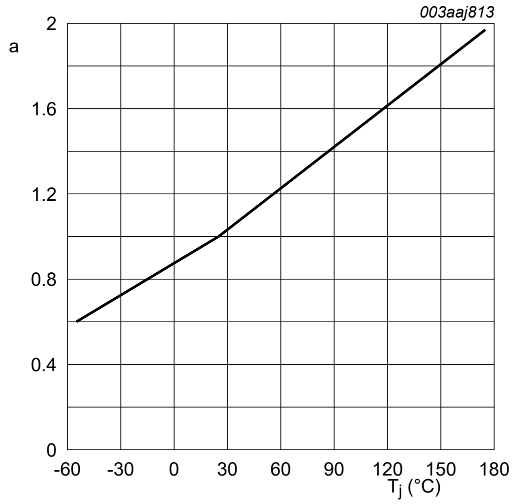
I_D = 1 mA; V_{DS} = V_{GS}

Fig. 11. Gate-source threshold voltage as a function of junction temperature



T_j = 25 °C

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}\,(25°C)}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

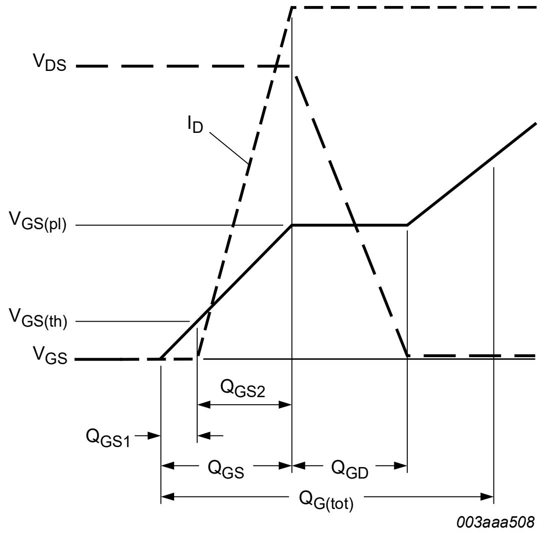
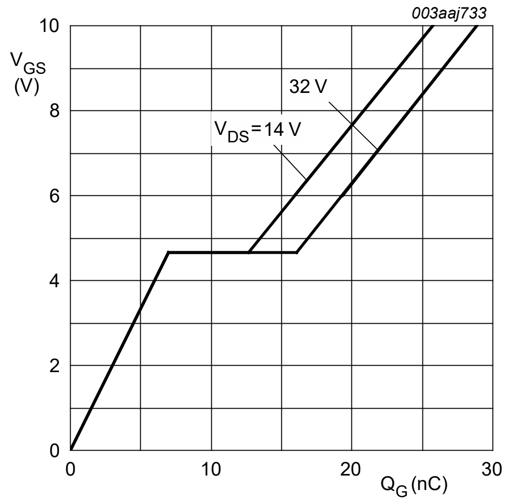
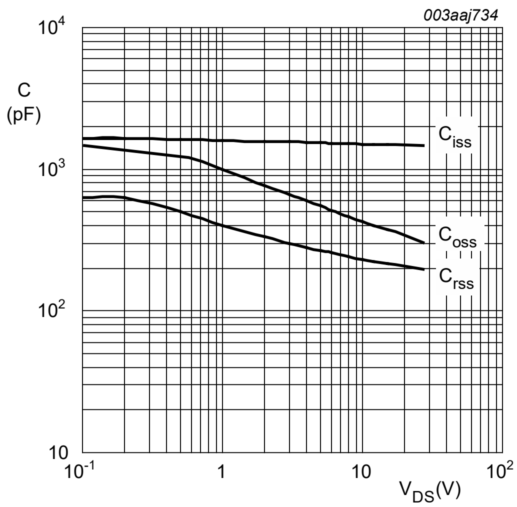


Fig. 14. Gate charge waveform definitions



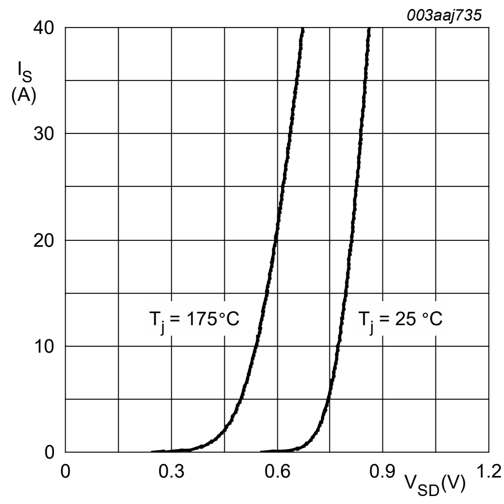
T_j = 25 °C; I_D = 20 A

Fig. 15. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V; f = 1 MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

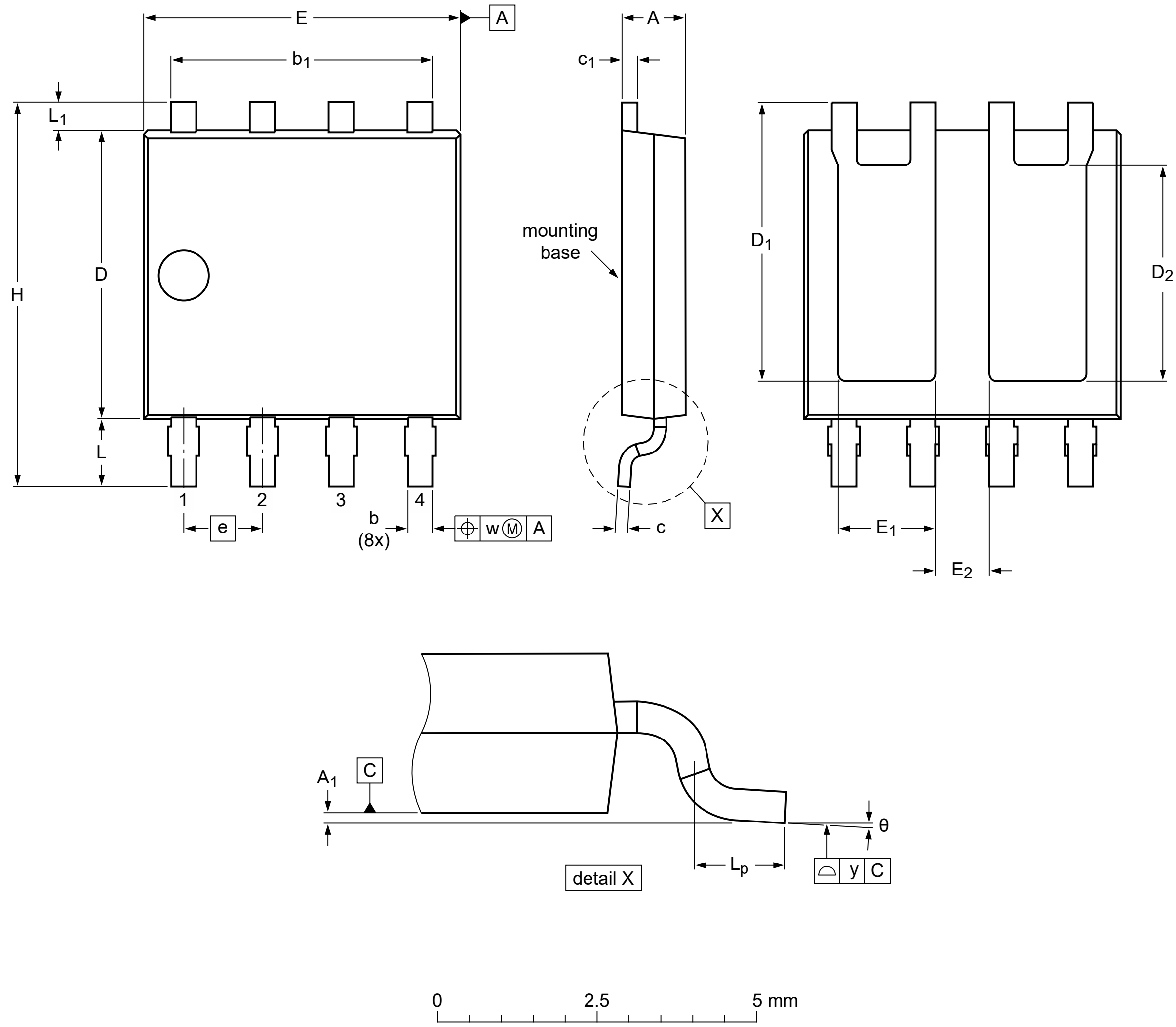


V_{GS} = 0 V

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads **SOT1205**



Dimensions

Unit		A	A_1	b	b_1	c	c_1	$D^{(1)}$	$D_1^{(1)}$	D_2 (ref)	$E^{(1)}$	$E_1^{(1)}$	E_2	e	H	L	L_1	L_p	w	y	θ
mm	max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85			8°
	nom													1.27					0.25	0.1	
	min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						~~14-08-21~~ 14-10-28

Fig. 18. Package outline LFPAK56D; Dual LFPAK (SOT1205)

12. Soldering

Footprint information for reflow soldering of LFPAK56D package **SOT1205**

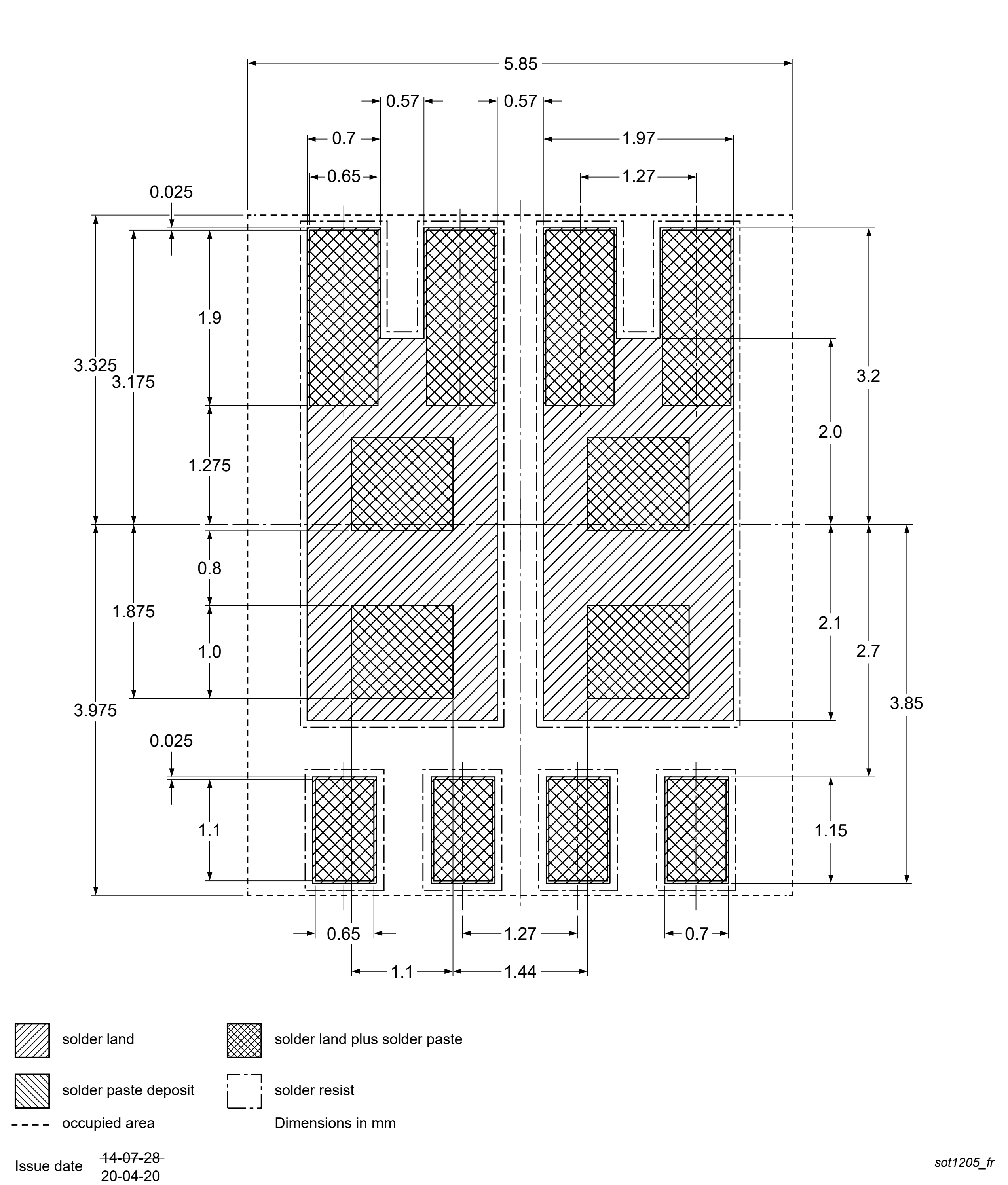


Fig. 19. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 19 October 2022

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