PIMC31PAS-Q

50 V, 500 mA NPN/PNP Resistor-Equipped double Transistor; R1 = 1 kΩ, R2 = 10 kΩ

31 August 2023 Product data sheet

1. General description

NPN/PNP Resistor-Equipped double Transistor (RET) in a medium power SOT1118D (DFN2020D-6) leadless Surface-Mounted Device (SMD) plastic package with side-wettable flanks (SWF).

NPN/NPN complement: PIMN31PAS-Q

PNP/PNP complement: PIMP31PAS-Q

2. Features and benefits

- 500 mA output current capability
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Digital applications
- Cost-saving alternative to BC807 / BC817 series in digital applications
- Control of IC inputs
- Switching loads

4. Quick reference data

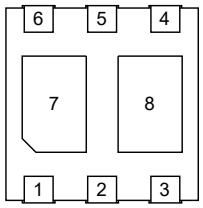
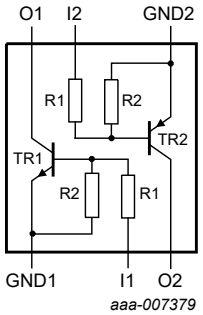
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{CEO}	collector-emitter voltage	open base	[1]	-	-	50	V
I_O	output current		[1]	-	-	500	mA
R1	bias resistor 1 (input)	T_{amb} = 25 °C	[2]	0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		[2]	9	10	11	

[1] For the PNP transistor with negative polarity.
[2] See section "Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 Transparent top view **DFN2020D-6 (SOT1118D)**	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PIMC31PAS-Q	DFN2020D-6	plastic, leadless thermally enhanced ultra thin and small outline package with side-wettable flanks (SWF); 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1118D

7. Marking

Table 4. Marking codes

Type number	Marking code
PIMC31PAS-Q	8E

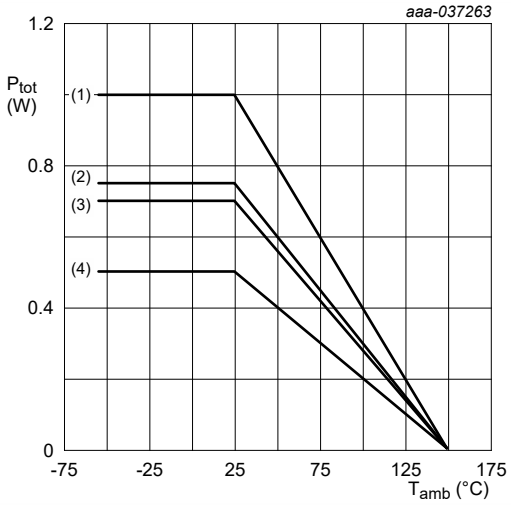
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter	[1]	-	50	V
V_{CEO}	collector-emitter voltage	open base	[1]	-	50	V
V_{EBO}	emitter-base voltage	open collector	[1]	-	5	V
V_I	input voltage		[1]	-5	10	V
I_O	output current		[1]	-	500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[2]	-	360	mW
			[3]	-	550	mW
			[4]	-	510	mW
			[5]	-	730	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[2]	-	500	mW
			[3]	-	750	mW
			[4]	-	700	mW
			[5]	-	1	W
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] For the PNP transistor with negative polarity.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.
[3] Device mounted on an FR4 PCB, single-sided, 35µm copper, tin-plated; mounting pad for collector 1 cm^2.
[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
[5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 cm^2.



(1) FR4 PCB, 4-layer copper, 1 cm^2
(2) FR4 PCB, single-sided, 35µm copper, 1 cm^2
(3) FR4 PCB, 4-layer copper, standard footprint
(4) FR4 PCB, single-sided, 35µm copper, standard footprint

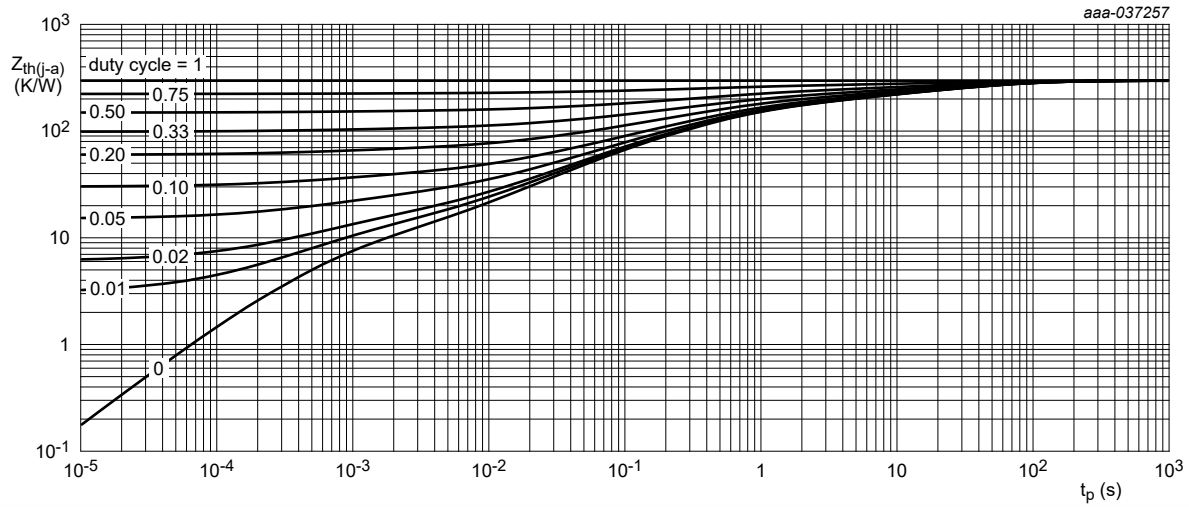
Fig. 1. Per device: Power derating curves for DFN2020D-6 (SOT1118D)

9. Thermal characteristics

Table 6. Thermal characteristics

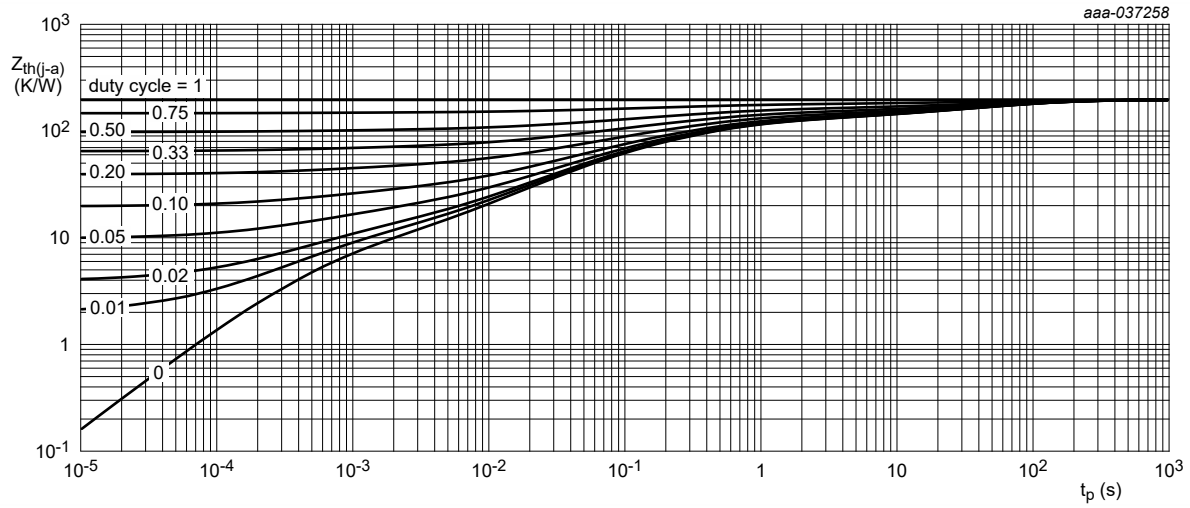
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	348	K/W
			[2]	-	-	228	K/W
			[3]	-	-	246	K/W
			[4]	-	-	172	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W
			[2]	-	-	167	K/W
			[3]	-	-	179	K/W
			[4]	-	-	125	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided, 35µm copper, tin-plated; mounting pad for collector 1 cm^2.
[3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 cm^2.



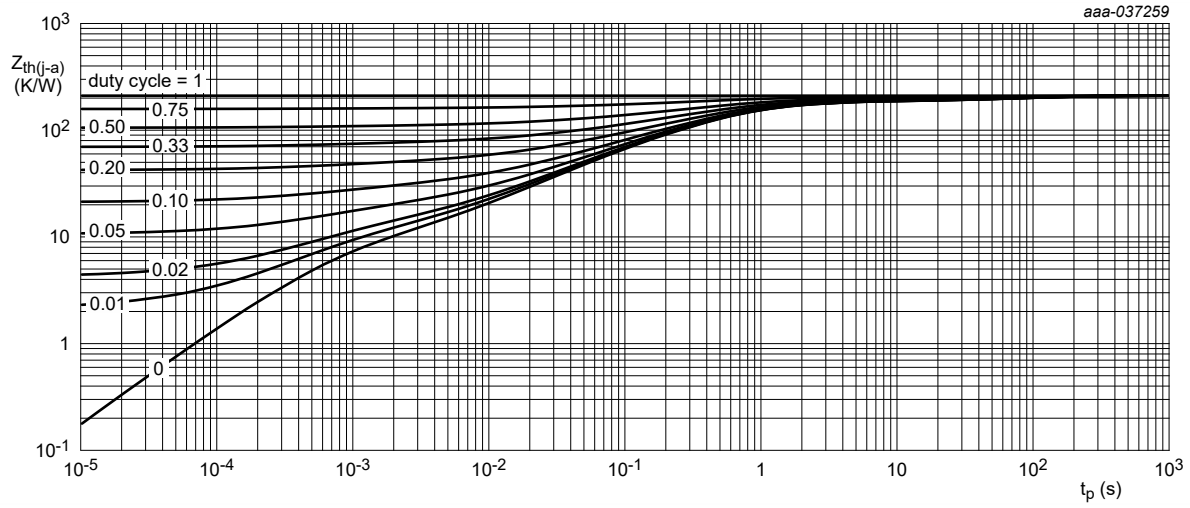
FR4 PCB, single-sided, 35µm copper, tin-plated and standard footprint

Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



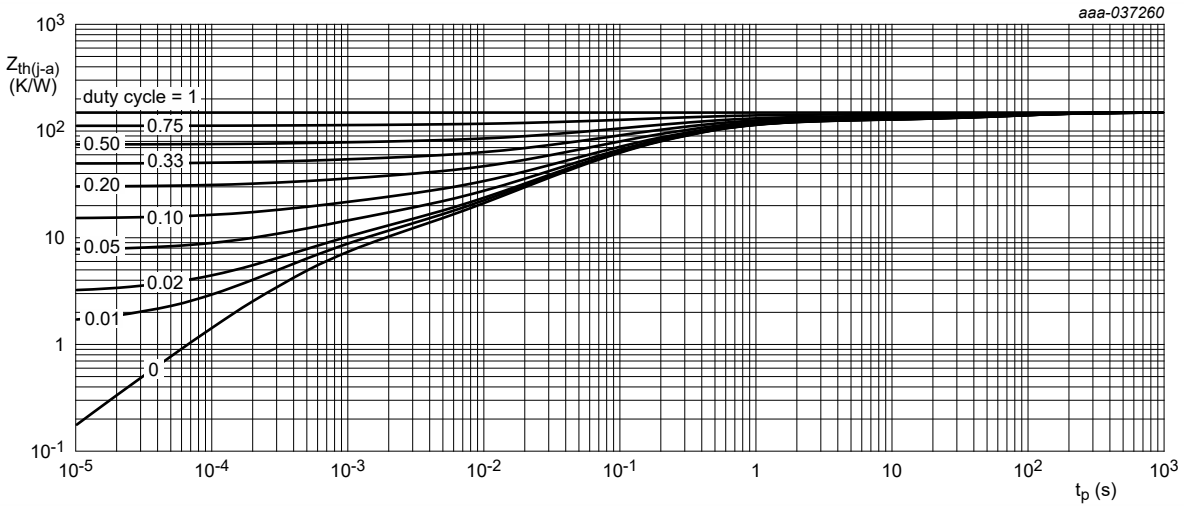
FR4 PCB, single-sided, 35µm copper, tin-plated, mounting pad for collector 1 cm^2.

Fig. 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, tin-plated and standard footprint.

Fig. 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm^2.

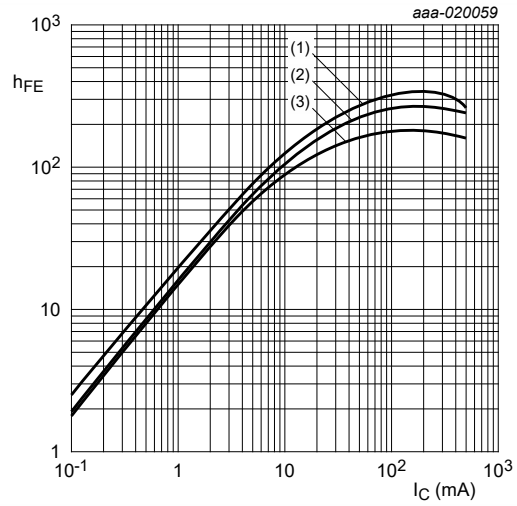
Fig. 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

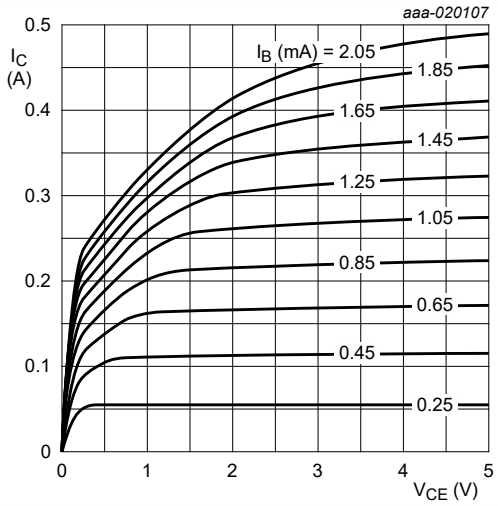
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A; T_{amb} = 25 °C	[1]	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 10 mA; I_B = 0 A; T_{amb} = 25 °C	[1]	50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A; T_{amb} = 25 °C	[1]	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 50 V; I_B = 0 A; T_{amb} = 25 °C	[1]	-	-	0.5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A; T_{amb} = 25 °C	[1]	-	-	0.72	mA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 50 mA; T_{amb} = 25 °C	[1]	70	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 50 mA; I_B = 2.5 mA; T_{amb} = 25 °C	[1]	-	-	100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA; T_{amb} = 25 °C	[1]	0.3	0.6	1	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 20 mA; T_{amb} = 25 °C	[1]	0.4	0.8	1.4	V
R1	bias resistor 1 (input)	T_{amb} = 25 °C	[2]	0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		[2]	9	10	11	
TR1 (NPN)							
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	5	-	pF
f_T	transition frequency	V_{CE} = 5 V; I_C = 50 mA; f = 100 MHz; T_{amb} = 25 °C	[3]	-	210	-	MHz
TR2 (PNP)							
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	7	-	pF
f_T	transition frequency	V_{CE} = -5 V; I_C = -50 mA; f = 100 MHz; T_{amb} = 25 °C	[3]	-	150	-	MHz

[1] For the PNP transistor with negative polarity.
[2] See section "Test information" for resistor calculation and test conditions.
[3] Characteristics of built-in transistor.



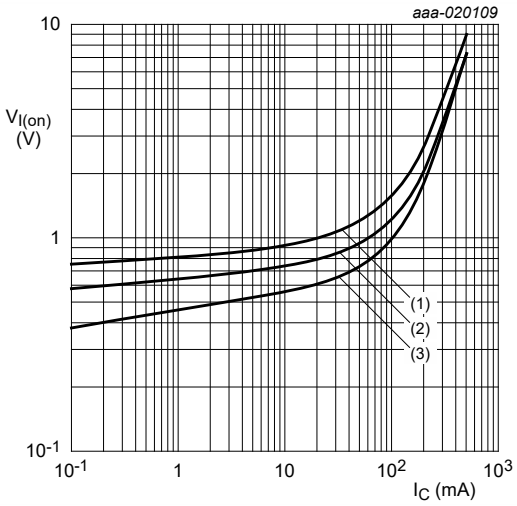
V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −40 °C

Fig. 6. TR1 (NPN): DC current gain as a function of collector current; typical values



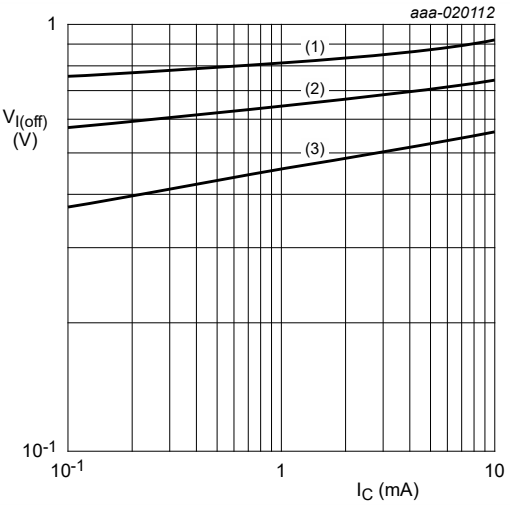
T_{amb} = 25 °C

Fig. 7. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values



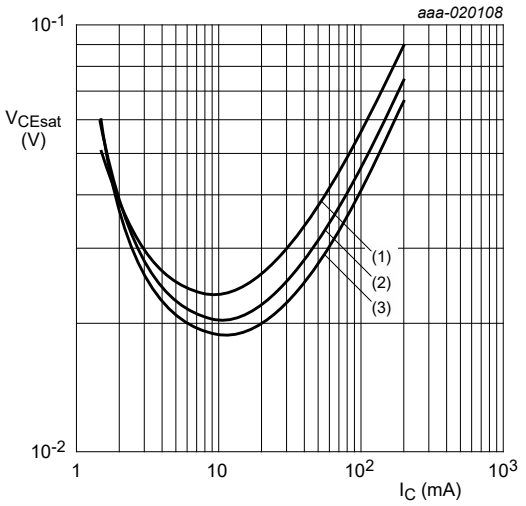
V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 8. TR1 (NPN): On-state input voltage as a function of collector current; typical values



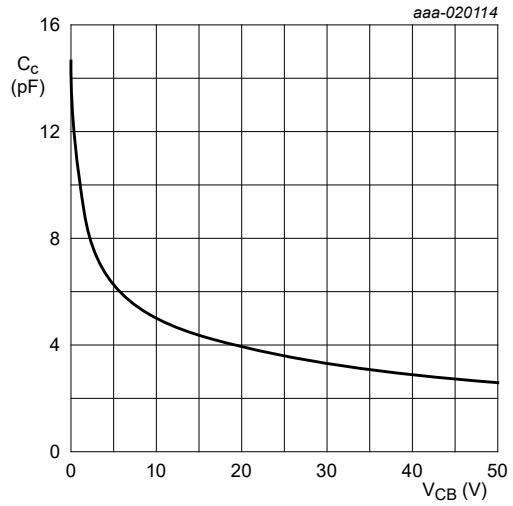
V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 9. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



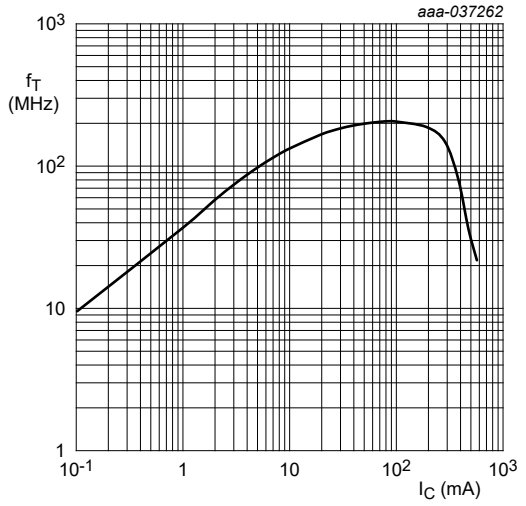
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −40 °C

Fig. 10. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



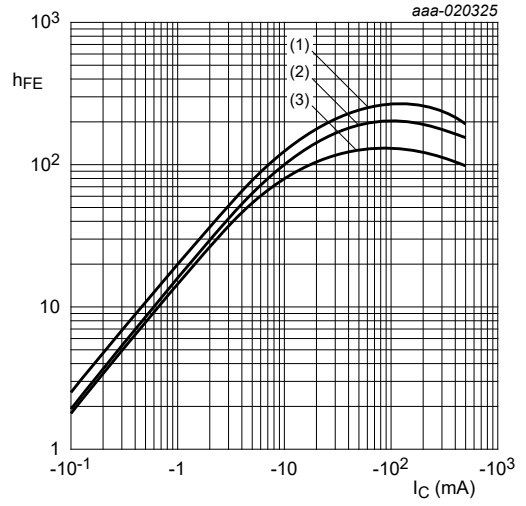
f = 1 MHz
T_{amb} = 25 °C

Fig. 11. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



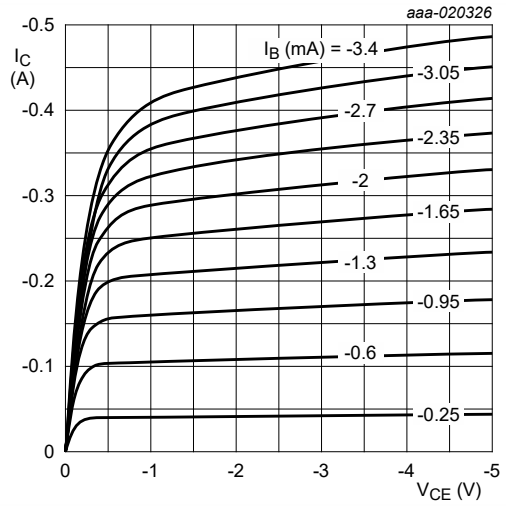
f = 100 MHz; V_{CE} = -5 V T_{amb} = 25 °C

Fig. 12. TR2 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



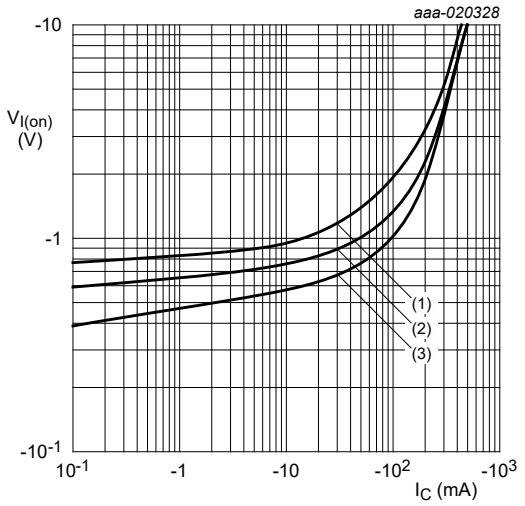
V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −40 °C

Fig. 13. TR2 (PNP): DC current gain as a function of collector current; typical values



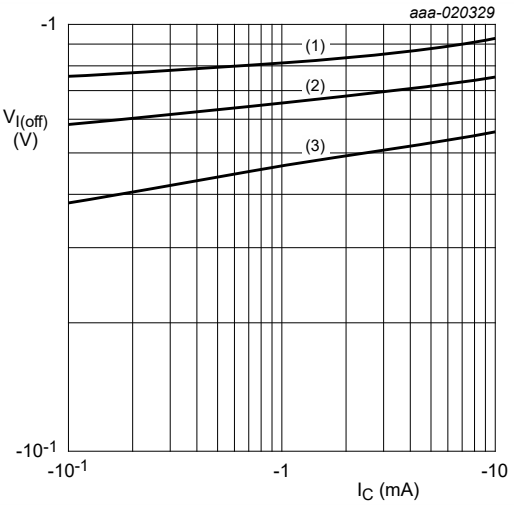
T_{amb} = 25 °C

Fig. 14. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values



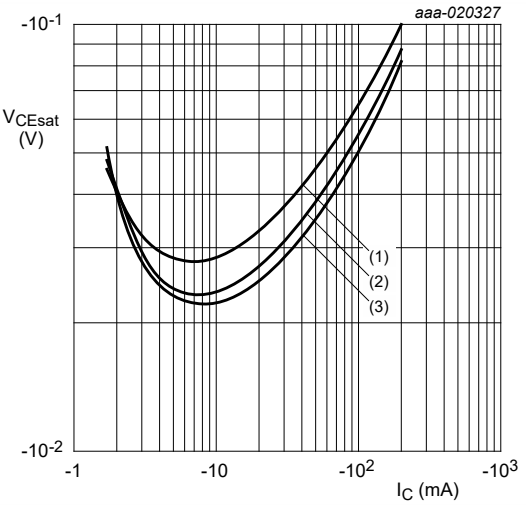
V_{CE} = -0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 15. TR2 (PNP): On-state input voltage as a function of collector current; typical values



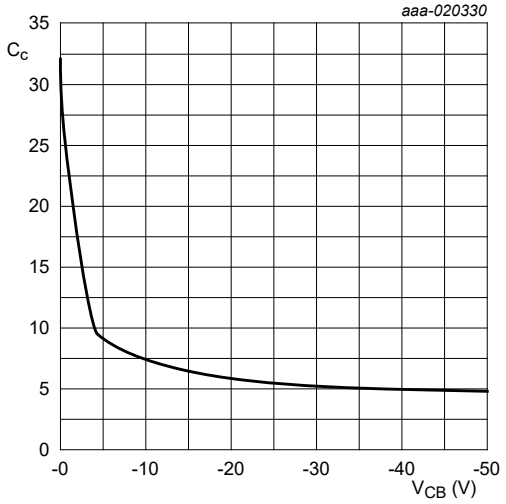
V_{CE} = -5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 16. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



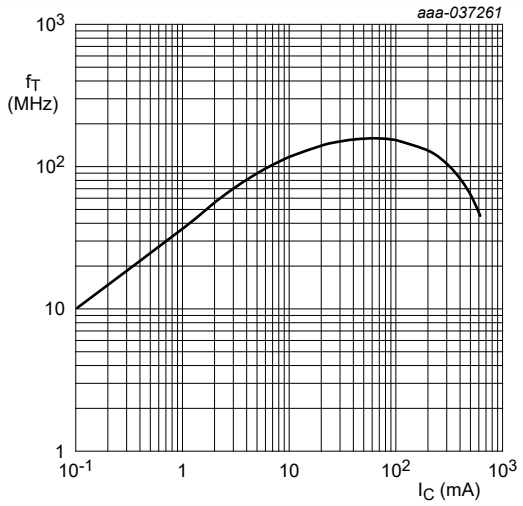
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −40 °C

Fig. 17. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



f = 1 MHz
T_{amb} = 25 °C

Fig. 18. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values



f = 100 MHz; V_{CE} = 5 V T_{amb} = 25 °C

Fig. 19. TR1 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1):

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1):

$$\frac{R2}{R1} = \frac{V(I_4) - V(I_3)}{R1 \cdot (I_4 - I_3)} - 1$$

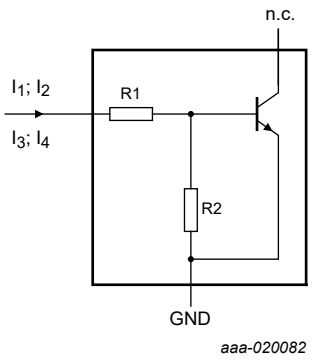


Fig. 20. NPN transistor: Resistor test circuit

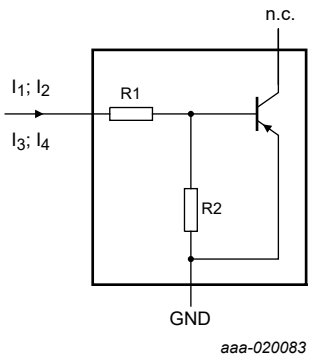


Fig. 21. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PIMC31PAS-Q	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I_1	I_2	I_3	I_4
TR1 (NPN)	1	10	0.7 mA	0.8 mA	-0.45 mA	-0.55 mA
TR2 (PNP)			-0.7 mA	-0.8 mA	0.45 mA	0.55 mA

12. Package outline

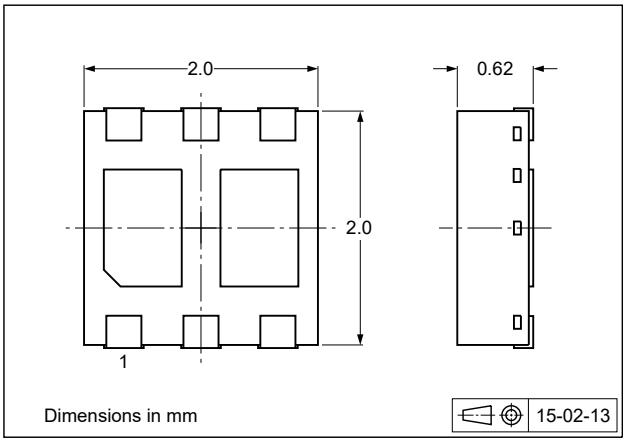


Fig. 22. Package outline DFN2020D-6 (SOT1118D)

13. Soldering

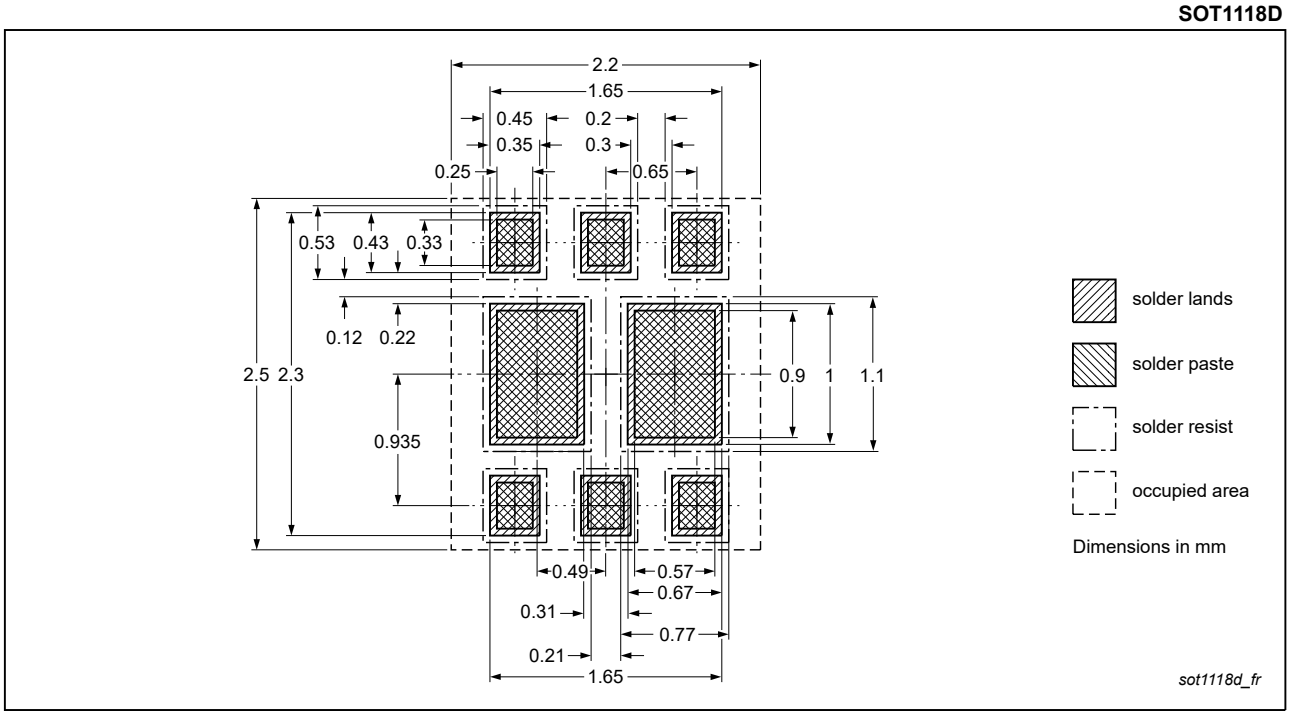


Fig. 23. Reflow soldering footprint for DFN2020D-6 (SOT1118D)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PIMC31PAS-Q v.1	20230831	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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