74AHC139; 74AHCT139

Dual 2-to-4 line decoder/demultiplexer

Rev. 4 — 29 February 2024 Product data sheet

1. General description

The 74AHC139; 74AHCT139 decodes two binary weighted address inputs (nA0, nA1) to four mutually exclusive outputs ($n\overline{Y}0$ to $n\overline{Y}3$). Each decoder features an enable input ($n\overline{E}$). When $n\overline{E}$ is HIGH all outputs are forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features and benefits

- Wide supply voltage range from 2.0 to 5.5 V
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- High noise immunity
- Overvoltage tolerant inputs to 5.5 V
- Input levels:
  - For 74AHC139: CMOS level
  - For 74AHCT139: TTL level
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC139D 74AHCT139D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC139PW 74AHCT139PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

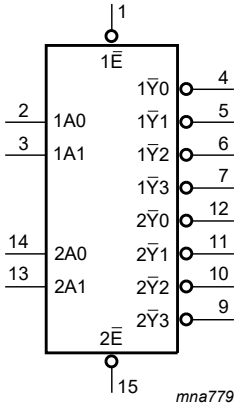
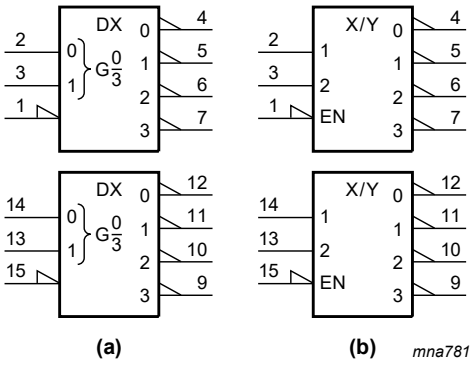


Fig. 1. Logic symbol



a = demultiplexer and b = decoder

Fig. 2. IEC logic symbol

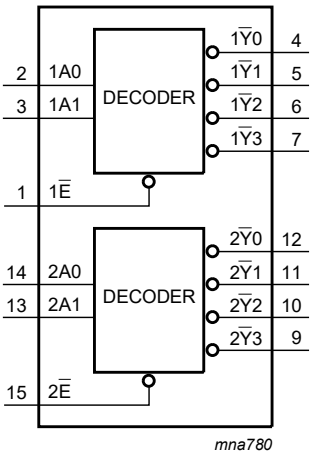
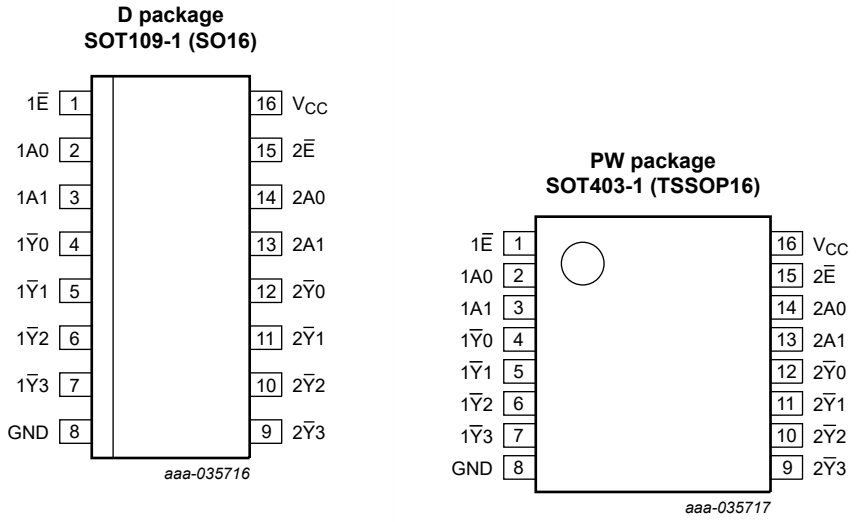


Fig. 3. Functional diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{E}$, 2$\overline{E}$	1, 15	enable input (active LOW)
1A0, 1A1	2, 3	address input
1$\overline{Y}$0, 1$\overline{Y}$1, 1$\overline{Y}$2, 1$\overline{Y}$3	4, 5, 6, 7	output
GND	8	ground (0 V)
2$\overline{Y}$3, 2$\overline{Y}$2, 2$\overline{Y}$1, 2$\overline{Y}$0	9, 10, 11, 12	output
2A1, 2A0	13, 14	address input
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Control	Input		Output			
n$\overline{E}$	**nA0**	**nA1**	**n$\overline{Y}$0**	**n$\overline{Y}$1**	**n$\overline{Y}$2**	**n$\overline{Y}$3**
H	X	X	H	H	H	H
L	L	L	L	H	H	H
	H	L	H	L	H	H
	L	H	H	H	L	H
	H	H	H	H	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage			-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V	[1]	-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	[1]	-20	+20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		-25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			-75	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC139						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT139						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC139										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT139										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V; other pins at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance	V_I = V_{CC} or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC139										
t_{pd}	propagation delay	nAn to nȲn; see Fig. 4 [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	5.5	11.0	1.0	13.0	1.0	14.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	7.9	14.5	1.0	16.5	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	3.9	7.2	1.0	8.5	1.0	9.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.6	9.2	1.0	10.5	1.0	11.5	ns
		nĒ to nȲn; see Fig. 5 [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	4.8	9.2	1.0	11.0	1.0	11.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	6.9	12.7	1.0	14.5	1.0	16.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	3.4	6.3	1.0	7.5	1.0	8.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	4.9	8.3	1.0	9.5	1.0	10.5	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [3]	-	26	-	-	-	-	-	pF
74AHCT139; V_{CC} = 4.5 V to 5.5 V										
t_{pd}	propagation delay	nAn to nȲn; see Fig. 4 [2]								
		C_L = 15 pF	-	4.7	7.2	1.0	8.5	1.0	9.0	ns
		C_L = 50 pF	-	6.5	9.2	1.0	10.5	1.0	11.5	ns
		nĒ to nȲn; see Fig. 5 [2]								
		C_L = 15 pF	-	3.6	6.3	1.0	7.5	1.0	8.0	ns
		C_L = 50 pF	-	5.2	8.3	1.0	9.5	1.0	10.5	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [3]	-	23	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

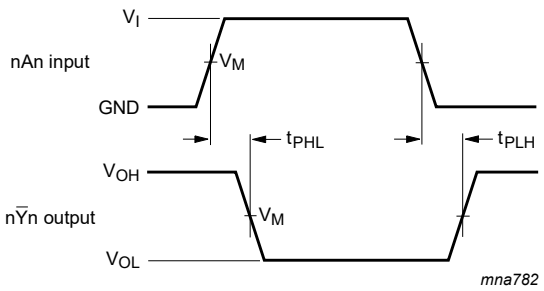
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

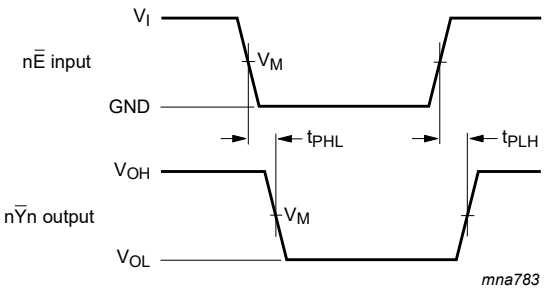
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Address input to output propagation delays



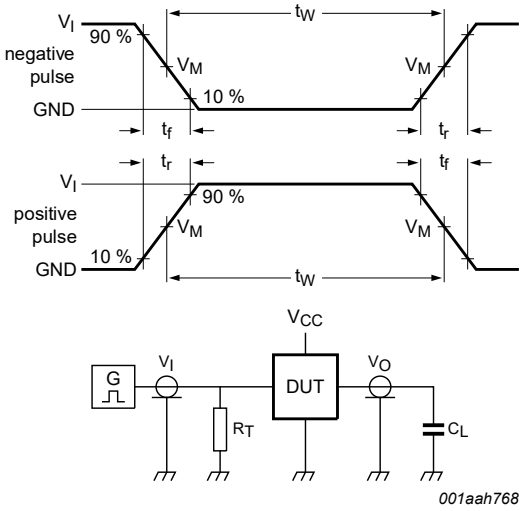
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Enable input to output propagation delays

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC139	0.5 × V_{CC}	0.5 × V_{CC}
74AHCT139	1.5 V	0.5 × V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = load capacitance including jig and probe capacitance.

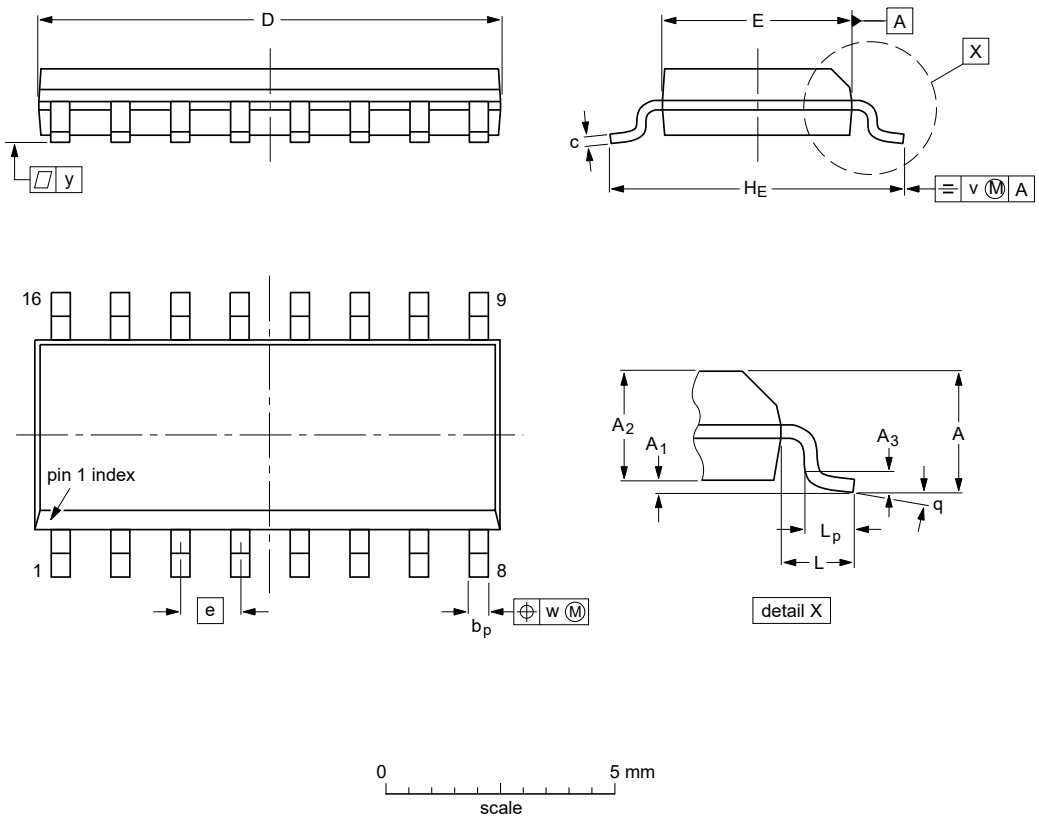
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC139	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT139	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

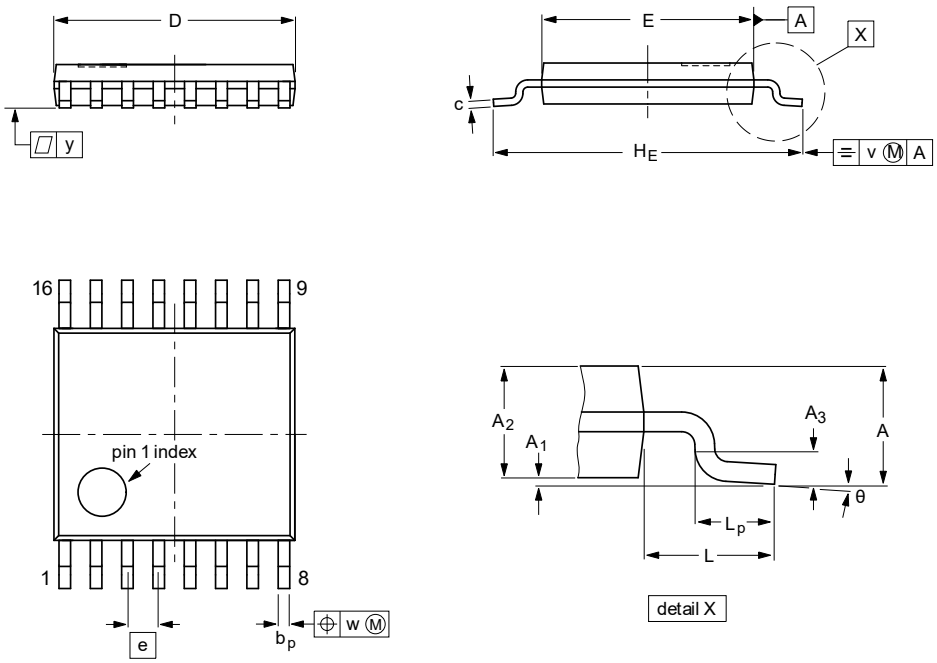
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

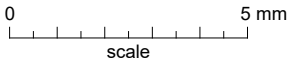
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT139 v.4	20240229	Product data sheet	-	74AHC_AHCT139 v.3
Modifications:	• Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74AHC_AHCT139 v.3	20230907	Product data sheet	-	74AHC_AHCT139 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 updated. • Section 2: updated, ESD specification updated according to the latest JEDEC standard. • Table 4: Derating values for P_{tot} total power dissipation updated.			
74AHC_AHCT139 v.2	20080509	Product data sheet	-	74AHC_AHCT139 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6: the conditions for input leakage current have been changed.			
74AHC_AHCT139 v.1	19990901	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 29 February 2024

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