1. General description

The 74HC14-Q100; 74HCT14-Q100 is a hex inverter with Schmitt-trigger inputs. This device features reduced input threshold levels to allow interfacing to TTL logic levels. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} . Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 to 6.0 V
- · CMOS low power dissipation
- · High noise immunity
- · Unlimited input rise and fall times
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- · Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

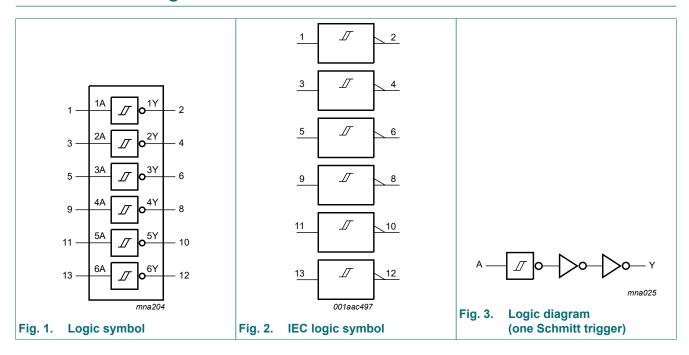


4. Ordering information

Table 1. Ordering information

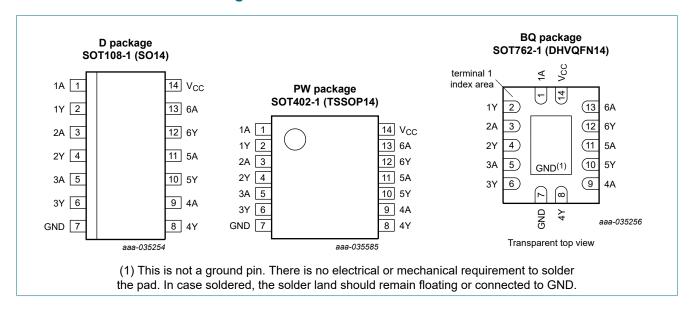
Type number	Package								
	Temperature range	Name	Description	Version					
74HC14D-Q100 74HCT14D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1					
74HC14PW-Q100 74HCT14PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1					
74HC14BQ-Q100 74HCT14BQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1					

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

7. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Input	Output
nA	nY
L	Н
Н	L

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC14-Q100		74H	Unit			
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V_{O}	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

^[2] For SOT108-1 (SO14) package: Ptot derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Ta	_{amb} = 25	°C	T _{amb} =	-40 °C 35 °C		-40 °C 25 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC14	-Q100		•							
V_{OH}	HIGH-level	$V_I = V_{T+}$ or V_{T-}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level	$V_I = V_{T+}$ or V_{T-}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		$I_{O} = 20 \mu A; V_{CC} = 6.0 V$	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT1	4-Q100			'	'			'		
V _{OH}	HIGH-level	$V_{I} = V_{T+} \text{ or } V_{T-}; V_{CC} = 4.5 \text{ V}$								
	output voltage	Ι _Ο = -20 μΑ	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level	$V_{I} = V_{T+} \text{ or } V_{T-}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 20 μA;	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA;	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μA
Δl _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other pins at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	30	108	-	135	-	147	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Fig. 5.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			: -40 °C 85 °C		-40 °C 25 °C		
			Min	Тур	Max	Min	Max	Min	Max	
74HC14	-Q100									
t _{pd}	propagation	nA to nY; see Fig. 4 [1]								
	delay	V _{CC} = 2.0 V	-	41	125	-	155	-	190	ns
		V _{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	21	-	26	-	32	ns
t _t	transition time	see <u>Fig. 4</u> [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	15	-	19	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	7	-	-	-	-	-	pF
74HCT1	4-Q100									
t _{pd}	propagation	nA to nY; see Fig. 4 [1]								
	delay	V _{CC} = 4.5 V	-	20	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
t _t	transition time	$V_{CC} = 4.5 \text{ V}; \text{ see } \frac{\text{Fig. 4}}{}$ [2]	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	per package; [3] V _I = GND to V _{CC} - 1.5 V	-	8	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} . [2] t_t is the same as t_{THL} and t_{TLH} . [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W): $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

$$P_D = C_{DD} \times V_{CO}^2 \times f_1 \times N + \sum_{i=1}^{n} (C_1 \times V_{CO}^2 \times f_2)$$
 where

f_i = input frequency in MHz;

f_o = output frequency in MHz;

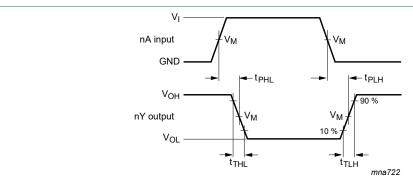
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

11.1. Waveforms and test circuit



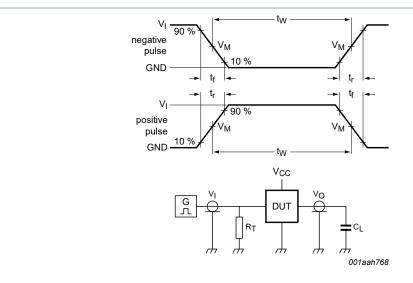
Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Input to output propagation delays

Table 8. Measurement points

Туре	Input	Output				
	V _M	V _M	V _X	V _Y		
74HC14-Q100	0.5 × V _{CC}	0.5 × V _{CC}	0.1 × V _{CC}	0.9 × V _{CC}		
74HCT14-Q100	1.3 V	1.3 V	0.1 × V _{CC}	0.9 × V _{CC}		



Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = load capacitance including jig and probe capacitance.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load	Test
	V _I	t _r , t _f	CL	
74HC14-Q100	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT14-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

74HC_HCT14_Q100

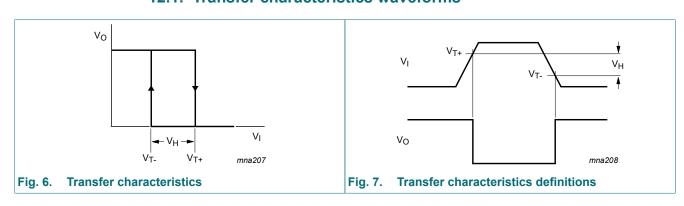
12. Transfer characteristics

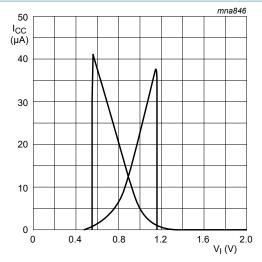
Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Fig. 6 and Fig. 7.

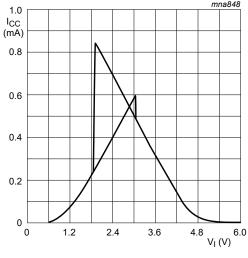
Symbol	Parameter	Conditions	Ta	T _{amb} = 25 °C					-40 °C 25 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC14	-Q100		<u> </u>							
V _{T+}		V _{CC} = 2.0 V	0.7	1.18	1.5	0.7	1.5	0.7	1.5	V
	threshold voltage	V _{CC} = 4.5 V	1.7	2.38	3.15	1.7	3.15	1.7	3.15	V
		V _{CC} = 6.0 V	2.1	3.14	4.2	2.1	4.2	2.1	4.2	V
V _{T-}	negative-going	V _{CC} = 2.0 V	0.3	0.52	0.9	0.3	0.9	0.3	0.9	V
	threshold voltage	V _{CC} = 4.5 V	0.9	1.4	2.0	0.9	2.0	0.9	2.0	V
		V _{CC} = 6.0 V	1.2	1.89	2.6	1.2	2.6	1.2	2.6	V
V _H	hysteresis voltage	V _{CC} = 2.0 V	0.2	0.66	1.0	0.2	1.0	0.2	1.0	V
		V _{CC} = 4.5 V	0.4	0.98	1.4	0.4	1.4	0.4	1.4	V
		V _{CC} = 6.0 V	0.6	1.25	1.6	0.6	1.6	0.6	1.6	V
74HCT1	4-Q100			'	'	,	'		,	
V _{T+}	positive-going	V _{CC} = 4.5 V	1.2	1.41	1.9	1.2	1.9	1.2	1.9	V
	threshold voltage	V _{CC} = 5.5 V	1.4	1.59	2.1	1.4	2.1	1.4	2.1	V
V _{T-}	negative-going	V _{CC} = 4.5 V	0.5	0.85	1.2	0.5	1.2	0.5	1.2	V
	threshold voltage	V _{CC} = 5.5 V	0.6	0.99	1.4	0.6	1.4	0.6	1.4	V
V _H	hysteresis voltage	V _{CC} = 4.5 V	0.4	0.56	-	0.4	-	0.4	-	V
	-	V _{CC} = 5.5 V	0.4	0.6	-	0.4	-	0.4	-	V

12.1. Transfer characteristics waveforms

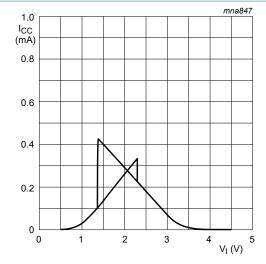




a. $V_{CC} = 2.0 \text{ V}$

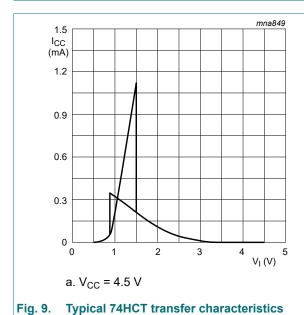


c. $V_{CC} = 6.0 \text{ V}$



b. $V_{CC} = 4.5 \text{ V}$





1.8 mna850
(mA)
1.5
1.2
0.9
0.6
0.3
0
0 1 2 3 4 5 6
V_I (V)

b. $V_{CC} = 5.5 \text{ V}$

13. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

 $P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC}$ where:

- P_{add} = additional power dissipation (μW);
- f_i = input frequency (MHz);
- t_r = rise time (ns); 10 % to 90 %;
- t_f = fall time (ns); 90 % to 10 %;
- ΔI_{CC(AV)} = average additional supply current (μA).

Average $\Delta I_{CC(AV)}$ differs with positive or negative input transitions, as shown in Fig. 10 and Fig. 11.

An example of a relaxation circuit using the 74HC14-Q100; 74HCT14-Q100 is shown in Fig. 12.

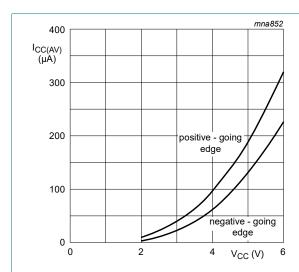


Fig. 10. Average additional supply current as a function of V_{CC} for 74HC14-Q100; linear change of V_I between 0.1V_{CC} to 0.9V_{CC}.

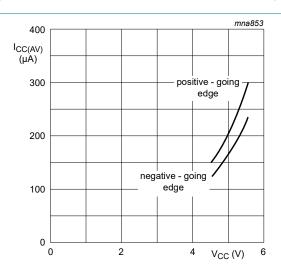
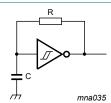


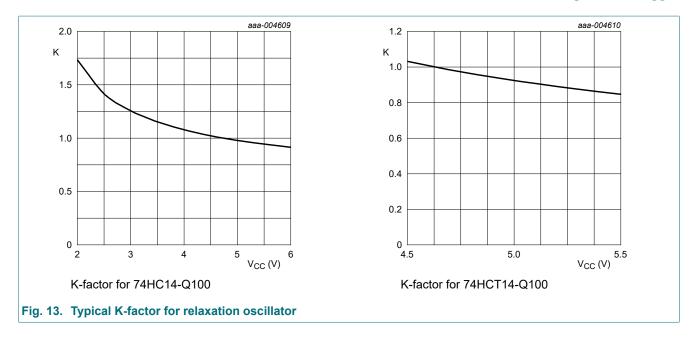
Fig. 11. Average additional supply current as a function of V_{CC} for 74HCT14-Q100; linear change of V_{I} between $0.1V_{CC}$ to $0.9V_{CC}$.



For 74HC14-Q100 and 74HCT14-Q100: $f = \frac{1}{T} \approx \frac{1}{K \times RC}$

For K-factor see Fig. 13

Fig. 12. Relaxation oscillator



14. Package outline

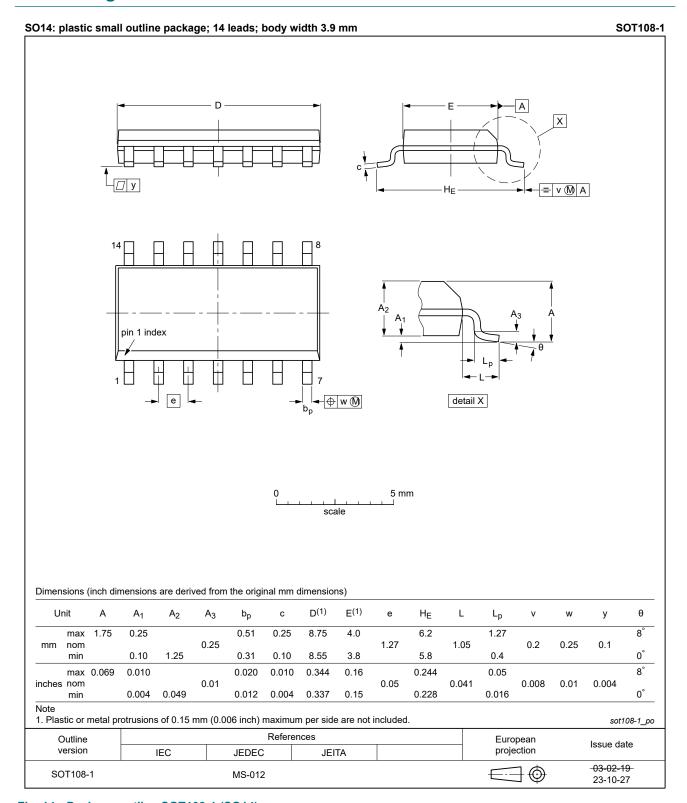


Fig. 14. Package outline SOT108-1 (SO14)

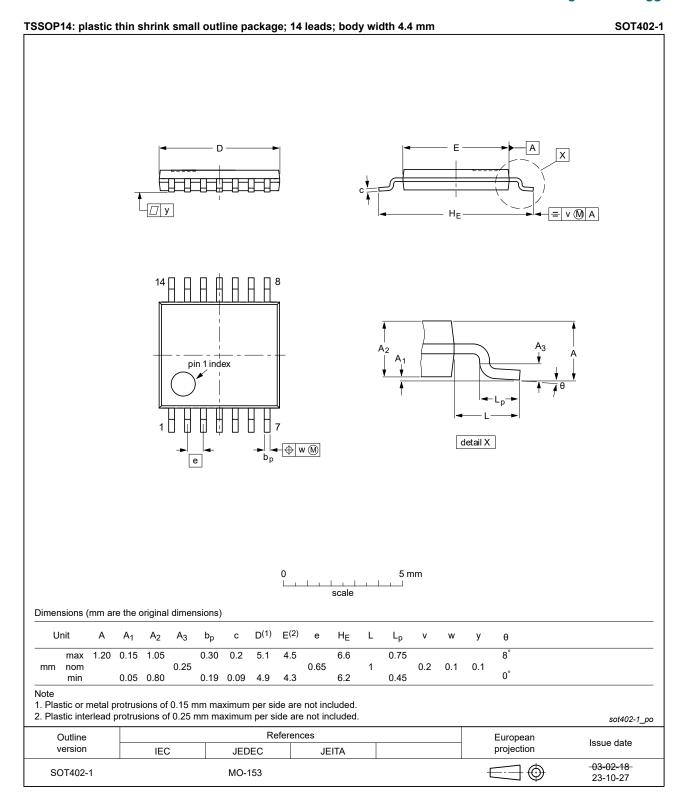


Fig. 15. Package outline SOT402-1 (TSSOP14)

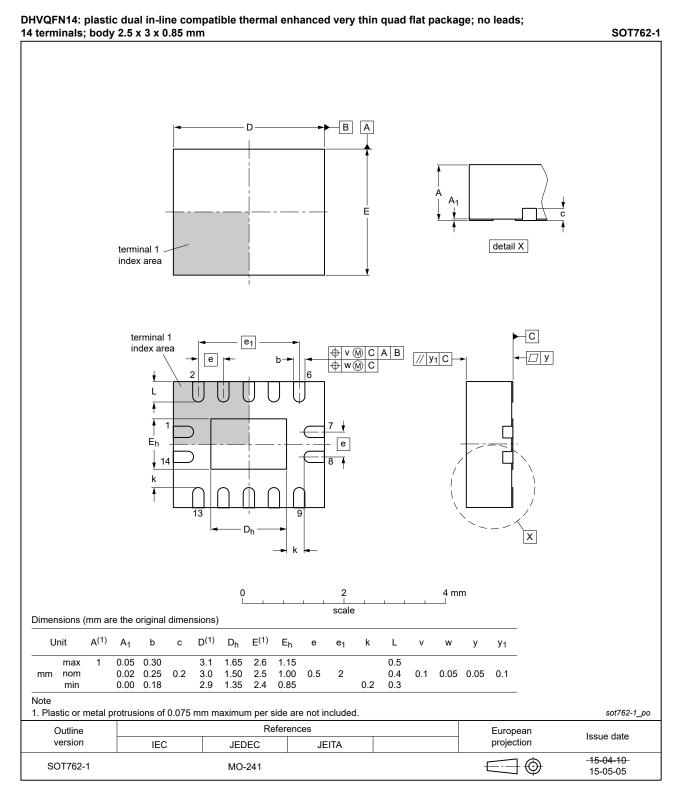


Fig. 16. Package outline SOT762-1 (DHVQFN14)

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
74HC_HCT14_Q100 v.8	20240229	Product data sheet	-	74HC_HCT14_Q100 v.7			
Modifications:		2: ESD specification updated according to the latest JEDEC standard. Fig. 15: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 0-153					
74HC_HCT14_Q100 v.7	20210813	Product data sheet	-	74HC_HCT14_Q100 v.6			
Modifications:	Section 2 up	odated.					
74HC_HCT14_Q100 v.6	20200522	Product data sheet	-	74HC_HCT14_Q100 v.5			
Modifications:	guidelines of Legal texts Section 2 up	have been adapted to the i	new company nar	ne where appropriate.			
74HC_HCT14_Q100 v.5	20151201	Product data sheet	-	74HC_HCT14_Q100 v.4			
Modifications:	Type number	er 74HC14N-Q100 (SOT27	'-1) removed.				
74HC_HCT14_Q100 v.4	20130419	Product data sheet	-	74HC_HCT14_Q100 v.3			
Modifications:	• 74HCT14N-	Q100 removed.					
74HC_HCT14_Q100 v.3	20130410	Product data sheet	-	74HC_HCT14_Q100 v.2			
Modifications:	74HC14N-Q100 and 74HCT14N-Q100 added.						
74HC_HCT14_Q100 v.2	20120810	Product data sheet	-	74HC_HCT14_Q100 v.1			
Modifications:	• <u>Fig. 13</u> adde	Fig. 13 added (typical K-factor for relaxation oscillator).					
74HC_HCT14_Q100 v.1	20120709	Product data sheet	-	-			

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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