74ALVCH16825

18-bit buffer/driver; 3-state

Rev. 4 — 10 July 2024 **Product data sheet**

1. General description

The 74ALVCH16825 is an 18–bit non-inverting buffer/driver with 3-state outputs for bus-oriented applications. The 74ALVCH16825 consists of two 9-bit sections with separate output enable signals. For either 9-bit buffer section, the two output enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be LOW for corresponding nYn outputs to be active. If either output enable input is HIGH, the outputs of that 9-buffer section are in the high impedance state.

The 74ALVCH16825 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range of 1.2 V to 3.6 V
- CMOS low power dissipation
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ± 24 mA at 3.0 V
- Latch-up performance exceeds 250 mA per JESD 78 Class II.A
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD specifications:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH16825DGG	−40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

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4. Functional diagram

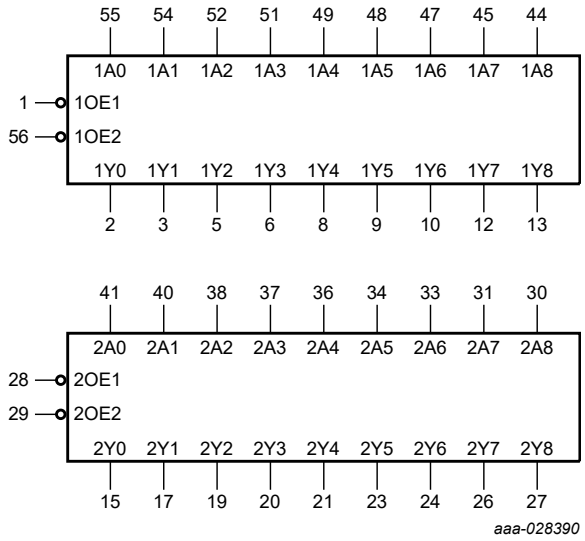

Fig. 1. Logic symbol

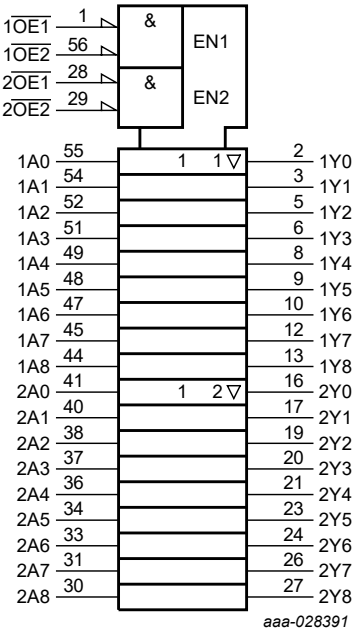

Fig. 2. IEC logic symbol

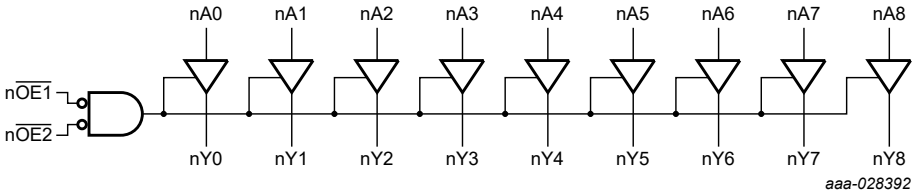

Fig. 3. Logic diagram

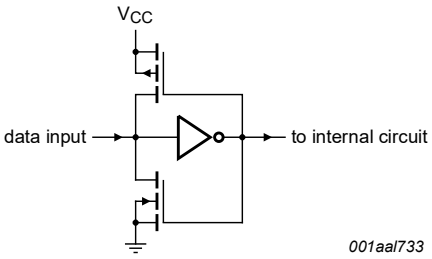

Fig. 4. Bus hold circuit

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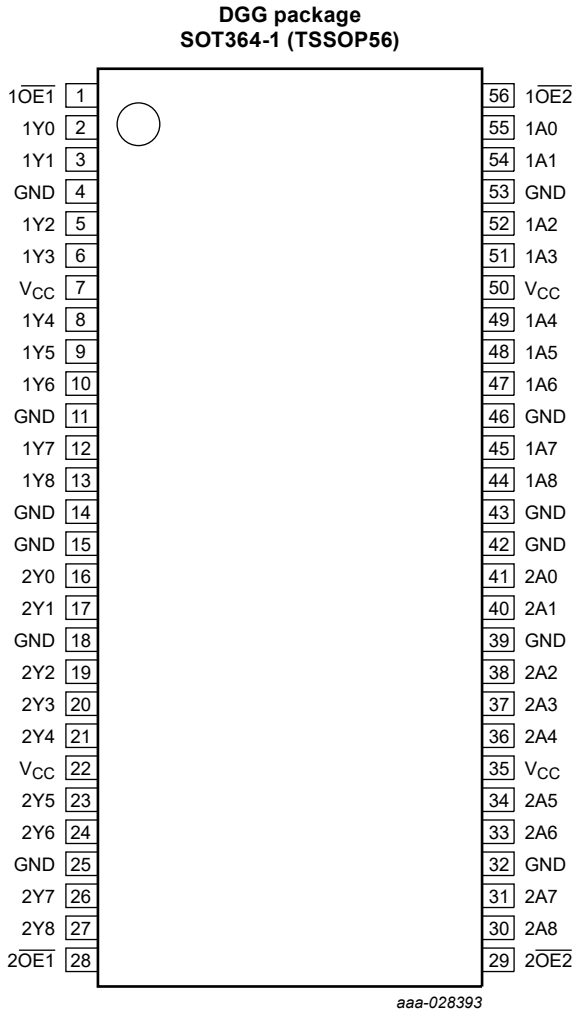
5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8	55, 54, 52, 51, 49, 48, 47, 45, 44	data input
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7, 2A8	41, 40, 38, 37, 36, 34, 33, 31, 30	data input
1Y0, 1Y1, 1Y2, 1Y3, 1Y4, 1Y5, 1Y6, 1Y7, 1Y8	2, 3, 5, 6, 8, 9, 10, 12, 13	data output
2Y0, 2Y1, 2Y2, 2Y3, 2Y4, 2Y5, 2Y6, 2Y7, 2Y8	16, 17, 19, 20, 21, 23, 24, 26, 27	data output
$1\overline{OE1}$, $1\overline{OE2}$, $2\overline{OE1}$, $2\overline{OE2}$	1, 56, 28, 29	output enable input (active-LOW)
GND	4, 11, 14, 15, 18, 25, 32, 39, 42, 43, 46, 53	ground (0 V)
V_{CC}	7, 22, 35, 50	supply voltage

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6. Functional description

Table 3. Function table

X = don't care; Z = High-impedance OFF-state; H = HIGH voltage level; L = LOW voltage level.

Input			Output	Operating mode
$n\overline{OE1}$	$n\overline{OE2}$	nAn	nYn	
L	L	L	L	transparent
L	L	H	H	transparent
H	X	X	Z	High-impedance OFF-state
X	H	X	Z	High-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	data inputs	[1]	-0.5	V_{CC} + 0.5	V
		control inputs	[1]	-0.5	+4.6	V
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
$I_{O\ (sink/source)}$	output sink or source current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +85 °C		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	V_{CC} = 2.5 V: for maximum speed performance at C_L = 30 pF	2.3	2.7	V
		V_{CC} = 3.3 V: for maximum speed performance at C_L = 50 pF	3.0	3.6	V
V_I	input voltage		0	V_{CC}	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature	in free air	−40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	0	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	10	ns/V

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 µA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	V_{CC} - 0.6	V_{CC} - 0.09	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.40	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.70	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	V
I_I	input leakage current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND	-	0.1	5	µA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V	45	-	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V	-45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V	-75	-175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V	-500	-	-	µA
I_{OZ}	OFF-state output current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	0.1	10	µA
I_{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.2	40	µA
ΔI_{CC}	additional supply current	V_{CC}= 2.3 V to 3.6 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	150	750	µA
C_I	input capacitance		-	4.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 7.

Symbol	Parameter	Conditions		-40 °C to +85 °C			Unit
				Min	Typ [1]	Max	
t_{pd}	propagation delay	nAn to nYn; Fig. 5	[2]				
		V_{CC} = 2.3 V to 2.7 V		1.0	2.0	4.1	ns
		V_{CC} = 2.7 V		1.0	2.1	3.9	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.0	3.4	ns
t_{en}	enable time	$n\overline{OE}n$ to nYn; Fig. 6	[2]				
		V_{CC} = 2.3 V to 2.7 V		1.0	2.9	6.0	ns
		V_{CC} = 2.7 V		1.0	2.9	5.7	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.8	4.7	ns
t_{dis}	disable time	$n\overline{OE}n$ to nYn; Fig. 6	[2]				
		V_{CC} = 2.3 V to 2.7 V		1.2	2.2	5.6	ns
		V_{CC} = 2.7 V		1.3	3.0	4.9	ns
		V_{CC} = 3.0 V to 3.6 V		1.3	2.9	4.5	ns
C_{PD}	power dissipation capacitance	per latch; V_I = GND to V_{CC}	[3]				
		outputs enabled		-	19	-	pF
		outputs disabled		-	3	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

[2] t_{pd} is the same as t_{PHL} and t_{PLH};
t_{en} is the same as t_{PZH} and t_{PZL};
t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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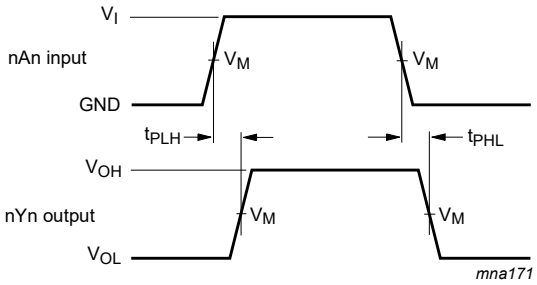
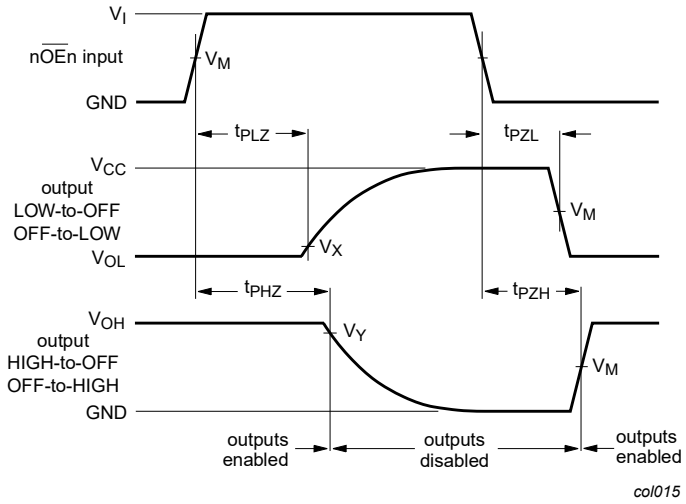
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Input nAn to output nYn propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V

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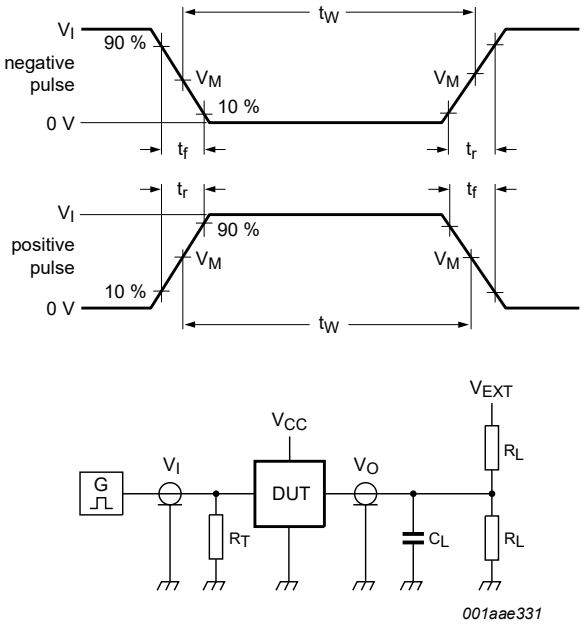

Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

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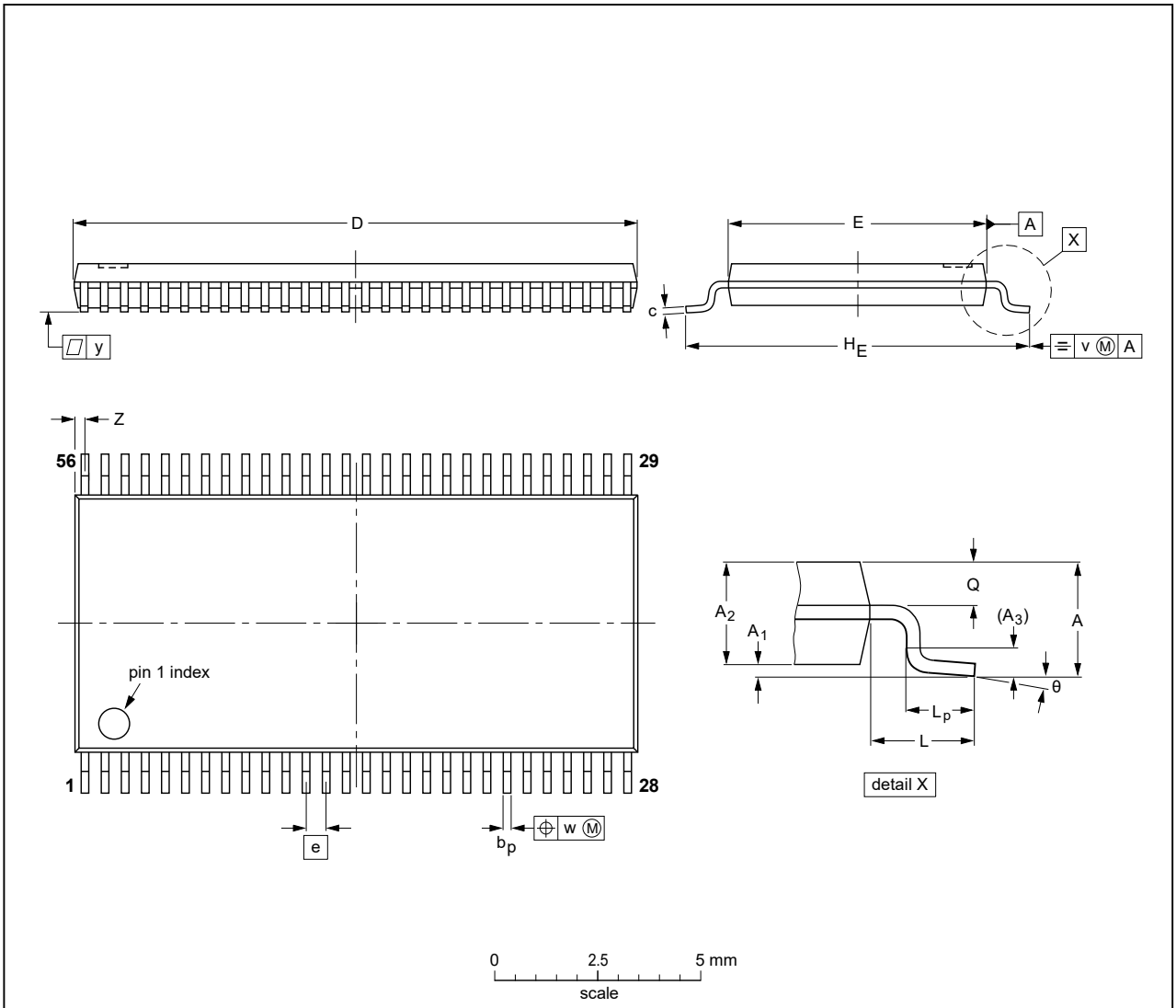
11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT364-1 (TSSOP56)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16825 v.4	20240710	Product data sheet	-	74ALVCH16825 v.3
Modifications:	• Section 1 and Section 2 updated. • Section 2: ESD specification updated according to the latest JEDEC standard. • Table 4: P_{tot} total power dissipation updated.			
74ALVCH16825 v.3	20180406	Product data sheet	-	74ALVCH16825 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ALVCH16825 v.2	19980727	Product specification	-	74ALVCH16825 v.1
74ALVCH16825 v.1	19980727	Product specification	-	-

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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