**Product data sheet** 

# 1. General description

The 74HC540; 74HCT540 is an 8-bit inverting buffer/line driver with 3-state outputs. The device features two output enables ( $\overline{\text{OE}}1$  and  $\overline{\text{OE}}2$ ). A HIGH on  $\overline{\text{OE}}$ n causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

#### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- · High noise immunity
- · Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Inverting outputs
- · Input levels:
  - For 74HC540: CMOS level
  - For 74HCT540: TTL level
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- · ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- · Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

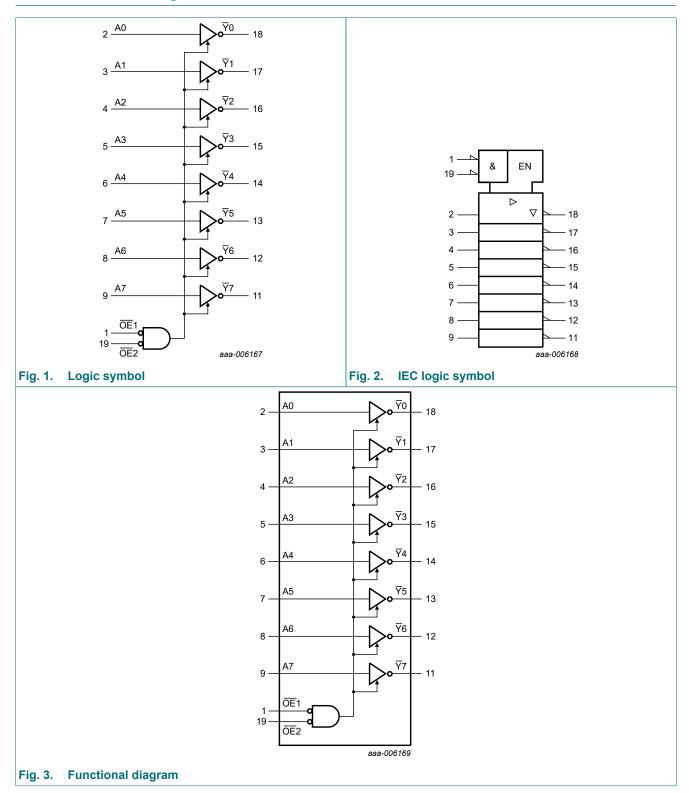
# 3. Ordering information

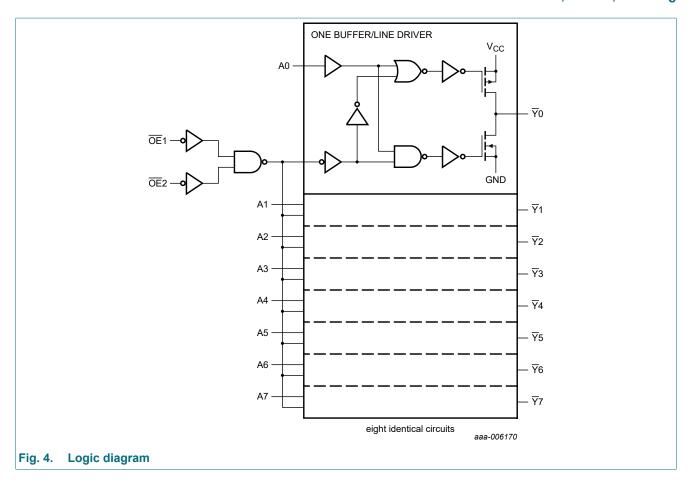
#### **Table 1. Ordering information**

Type number	number Package								
	Temperature range	Name	Description	Version					
74HC540D 74HCT540D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1					
74HC540DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1					
74HC540PW 74HCT540PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1					



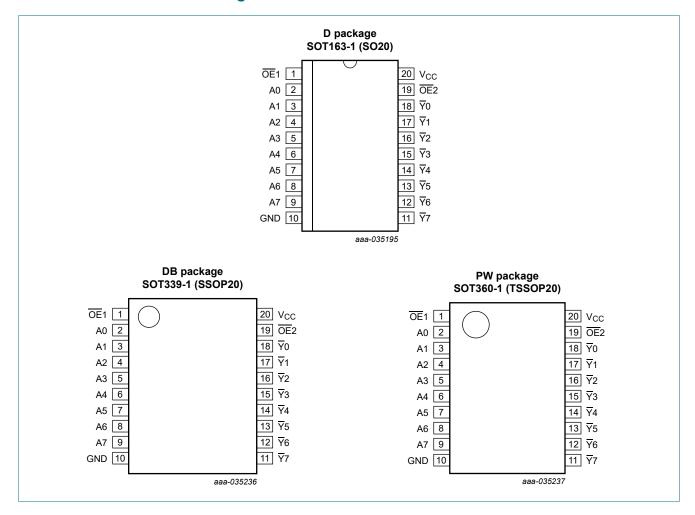
# 4. Functional diagram





# 5. Pinning information

## 5.1. Pinning



## 5.2. Pin description

**Table 2. Pin description** 

Symbol	Pin	Description
OE1, OE2	1, 19	output enable input (active LOW)
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
70, 71, 72, 73, 74, 75, 76, 77	18, 17, 16, 15, 14, 13, 12, 11	data output
V <sub>CC</sub>	20	supply voltage

# 6. Functional description

#### **Table 3. Functional table**

 $H = HIGH \text{ voltage level}; L = LOW \text{ voltage level}; X = don't care; Z = high-impedance OFF-state.}$ 

Control		Input	Output
OE1	OE2	An	Yn
L	L	L	Н
L	L	Н	L
X	Н	X	Z
Н	X	X	Z

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±35	mA
I <sub>CC</sub>	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	[2]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT339-1 (SSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.

For SOT360-1 (TSSOP20) package: Ptot derates linearly with 10.0 mW/K above 100 °C.

# 8. Recommended operating conditions

## Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC540	)	7	Unit		
			Min	Min Typ		Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

<sup>[2]</sup> For SOT163-1 (SO20) package: Ptot derates linearly with 12.3 mW/K above 109 °C.

# 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	Unit	
			Min	Тур	Max	Min	Max	Min	Max	1
74HC54	0							1	'	
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O}$ = -20 $\mu$ A; $V_{CC}$ = 6.0 $V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_{O}$ = -6.0 mA; $V_{CC}$ = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_{O}$ = 20 $\mu$ A; $V_{CC}$ = 2.0 $V$	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		$I_{O}$ = 7.8 mA; $V_{CC}$ = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 6.0 \text{ V}$ ; $V_O = V_{CC}$ or GND	-	±0.5	-	±5.0	-	±10	-	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT5</b>	40							1	'	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	Ι <sub>O</sub> = -20 μΑ	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -6.0 mA	3.98	4.32	-	3.84	-	3.7	-	٧
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 20 μA;	-	0	0.1	-	0.1	-	0.1	٧
		I <sub>O</sub> = 6.0 mA;	-	0.16	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
Iı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μA
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5 V$ ; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; $I_O = 0$ A; $V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V								
		An input	-	140	504	-	630	-	686	μΑ
		OE1 input	-	150	540	-	675	-	735	μA
		OE2 input	-	100	360	-	450	-	490	μΑ
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

# 10. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

GND = 0 V;  $C_L$  = 50 pF; for test circuit see Fig. 7.

Symbol	Parameter	Conditions		2	25 °C		-40 °C to 85 °C	-40 °C to +125 °C	Unit
			М	in	Тур	Max	Max	Max	
74HC54	0								
t <sub>pd</sub>	propagation	An to Yn; see Fig. 5	[1]						
	delay	V <sub>CC</sub> = 2.0 V	-		30	100	125	150	ns
		V <sub>CC</sub> = 4.5 V	-		11	20	25	30	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-		9	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-		9	17	21	26	ns
t <sub>en</sub>	enable time	OEn to Yn; see Fig. 6	[1]						
		V <sub>CC</sub> = 2.0 V	-		52	160	200	240	ns
		V <sub>CC</sub> = 4.5 V	-		19	32	40	48	ns
		V <sub>CC</sub> = 6.0 V	-		15	27	34	41	ns
t <sub>dis</sub>	disable time	OEn to Yn; see Fig. 6	[1]						
		V <sub>CC</sub> = 2.0 V	-		61	160	200	240	ns
		V <sub>CC</sub> = 4.5 V	-		22	32	40	48	ns
		V <sub>CC</sub> = 6.0 V	-		18	27	34	41	ns
t <sub>t</sub>	transition time	see Fig. 5	[2]						
		V <sub>CC</sub> = 2.0 V	-		14	60	75	90	ns
		V <sub>CC</sub> = 4.5 V	-		5	12	15	18	ns
		V <sub>CC</sub> = 6.0 V	-		4	10	13	15	ns
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub>	[3]		39	-	-	-	pF

Symbol	Parameter	Conditions		25 °C	;	-40 °C to 85 °C	-40 °C to +125 °C	Unit
			Mi	1 Тур	Max	Max	Max	
<b>74HCT5</b>	40		'					
t <sub>pd</sub>	propagation	An to Yn; see Fig. 5	]					
	delay	V <sub>CC</sub> = 4.5 V	-	13	24	30	36	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	11	-	-	-	ns
t <sub>en</sub>	enable time	OEn to Yn; see Fig. 6	]					
		V <sub>CC</sub> = 4.5 V	-	22	35	44	53	ns
t <sub>dis</sub>	disable time	OEn to Yn; see Fig. 6	]					
		V <sub>CC</sub> = 4.5 V	-	23	35	44	53	ns
t <sub>t</sub>	transition time	$V_{CC} = 4.5 \text{ V}; \text{ see } \frac{\text{Fig. 5}}{}$	2] -	5	12	15	18	ns
C <sub>PD</sub>	power dissipation capacitance	per package; [3 V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	-	44	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

 $t_{\text{en}}$  is the same as  $t_{\text{PZL}}$  and  $t_{\text{PZH}}.$ 

 $t_{\text{dis}}$  is the same as  $t_{\text{PLZ}}$  and  $t_{\text{PHZ}}.$ 

- t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
   C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):
   P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_0)$$
 where

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

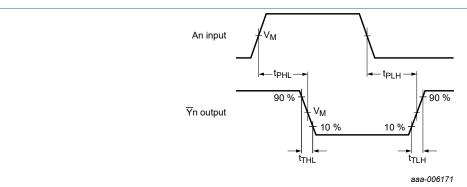
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$ 

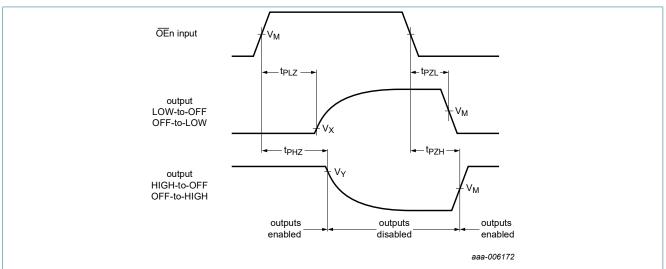
### 10.1. Waveforms and test circuit



Measurement points are given in <u>Table 8</u>.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig. 5. Input to output propagation delays



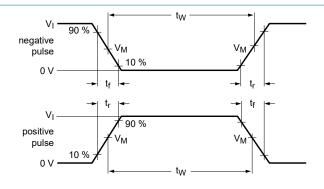
Measurement points are given in <u>Table 8</u>.

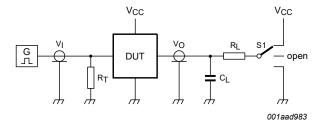
 $\ensuremath{V_{\text{OL}}}$  and  $\ensuremath{V_{\text{OH}}}$  are typical voltage output levels that occur with the output load.

Fig. 6. 3-state enable and disable times

**Table 8. Measurement points** 

Туре	Input	Output	Output							
	$V_{M}$	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>						
74HC540	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>						
74HCT540	1.3 V	1.3 V	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>						





Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

R<sub>L</sub> = Load resistance;

S1 = Test selection switch.

#### Fig. 7. Test circuit for measuring switching times

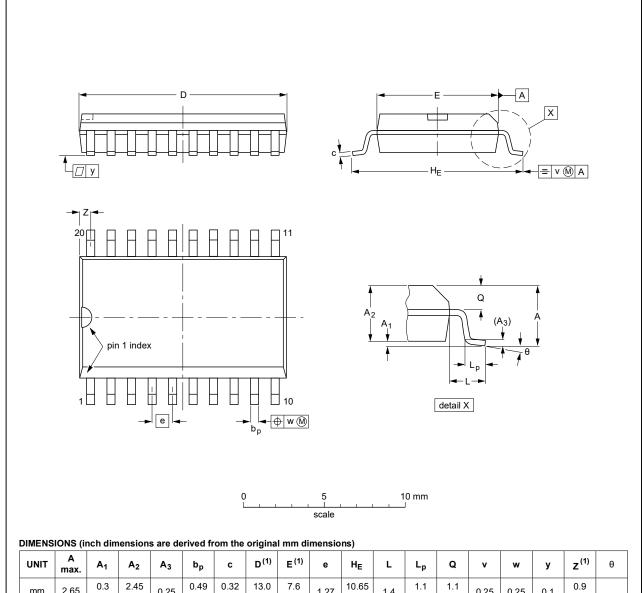
Table 9. Test data

Туре	Input		Load		S1 position				
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>		
74HC540	V <sub>CC</sub>	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>		
74HCT540	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>		

# 11. Package outline

#### SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

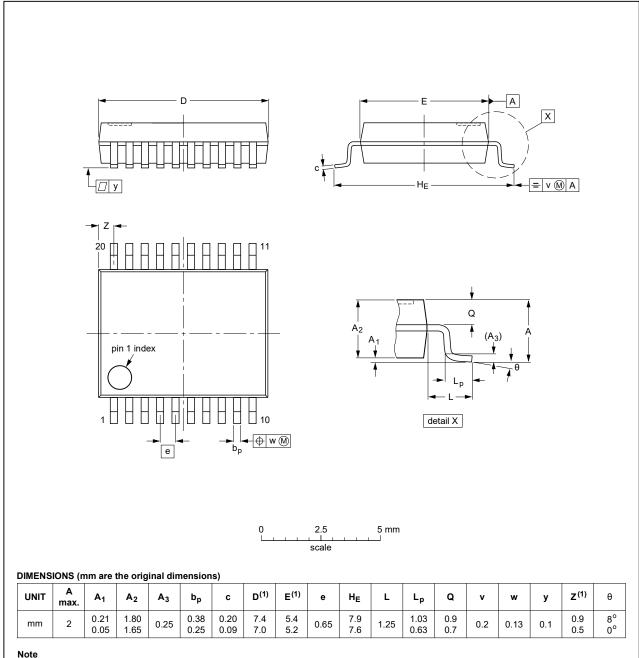
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013				<del>99-12-27</del> 03-02-19

Package outline SOT163-1 (SO20)

#### SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



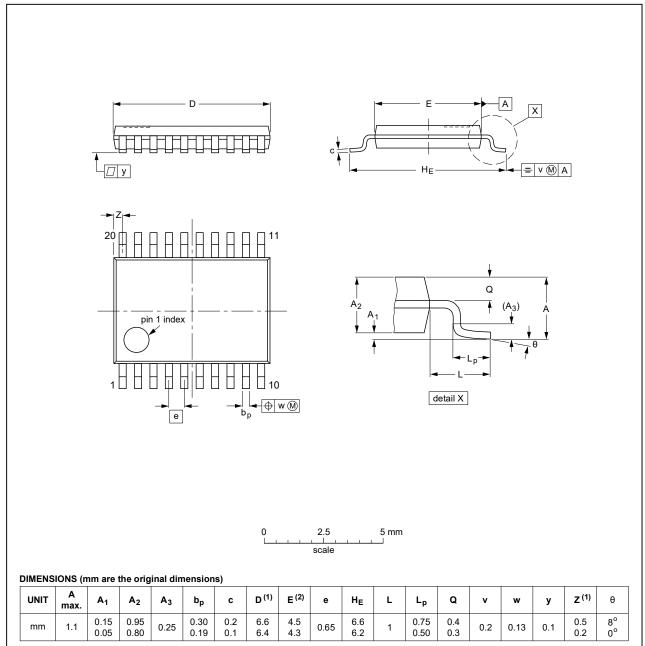
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT339-1		MO-150				<del>99-12-27</del> 03-02-19

Package outline SOT339-1 (SSOP20)

#### TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFERENCES				EUROPEAN	ISSUE DATE
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT360-1		MO-153				<del>-99-12-27</del> 03-02-19

Fig. 10. Package outline SOT360-1 (TSSOP20)

# 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
НВМ	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

# 13. Revision history

### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes			
74HC_HCT540 v.8	20240805	Product data sheet	-	74HC_HCT540 v.7			
Modifications:	Section 2: E	Section 2: ESD specification updated according to the latest JEDEC standard.					
74HC_HCT540 v.7	20240507	Product data sheet	-	74HC_HCT540 v.6			
Modifications:	Type number	er 74HCT540DB (SOT339-	-1/SSOP20) remo	ved.			
74HC_HCT540 v.6	20211019	Product data sheet	-	74HC_HCT540 v.5			
Modifications:	Type number	er 74HCT540PW (SOT360	-1/TSSOP20) add	ded.			
74HC_HCT540 v.5	20210816	Product data sheet	-	74HC_HCT540 v.4			
	<ul><li>Legal texts</li><li>Type number</li><li>Section 2 up</li></ul>	• Type number 74HC540PW (SOT360-1/TSSOP20) added.					
74HC_HCT540 v.4	20160301	Product data sheet	-	74HC_HCT540 v.3			
Modifications:	Type number	Type numbers 74HC540N and 74HCT540N (SOT146-1) removed.					
74HC_HCT540 v.3	20130121	Product data sheet	-	74HC_HCT540_CNV v.2			
Modifications:	guidelines o	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>					
74HC_HCT540_CNV v.2	19970905	Product specification	-	-			

# 14. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <a href="https://www.nexperia.com">https://www.nexperia.com</a>.

#### **Definitions**

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