74CBTLV3125

4-bit bus switch

Rev. 7 — 11 April 2024 Product data sheet

1. General description

The 74CBTLV3125 provides a 4-bit high-speed bus switch with separate output enable inputs (1$\overline{OE}$ to 4$\overline{OE}$). The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The switch is disabled (high-impedance OFF-state) when the output enable (n$\overline{OE}$) input is HIGH.

To ensure the high-impedance OFF-state during power-up or power-down, n$\overline{OE}$ should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLV3125DS	-40 °C to +125 °C	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
74CBTLV3125PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74CBTLV3125BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

[1] Also known as QSOP16.

4. Functional diagram

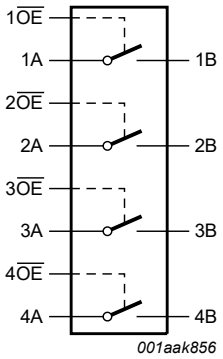


Fig. 1. Logic symbol

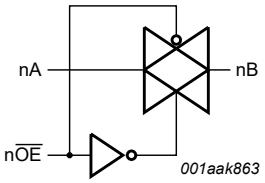


Fig. 2. Logic diagram (one switch)

5. Pinning information

5.1. Pinning

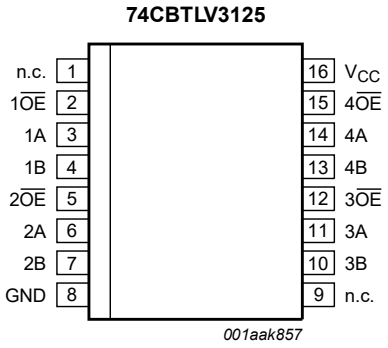


Fig. 3. Pin configuration SOT519-1 (SSOP16)

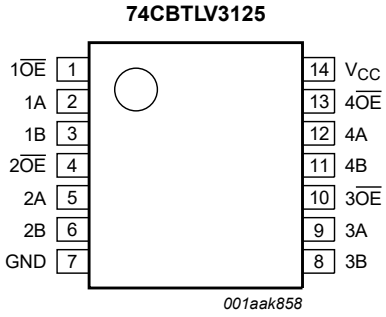
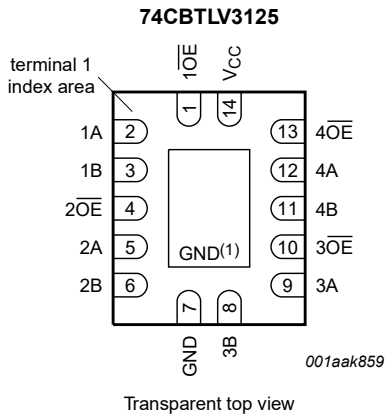


Fig. 4. Pin configuration SOT402-1 (TSSOP14)



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT519-1	SOT402-1 and SOT762-1	
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	2, 5, 12, 15	1, 4, 10, 13	output enable input
1A, 2A, 3A, 4A,	3, 6, 11, 14	2, 5, 9, 12	A input/output
1B, 2B, 3B, 4B	4, 7, 10, 13	3, 6, 8, 11	B output/input
GND	8	7	ground (0 V)
V_{CC}	16	14	positive supply voltage
n.c.	1, 9	-	not connected

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Output enable input $\overline{OE}$	Function switch
L	ON-state
H	OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	control inputs	[1]	-0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode	[2]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < -0.5 V		-50	-	mA
I_{SK}	switch clamping current	V_I < -0.5 V		-50	-	mA
I_{SW}	switch current	V_{SW} = 0 V to V_{CC}		-	±128	mA
I_{CC}	supply current			-	+100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.
[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed
[3] For SOT519-1 (SSOP16) packages: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage	control inputs	0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	pin n$\overline{OE}$; V_{CC} = 2.3 V to 3.6 V	0	200	ns/V

9. Static characteristics

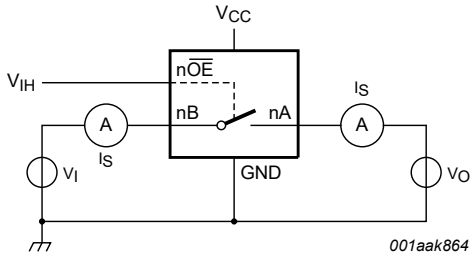
Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I_I	input leakage current	pin $n\overline{OE}$; V_I = GND to V_{CC}; V_{CC} = 3.6 V	-	-	±1.0	-	±20	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 3.6 V; see Fig. 6	-	-	±1	-	±20	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 3.6 V; see Fig. 7	-	-	±1	-	±20	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±10	-	±50	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{SW} = GND or V_{CC}; V_{CC} = 3.6 V	-	-	10	-	50	µA
ΔI_{CC}	additional supply current	pin $n\overline{OE}$; V_I = V_{CC} - 0.6 V; [2] V_{SW} = GND or V_{CC}; V_{CC} = 3.6 V	-	-	300	-	2000	µA
C_I	input capacitance	pin $n\overline{OE}$; V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	0.9	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	5.2	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	14.3	-	-	-	pF

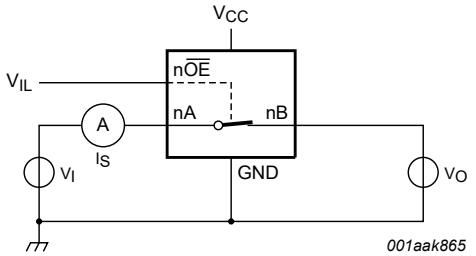
[1] All typical values are measured at T_{amb} = 25 °C.
[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1. Test circuits



V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Fig. 6. Test circuit for measuring OFF-state leakage current (one switch)



V_I = V_{CC} or GND and V_O = open circuit.

Fig. 7. Test circuit for measuring ON-state leakage current (one switch)

9.2. ON resistance

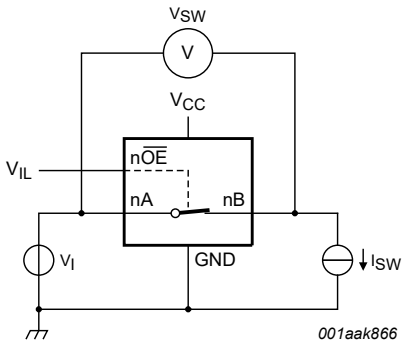
Table 7. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
R_{ON}	ON resistance	V_{CC} = 2.3 V to 2.7 V; see Fig. 9 to Fig. 11 [2]						
		I_{SW} = 64 mA; V_I = 0 V	-	4.2	8.0	-	15.0	Ω
		I_{SW} = 24 mA; V_I = 0 V	-	4.2	8.0	-	15.0	Ω
		I_{SW} = 15 mA; V_I = 1.7 V	-	8.4	40.0	-	60.0	Ω
		V_{CC} = 3.0 V to 3.6 V; see Fig. 12 to Fig. 14						
		I_{SW} = 64 mA; V_I = 0 V	-	4.0	7.0	-	11.0	Ω
		I_{SW} = 24 mA; V_I = 0 V	-	4.0	7.0	-	11.0	Ω
		I_{SW} = 15 mA; V_I = 2.4 V	-	6.2	15.0	-	25.5	Ω

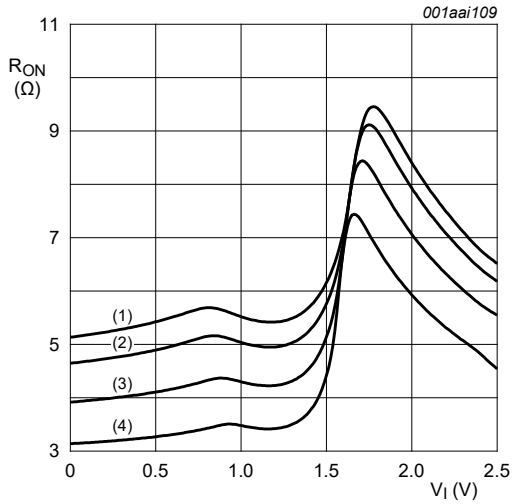
[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.3. ON resistance test circuit and graphs



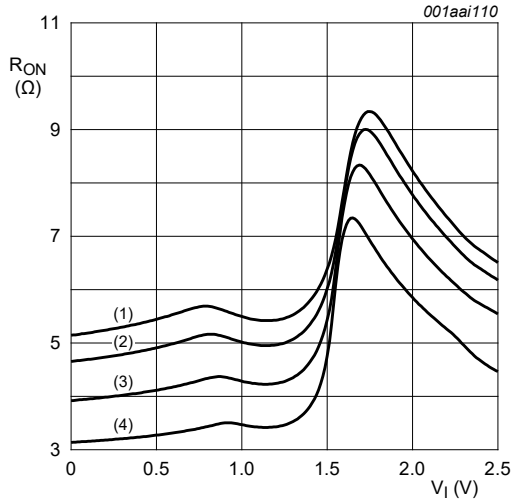
$R_{ON} = V_{SW} / I_{SW}$

Fig. 8. Test circuit for measuring ON resistance (one switch)



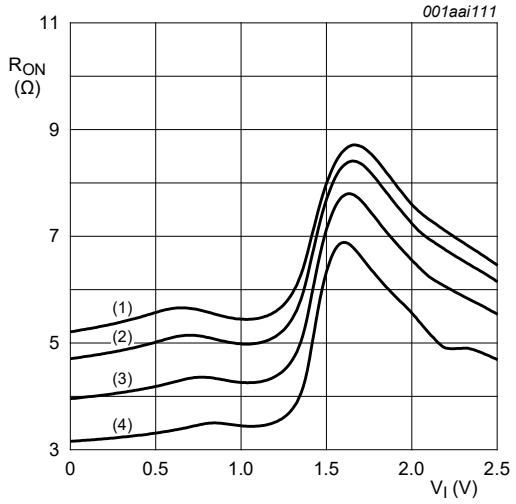
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 9. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 15 mA



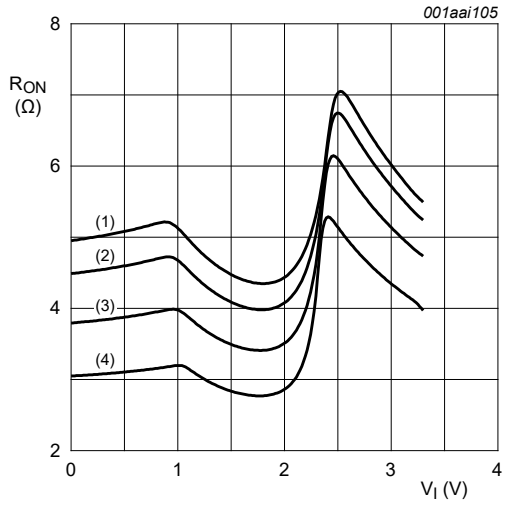
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 10. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 24 mA



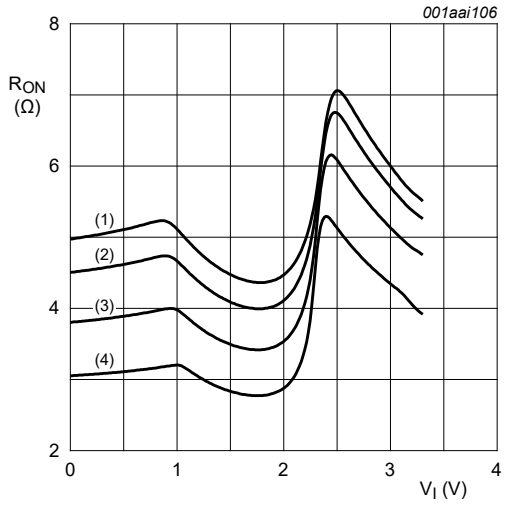
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 11. ON resistance as a function of input voltage; V_{CC} = 2.5 V; I_{SW} = 64 mA



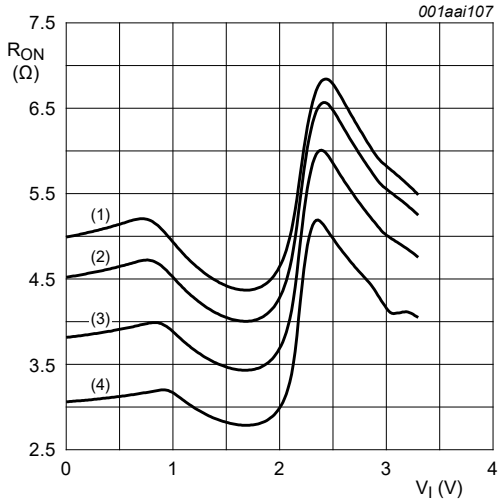
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 12. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 15 mA



(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 13. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 24 mA



(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 14. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 64 mA

10. Dynamic characteristics

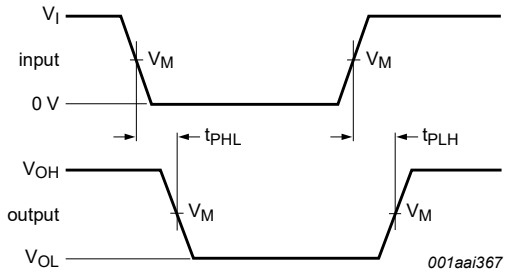
Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 17

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nB or nB to nA; see Fig. 15 [2] [3]						
		V_{CC} = 2.3 V to 2.7 V	-	-	0.13	-	0.20	ns
		V_{CC} = 3.0 V to 3.6 V	-	-	0.20	-	0.31	ns
t_{en}	enable time	$n\overline{OE}$ to nA or nB; see Fig. 16 [4]						
		V_{CC} = 2.3 V to 2.7 V	1.0	2.7	4.6	1.0	6.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.4	4.4	1.0	6.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nA or nB; see Fig. 16 [5]						
		V_{CC} = 2.3 V to 2.7 V	1.0	2.2	3.9	1.0	5.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.9	4.2	1.0	5.5	ns

[1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.
[2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
[3] t_{pd} is the same as t_{PLH} and t_{PHL}.
[4] t_{en} is the same as t_{PZH} and t_{PZL}.
[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

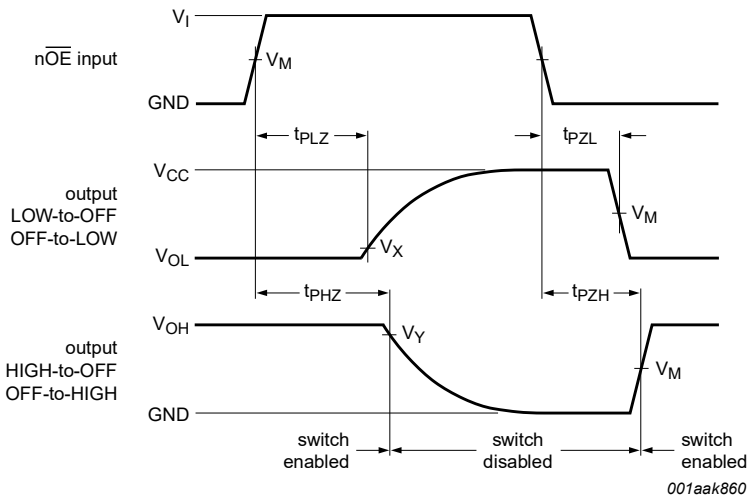
10.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 15. The data input (nA or nB) to output (nB or nA) propagation delays



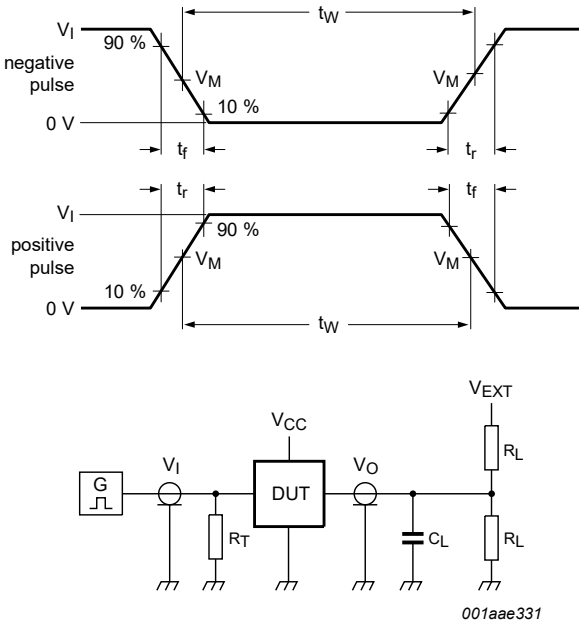
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 16. Enable and disable times

Table 9. Measurement points

Supply voltage	Input			Output		
V_{CC}	V_M	V_I	$t_r = t_f$	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 17. Test circuit for measuring switching times

Table 10. Test data

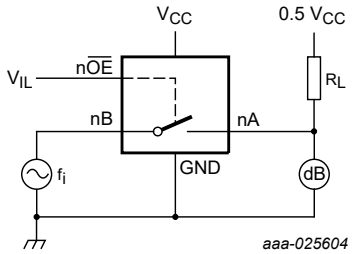
Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	open	GND	$2V_{CC}$
3.0 V to 3.6 V	50 pF	500 Ω	open	GND	$2V_{CC}$

10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
$f_{(-3dB)}$	-3 dB frequency response	V_I = GND or V_{CC}; $t_r = t_f \leq 2.5$ ns; V_{CC} = 3.3 V; R_L = 50 Ω; see Fig. 18	-	406	-	MHz

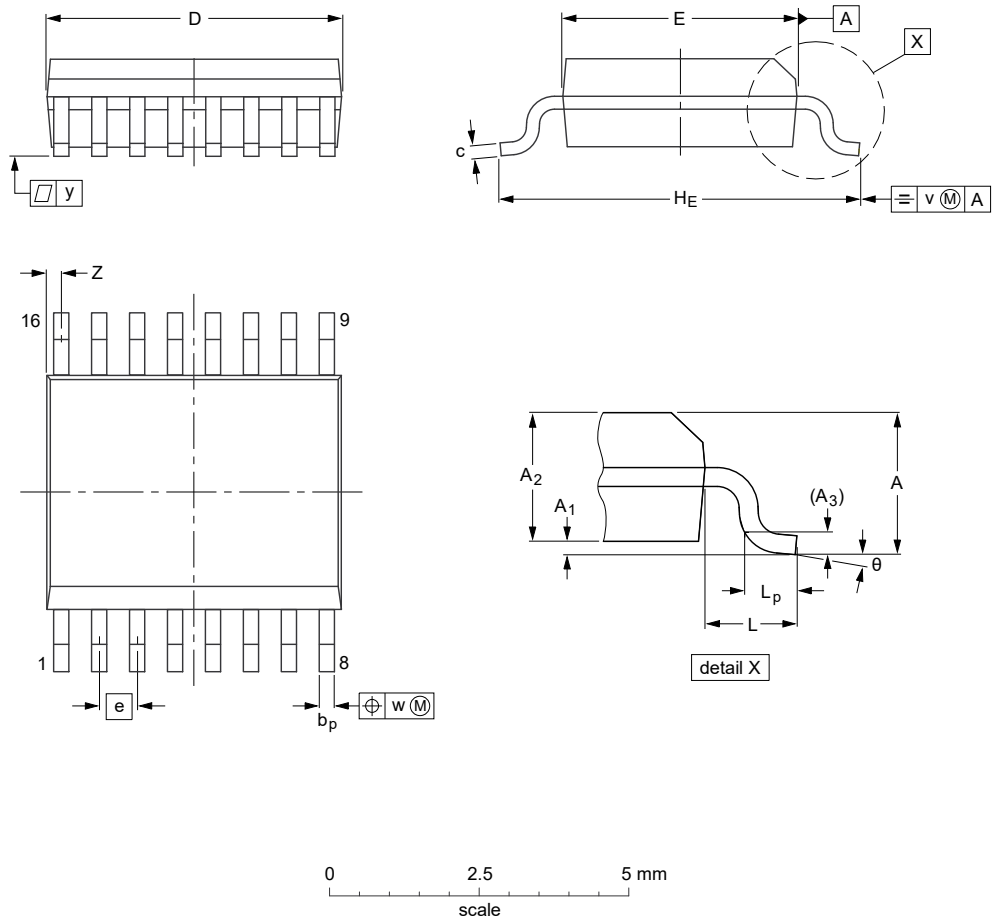


nOE connected to GND; f_i is biased at $0.5V_{CC}$; Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 18. Test circuit for measuring the frequency response when channel is in ON-state

11. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	v	w	y	Z (1)	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8° 0°

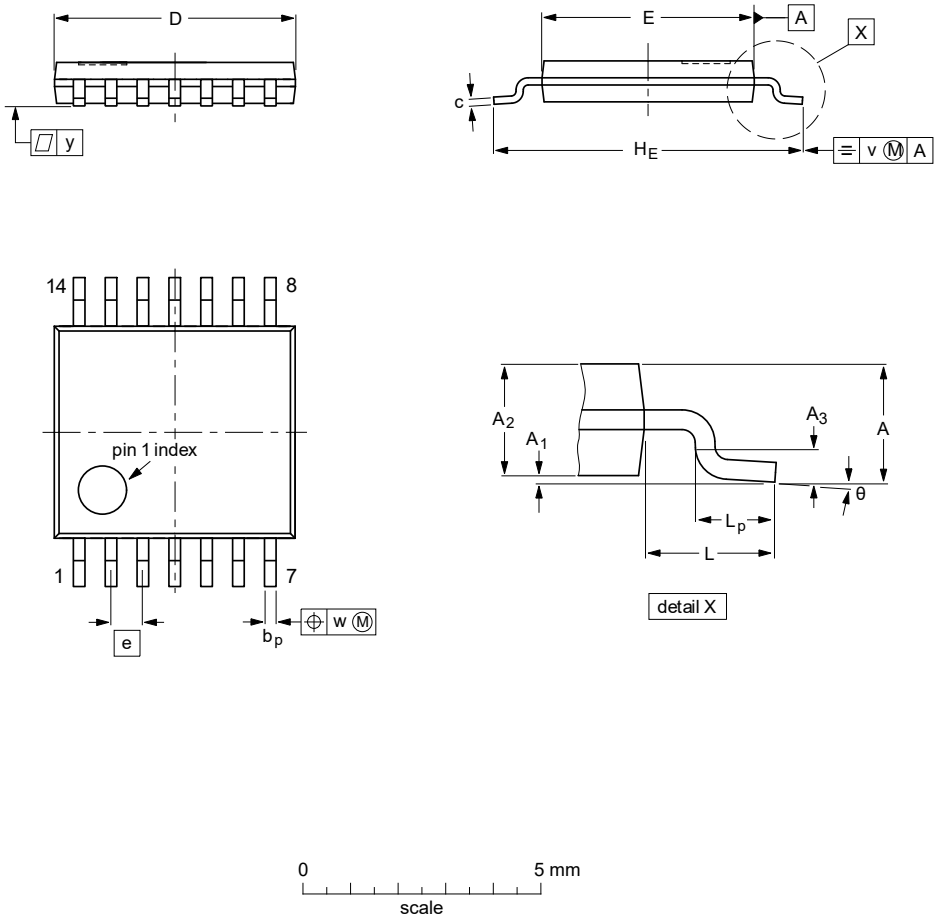
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT519-1						~~99-05-04~~ 03-02-18

Fig. 19. Package outline SOT519-1 (SSOP16)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

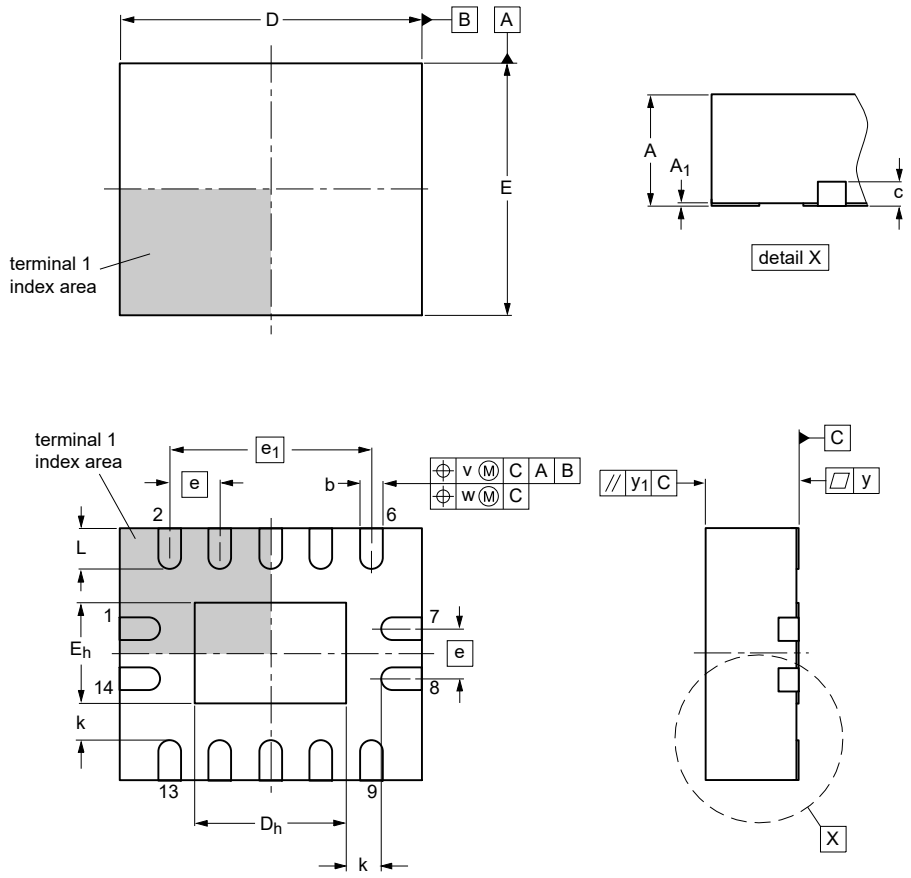
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 20. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	k	L	v	w	y	y1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 21. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3125 v.7	20240411	Product data sheet	-	74CBTLV3125 v.6
Modifications:	• Fig. 20: Aligned TSSOP package outline drawing to JEDEC MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74CBTLV3125 v.6	20200923	Product data sheet	-	74CBTLV3125 v.5
Modifications:	• Table 4: Derating values for P_{tot} total power dissipation updated.			
74CBTLV3125 v.5	20181008	Product data sheet	-	74CBTLV3125 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74CBTLV3125 v.4	20161109	Product data sheet	-	74CBTLV3125 v.3
Modifications:	• Section 10.2 added.			
74CBTLV3125 v.3	20111215	Product data sheet	-	74CBTLV3125 v.2
Modifications:	• Legal pages updated.			
74CBTLV3125 v.2	20110104	Product data sheet	-	74CBTLV3125 v.1
74CBTLV3125 v.1	20100108	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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