



# PSMN7R6-100BSE

N-channel 100 V 7.6 mΩ standard level MOSFET in D2PAK

18 December 2012

Product data sheet

## 1. General description

Standard level N-channel MOSFET in a D2PAK package qualified to 175 °C. Part of Nexperia's "NextPower Live" portfolio, the PSMN7R6-100BSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, whilst offering a low  $R_{DS(on)}$  characteristic to keep temperatures down and efficiency up in continued use. Ideal for telecommunication systems based on a 48 V backplane / supply rail.

## 2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low  $R_{DS(on)}$  for low conduction losses

## 3. Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$		-	-	100	V
$I_D$	drain current	$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 1</a>	[1]	-	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>		-	-	296	W
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>		-	6.5	7.6	mΩ
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 50\text{ V}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	41	-	nC
$Q_{G(tot)}$	total gate charge			-	128	-	nC

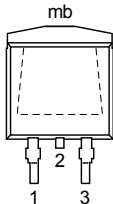
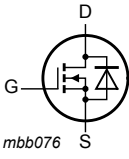
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche Ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 75\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; <a href="#">Fig. 3</a>	-	-	426	mJ

[1] Continuous current limited by package

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>D2PAK (SOT404)</b></p>	 <p>mbb076</p>
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN7R6-100BSE	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN7R6-100BSE	PSMN7R6100BSE

## 8. Limiting values

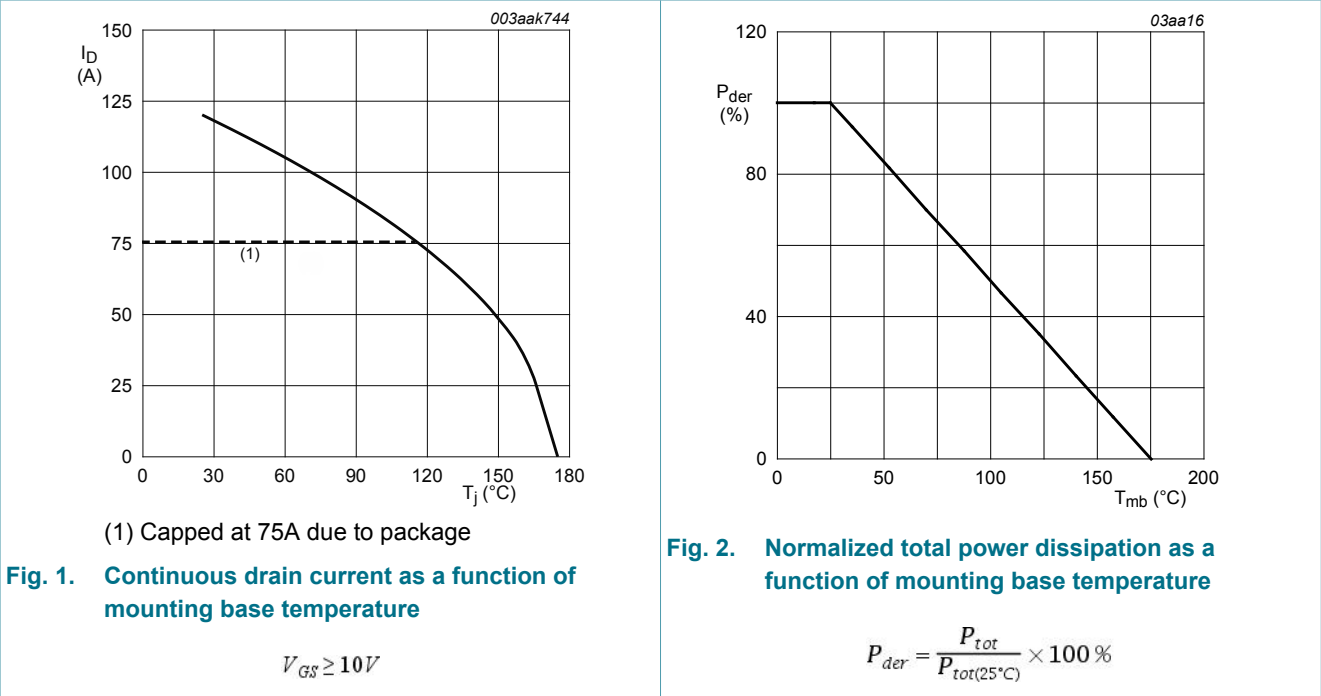
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	100	V

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 1</a>	[1]	-	75	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 1</a>	[1]	-	75	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 4</a>		-	481	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	296	W
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	75	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	481	A
Avalanche Ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 75 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; unclamped; <a href="#">Fig. 3</a>		-	426	mJ

[1] Continuous current limited by package



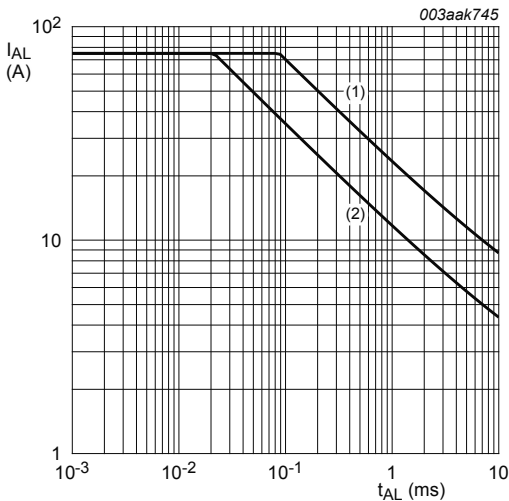


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j(jnt)} = 25^{\circ}C$ ; (2)  $T_{j(jnt)} = 100^{\circ}C$

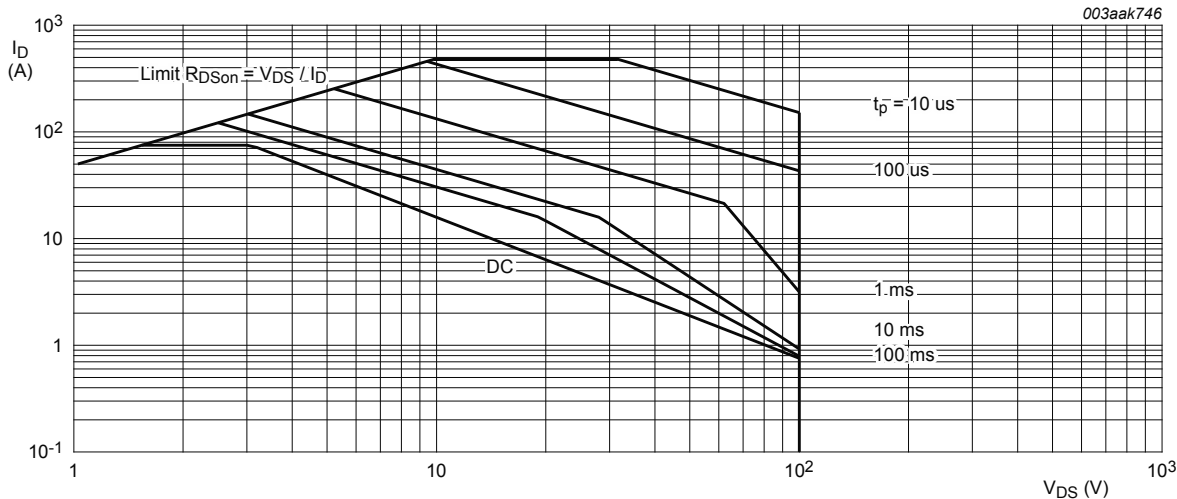


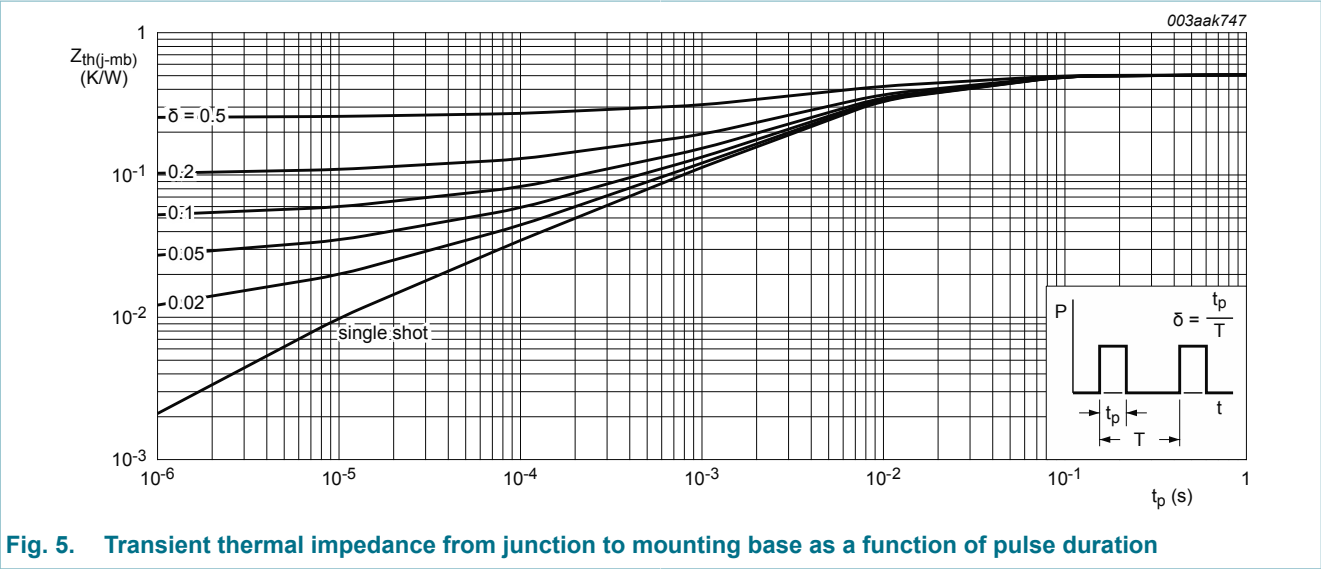
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	0.42	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	100	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -55 °C	90	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 25 °C; Fig. 10; Fig. 11	2	3	4	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 175 °C; Fig. 11	1	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = -55 °C; Fig. 11	-	-	4.6	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	0.1	2	μA
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	10	100	nA
		V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	10	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; Fig. 12	-	6.5	7.6	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 100 °C; Fig. 12; Fig. 13	-	-	13.7	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C; Fig. 12; Fig. 13	-	-	20.5	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz	0.42	0.83	1.66	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	128	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V		-	110	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	33	-	nC
Q <sub>GD</sub>	gate-drain charge			-	41	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	5.3	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>		-	7110	-	pF
C <sub>oss</sub>	output capacitance			-	450	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	310	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; R <sub>L</sub> = 2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω		-	31	-	ns
t <sub>r</sub>	rise time			-	48	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	82	-	ns
t <sub>f</sub>	fall time			-	47	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>		-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V		-	69	-	ns
Q <sub>r</sub>	recovered charge			-	210	-	nC

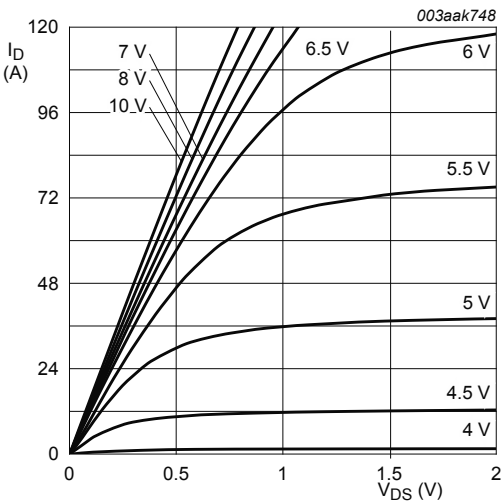


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^{\circ}\text{C}$

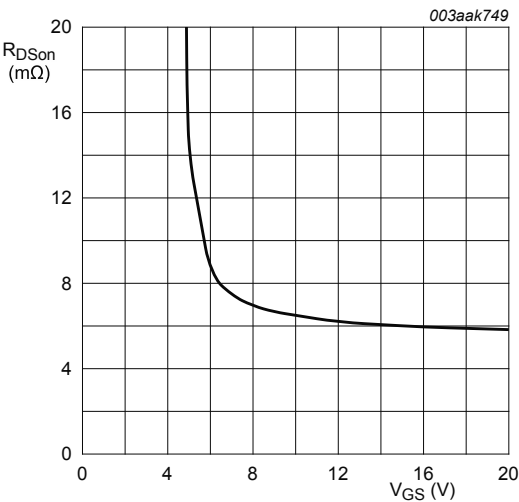


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^{\circ}\text{C}$ ;  $I_D = 25\text{A}$

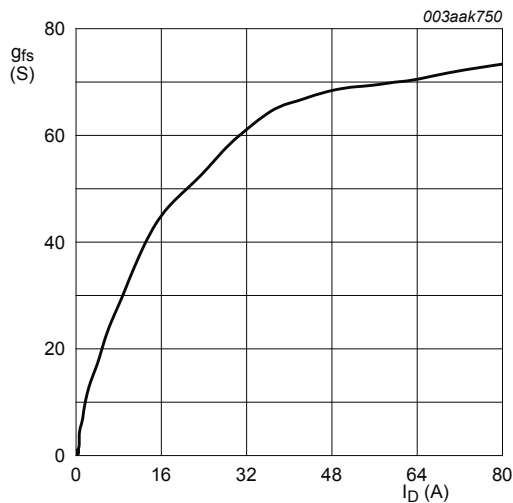


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_J = 25^{\circ}\text{C}; V_{DS} = 10\text{V}$

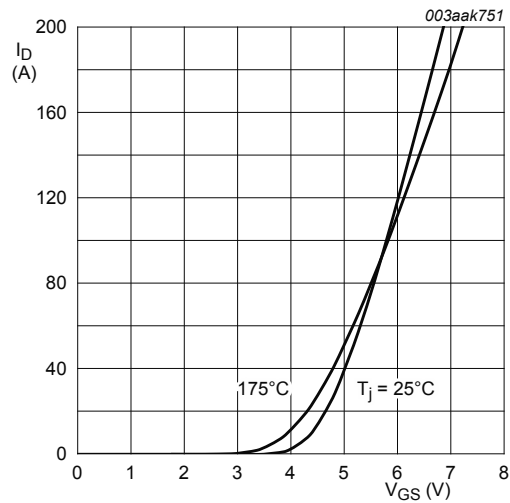


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

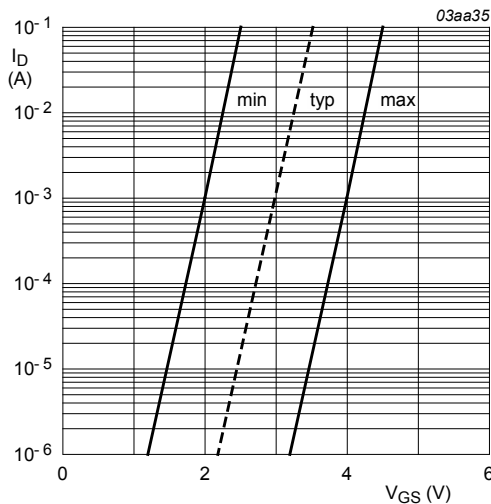


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_J = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

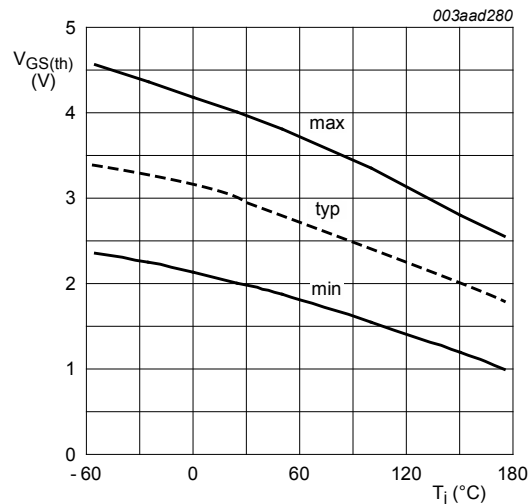


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

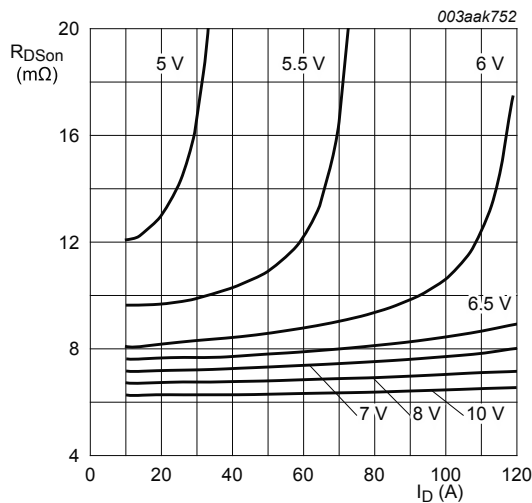


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^{\circ}C$$

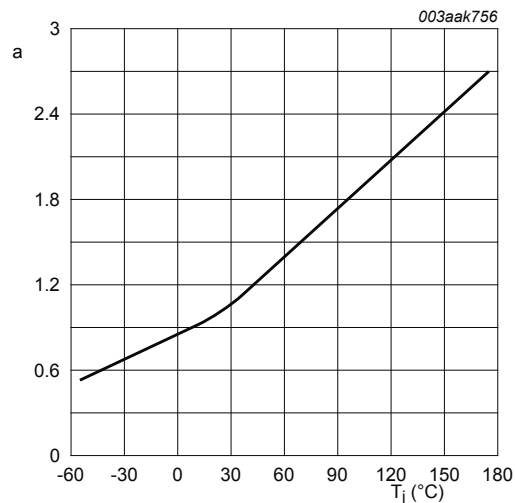


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^{\circ}C)}$$

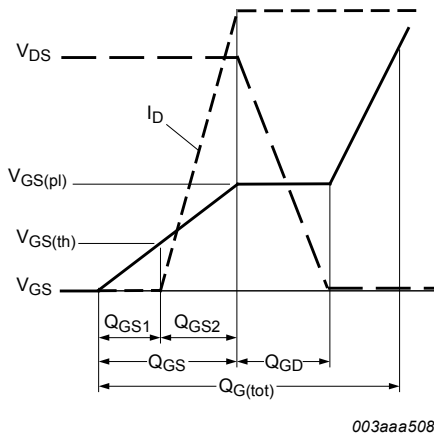


Fig. 14. Gate charge waveform definitions

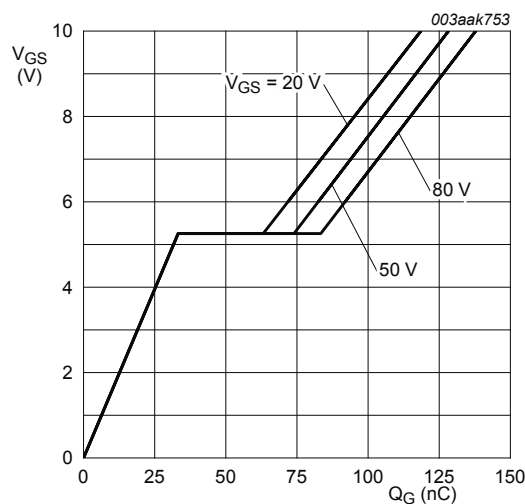


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$



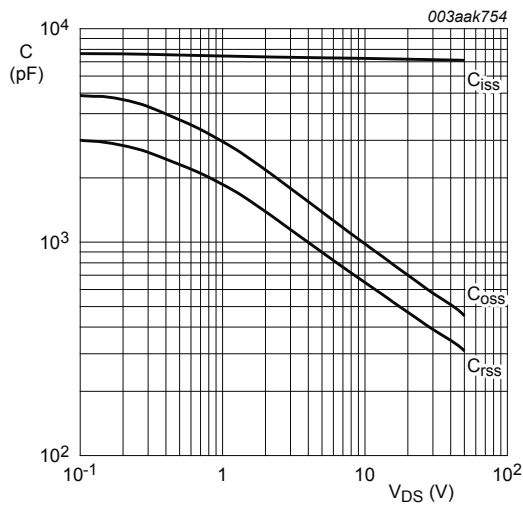


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS}=0V; f=1MHz$

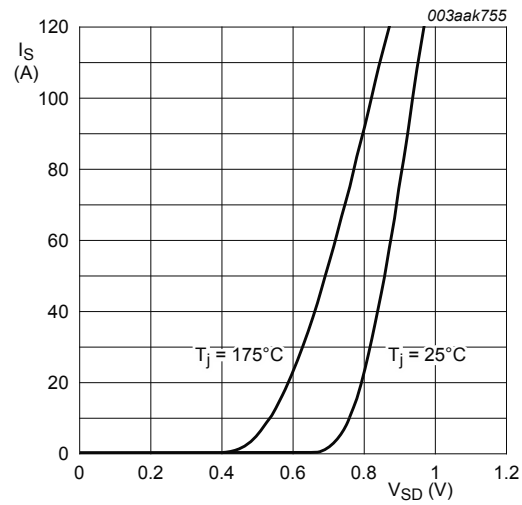


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS}=0V$

11. Package outline

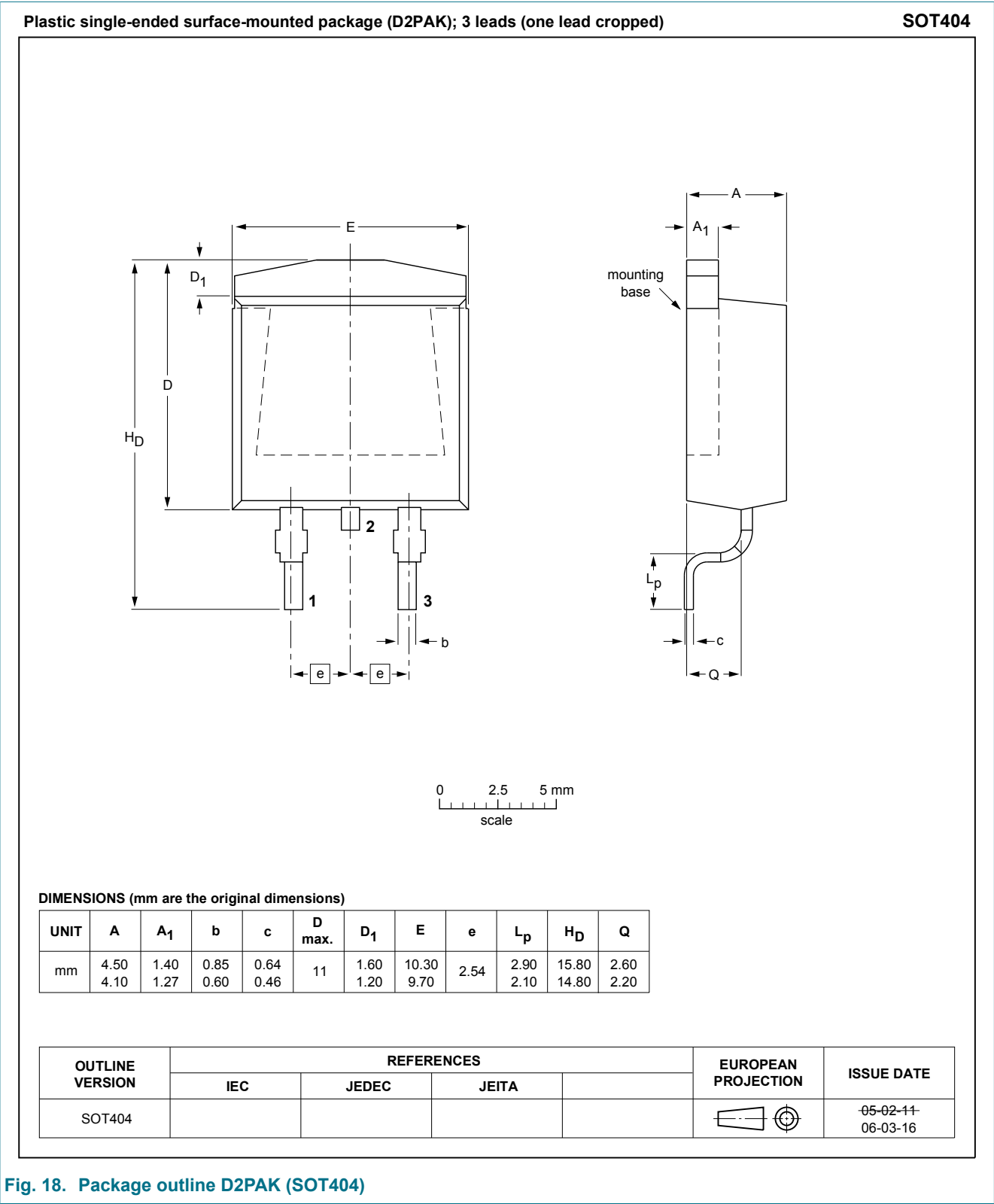


Fig. 18. Package outline D2PAK (SOT404)

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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