



# BUK7K23-80E

Dual N-channel 80 V, 23 mΩ standard level MOSFET

11 May 2018

Product data sheet

## 1. General description

Dual Standard level N-channel MOSFET in an LFPK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- AEC-Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with  $V_{GS(th)}$  rating of greater than 1 V at 175 °C

## 3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

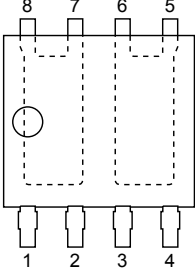
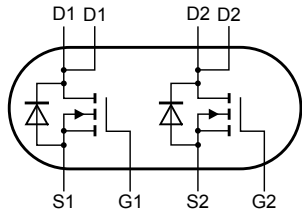
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Limiting values FET1 and FET2</b>						
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	17	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	53	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	17.6	23	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 10\text{ A}$ ; $V_{DS} = 64\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	7.5	-	nC
<b>Source-drain diode FET1 and FET2</b>						
$Q_r$	recovered charge	$I_S = 10\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $T_j = 25\text{ °C}$	-	29.8	-	nC

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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK7K23-80E	LFPAK56D	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K23-80E	72380E

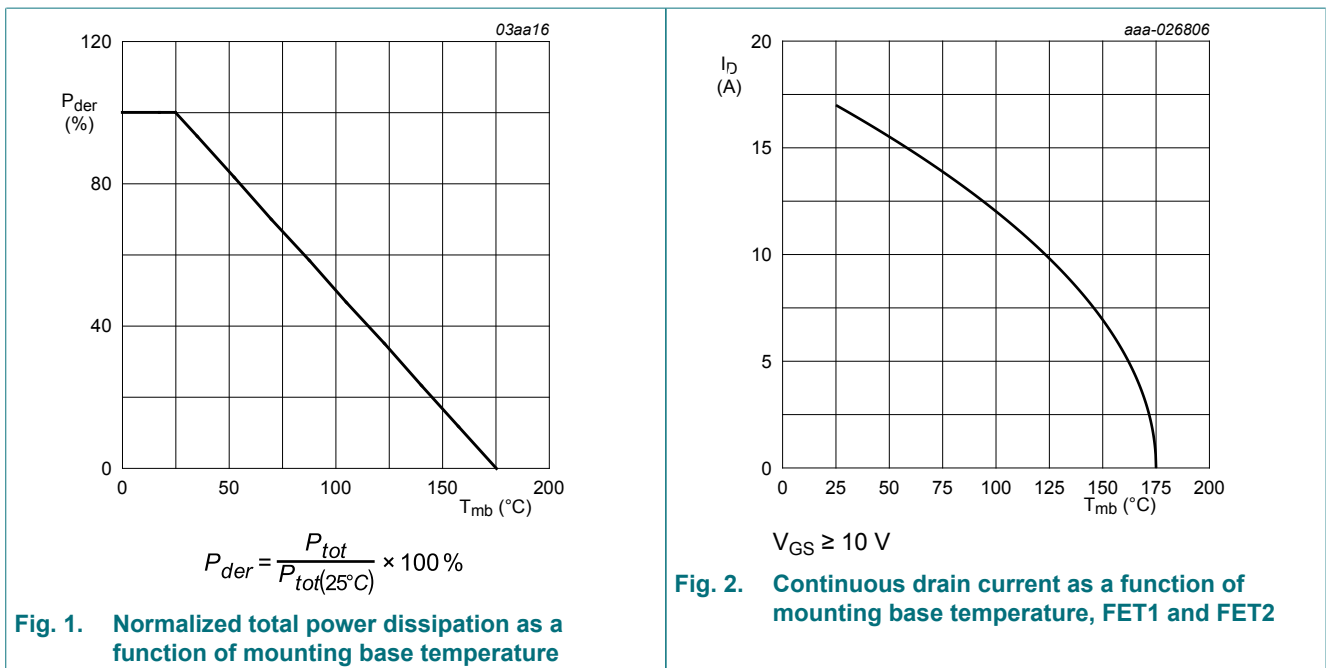
## 8. Limiting values

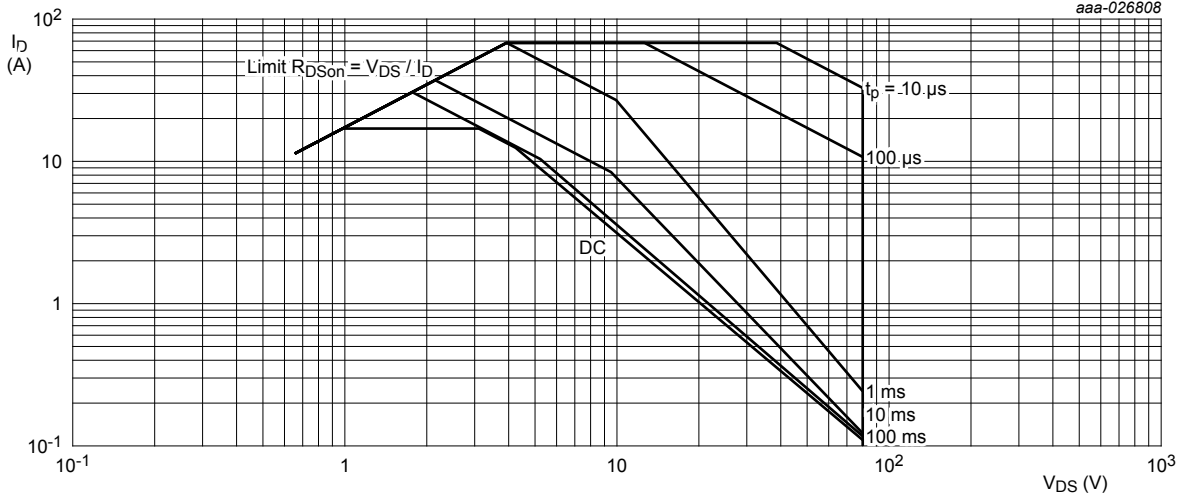
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Limiting values FET1 and FET2</b>					
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	80	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ	-	80	V
V <sub>GS</sub>	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C	-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1	-	53	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2	-	17	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2	-	12	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3	-	68	A
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode FET1 and FET2</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	17	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	68	A
<b>Avalanche ruggedness FET1 and FET2</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 17 A; V <sub>sup</sub> ≤ 80 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; Fig. 4	[1] [2]	-	72 mJ

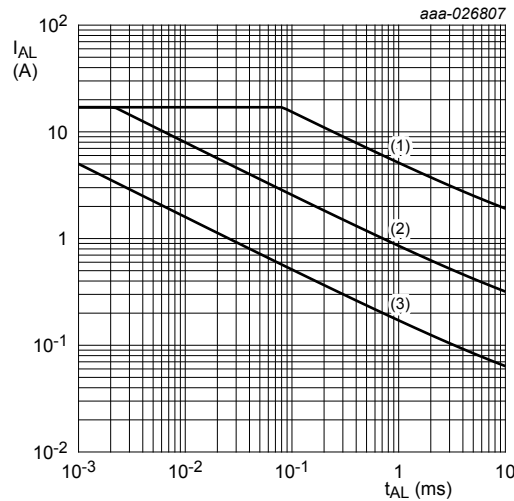
- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.





$T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{DM}$  is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2**



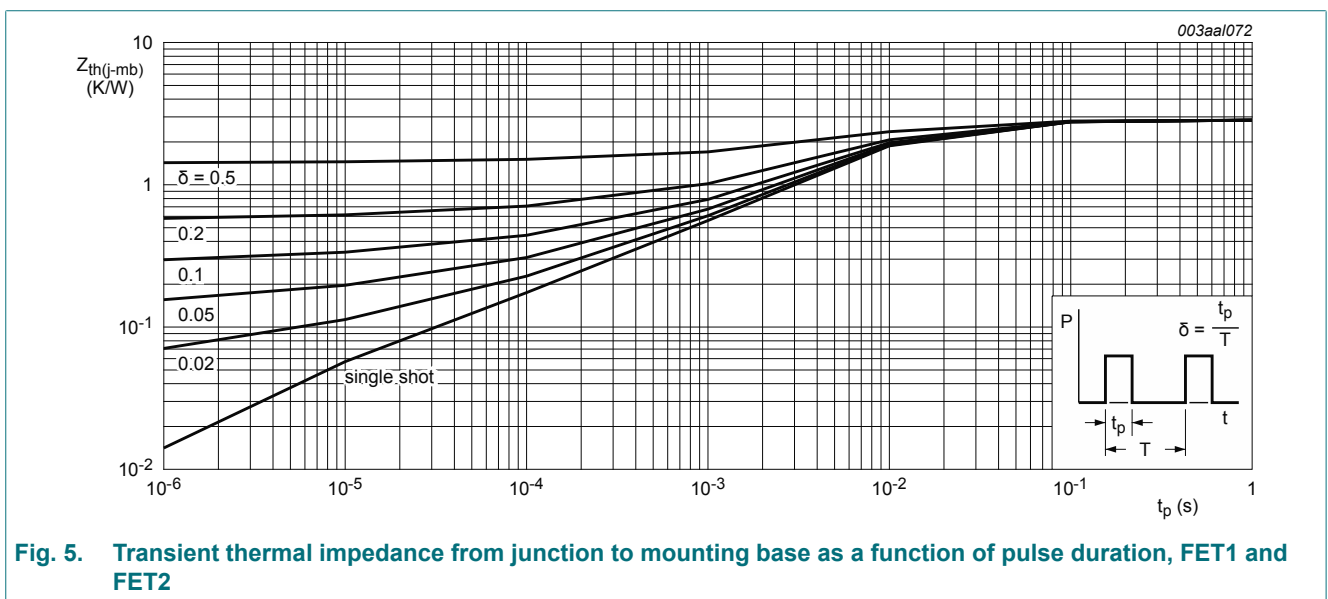
(1)  $T_{j\text{ (init)}} = 25\text{ }^{\circ}\text{C}$ ; (2)  $T_{j\text{ (init)}} = 150\text{ }^{\circ}\text{C}$ ; (3) Repetitive Avalanche

**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	2.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

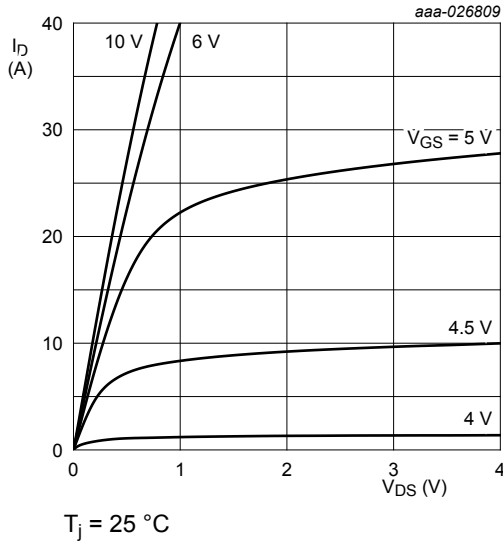


**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2**

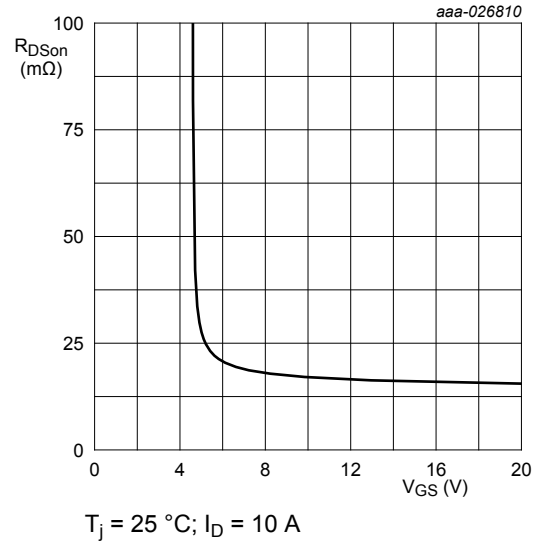
## 10. Characteristics

Table 7. Characteristics

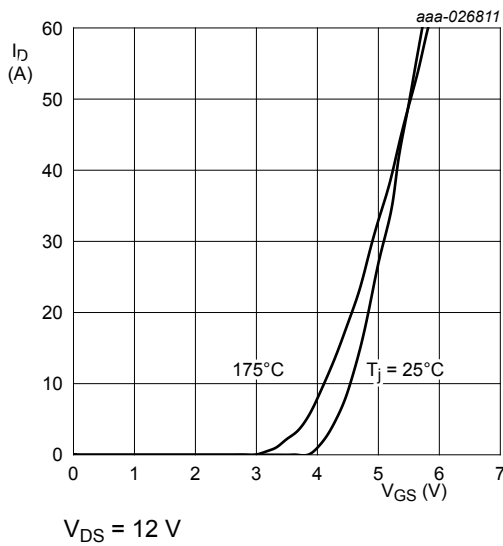
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$ ; <a href="#">Fig. 10</a>	-	-	4.5	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 10</a>	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 11</a>	-	17.6	23	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	-	58	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 64 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	22.8	-	nC
$Q_{GS}$	gate-source charge		-	5	-	nC
$Q_{GD}$	gate-drain charge		-	7.5	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 15</a>	-	1159	1542	pF
$C_{oss}$	output capacitance		-	130	156	pF
$C_{rss}$	reverse transfer capacitance		-	78	107	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 60 \text{ V}; R_L = 5 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	6.4	-	ns
$t_r$	rise time		-	8.9	-	ns
$t_{d(off)}$	turn-off delay time		-	16.9	-	ns
$t_f$	fall time		-	10.9	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 16</a>	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A}/\mu s; V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ C$	-	27.3	-	ns
$Q_r$	recovered charge		-	29.8	-	nC



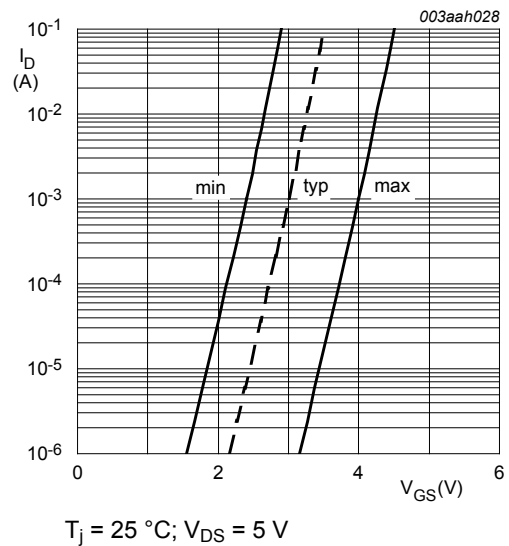
**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2**



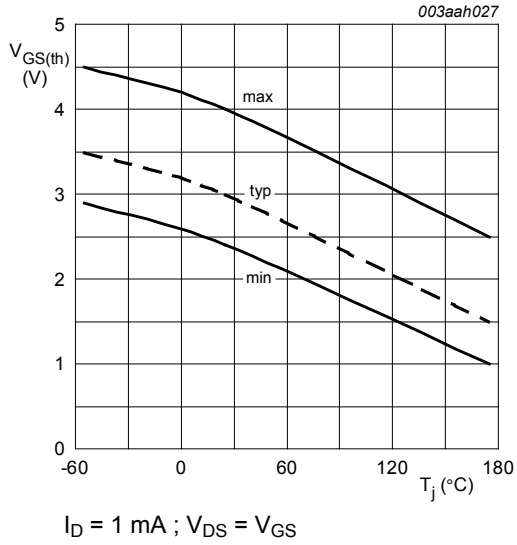
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2**



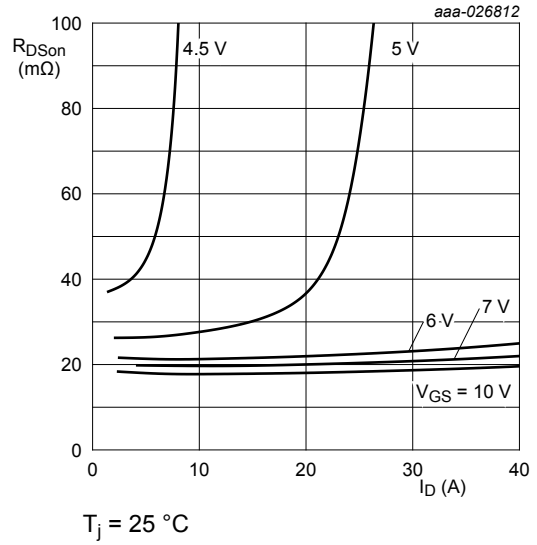
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2**



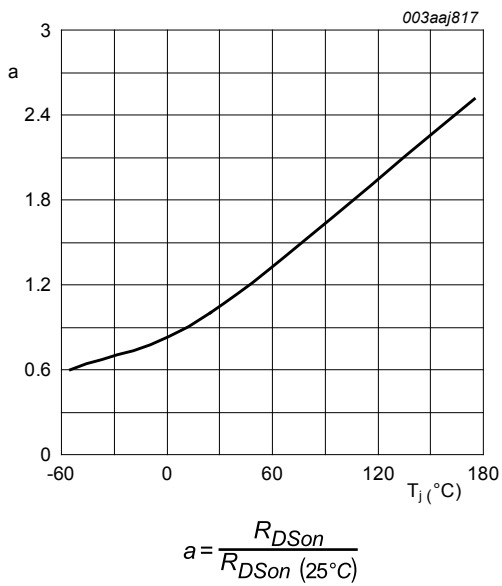
**Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2**



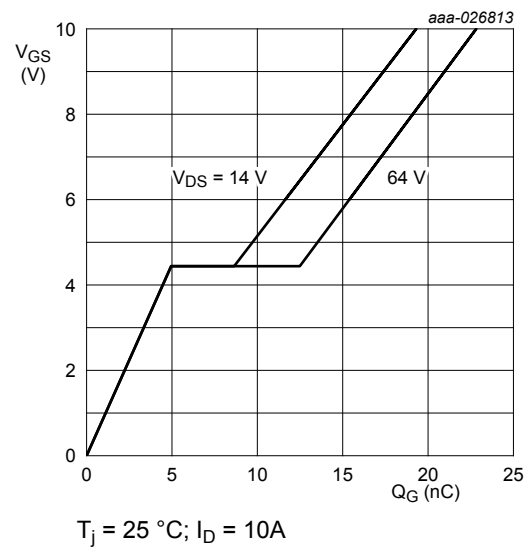
**Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2**



**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2**



**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2**



**Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2**



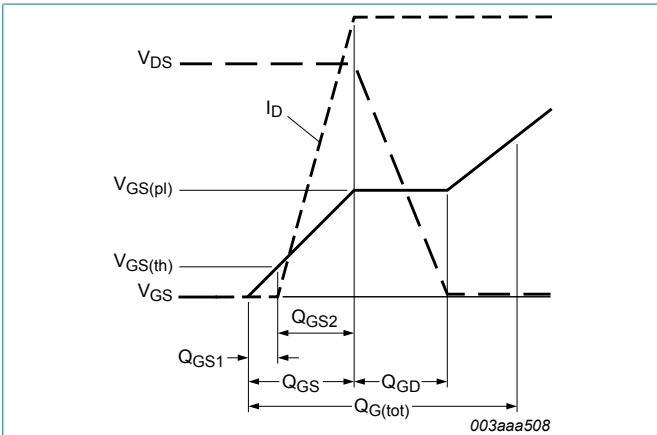
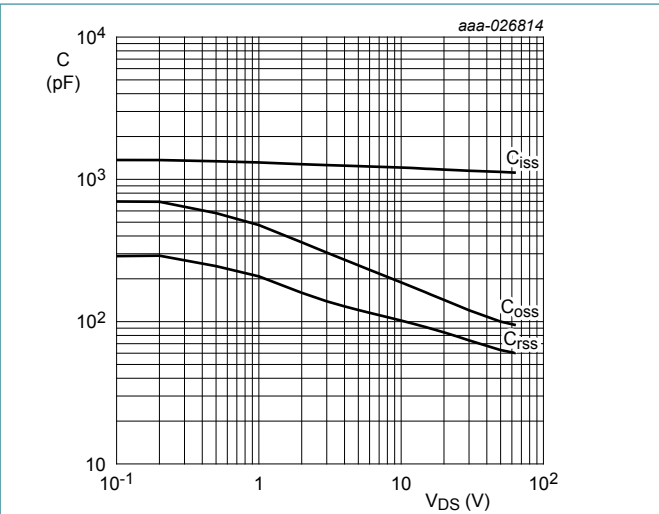
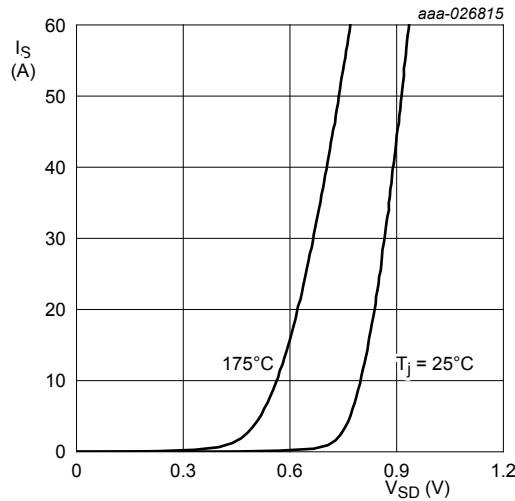


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

### 11. Package outline

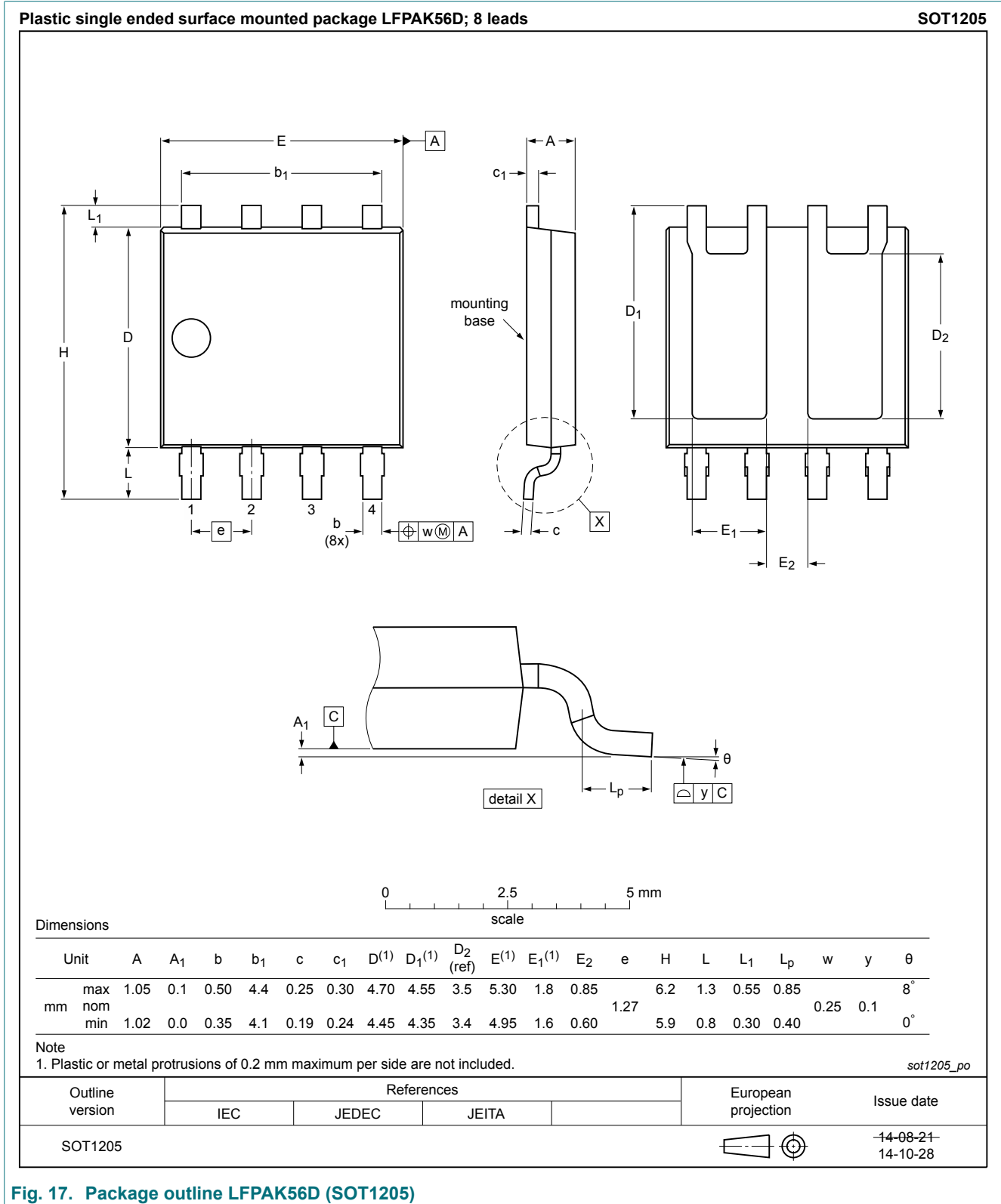


Fig. 17. Package outline LFAK56D (SOT1205)

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Document status [1][2]	Product status [3]	Definition
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Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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