NCA9700

Level translating Fm+ I²C bus repeater/accelerator

Rev. 1 — 10 September 2024 Product data sheet

1. General description

The NCA9700 is a dual-channel bidirectional repeater for I²C and SMBus/PMBus applications. It targets the Fast-mode Plus (Fm+) of the I²C protocol, making the true 1 MHz operation possible without violating I²C timing specifications. This is achieved by using edge accelerators added at all NCA9700 ports that speed up the LOW-to-HIGH transitions of I²C input and output signals.

The NCA9700 provides the buffering for both clock (SCL) and data (SDA) I²C signals with the voltage level translation possibility (up and down) at the same time. The unique feature of the IC is the same operating voltage range of 1.08 V to 3.6 V that can be applied at both port A and port B of the device. This offers more flexibility in how the device can be used in the target application. Multiple NCA9700s can be connected in series or in star, and their ports A and B can be exchanged. Only when the I²C clock stretching needs to be supported, the NCA9700 port A must be connected to the I²C Master side and the NCA9700 port B to the I²C Slave side.

The NCA9700 features integrated pull-up resistors of 4.3 kΩ at each I/O pin. This simplifies the system implementation and reduces BOM count. Though external pull-up resistors are not required, they might be added to shorten the rise times of I²C signals even further.

The NCA9700 provides true signal buffering as the device implementation does not use the pass-FET topology. No static or incremental offsets are needed either, and the lock-free operation is guaranteed by an innovative implementation of the buffers. The very low V_{OL} levels on port A and B improve the noise margin in the application and the potential noise components of input signals are filtered out by Schmitt trigger inputs. To reduce EMI, the negative edges of output signals are slew-controlled.

The NCA9700 is well suited for high-performance low-power applications which use the I²C communication protocol.

2. Features and benefits

- Two-channel bidirectional I²C buffer
- Voltage level translation from 1.08 V to 3.6 V at both port A and port B with unconstrained combination of the supply voltage levels
- Guaranteed 1 MHz operation (true I²C Fast-mode Plus, Fm+)
- Support for the I²C Standard-mode (Sm) and Fast-mode (Fm) operation
- No static voltage offset
- Very low V_{OL} on I/O pins of the port A; V_{OL} regulated to $0.1V_{CCB}$ on I/O pins of the port B
- Input and output rising-edge signal accelerators at all I/Os
- Active-HIGH enable input referenced to V_{CCA} supply
- Lock-free operation
- Glitch-free and sequence-independent IC power-up
- Open-drain input/outputs
- Series connection and star connection of NCA9700 devices possible
- I²C clock stretching support
- Compatibility with I²C bus and SMBus protocols
- Latch-up performance exceeds 100 mA per JESD 78B Class II

- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2 kV
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1 kV
- Very small footprint

3. Applications

- Smart phones and tablets
- Portable medical devices
- Portable instrumentation and test equipment
- Devices for IoT applications
- Power-sensitive applications

4. Ordering information

Table 1. Ordering information

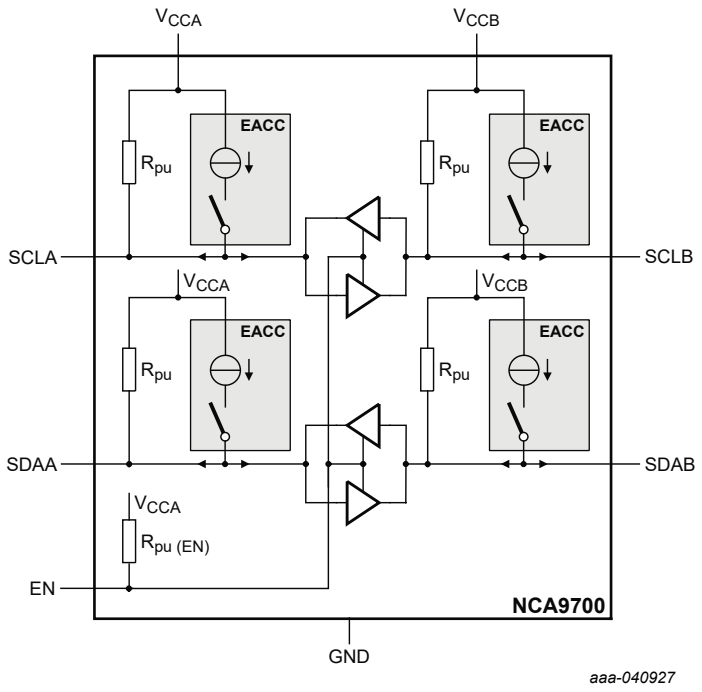
Type number	Package			
	Temperature range	Name	Description	Version
NCA9700DQ	-40 °C to +85 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-3

5. Marking

Table 2. Marking

Type number	Marking code
NCA9700DQ	z3

6. Functional diagram



EACC: Edge Accelerator

Fig. 1. Functional diagram

7. Pinning information

7.1. Pinning

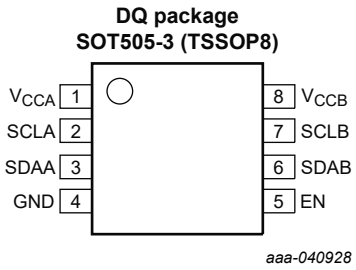


Fig. 2. Pin configuration SOT505-3 (TSSOP8)

7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
V_{CCA}	1	port A supply voltage
SCLA	2	serial clock port A bus
SDAA	3	serial data port A bus
GND	4	supply ground (0 V)
EN	5	active HIGH repeater enable input; referenced to V_{CCA}
SDAB	6	serial data port B bus
SCLB	7	serial clock port B bus
V_{CCB}	8	port B supply voltage

8. Functional description

8.1. Overview

The NCA9700 is a dual-channel bidirectional voltage translating repeater intended for I²C and SMBus/PMBus applications. It includes two bidirectional open-drain buffers for the clock (SCL) and data (SDA) buses of an I²C system. The levels of signals transferred via I²C buses can be up- or down-translated by the NCA9700 within the voltage range of 1.08 V to 3.6 V. The operating supply voltage range of the NCA9700 port A and port B is the same and there are no restrictions in the supply voltage choice nor dependencies between them.

The NCA9700 provides three main functions:

1. **Signal regeneration:** the device receives I²C signals and retransmits them regenerated; since no pass-FET based topology is used, an I²C bus is effectively split into two isolated bus segments with a reduced load capacitance. As a result, higher capacitive loads can be driven than it is possible without the NCA9700.
2. **Signal acceleration:** the NCA9700 reduces the LOW-to-HIGH transition time of input and output I²C signals. This is especially relevant for systems with heavy loaded I²C-buses as a large bus RC time constant means a long signal rise time. The signal acceleration is realized by Edge Accelerators available at all NCA9700 I/Os. Thanks to the Edge Accelerators, the I²C timing, and the data set-up time in particular, can be improved without using low-ohmic pull-up resistors and thus without additional static current consumption.

3. **Voltage translation:** the NCA9700 offers an up- and down-level translation of transmitted signals. The supported voltage range is from 1.08 V to 3.6 V for both NCA9700 ports; there are no restrictions on the voltage level selection for port A and B.

8.2. Key features

Bidirectional voltage translation at symmetrical operating voltage range

Unlike most traditional I²C repeaters, the NCA9700 features a symmetrical operating supply voltage range of 1.08 V to 3.6 V. This means that the supply voltages at port A and B can be exactly the same. There are no restrictions or dependencies between them.

The NCA9700 provides bidirectional, up and down, voltage-level translation over its whole operating voltage range. For example, a voltage down-translation from 3.6 V at port A to 1.08 V at port B or the operation at the lowest allowed voltage of the NCA9700, that is 1.08 V, at both port A and port B (no voltage translation) can be easily realized. This is not possible with other I²C repeaters, which typically are implemented with the minimum supply voltage at port B higher than the supply voltage at port A.

Edge acceleration

The edge acceleration is another unique feature of the NCA9700. The edge accelerators installed at all four I/Os of the NCA9700 speed-up LOW-to-HIGH transitions of I²C signals. By this, the LOW-to-HIGH transition times are less dependent on the I²C-bus RC time constant, which is defined by a pull-up resistor (R_{pu}) and a load capacitor (C_L) on the bus. Especially the choice of the pull-up resistor value requires a careful consideration. Too large pull-up resistor value means long LOW-to-HIGH transition times, while too small resistance value results in a high current consumption. The use of edge accelerators in the NCA9700 simplifies this trade-off. The accelerators modify the charging characteristic of the bus capacitors from exponential to partially- and fully-linear for input and output bus load capacitors, respectively.

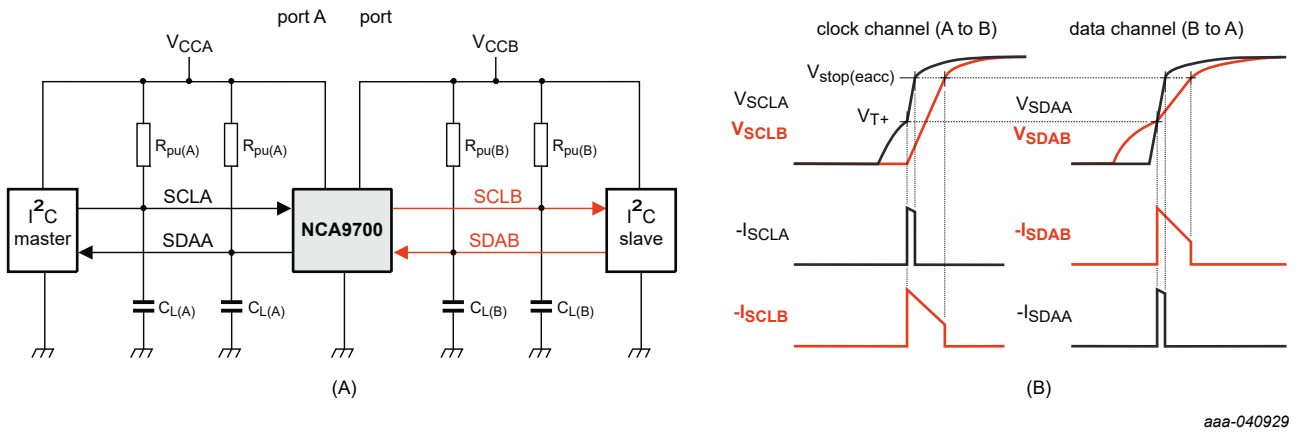
The NCA9700 edge accelerators are implemented as voltage-controlled current sources, see Fig. 1. Let's assume that an I²C signal with a LOW-to-HIGH transition needs to be transmitted from port A to port B of the NCA9700. When an (input) I²C signal at port A crosses V_{T+} threshold level, which corresponds to the voltage of $0.425V_{CCA}$, the input Edge Accelerator (EACC) is activated. As a result, the current starts flowing out of an input pin at port A and the capacitance at port A ($C_{L(A)}$) is getting charged. When the input signal at port A reaches the Edge Accelerator stop level, $V_{stop(eacc)}$, equal to $0.8V_{CCA}$, the input Edge Accelerator is disabled and the current flow stopped. Since the Edge Accelerator current actively helps to charge the input bus capacitance, the input signal transition is accelerated. This happens without a current consumption penalty as the Edge Accelerator current is provided shortly, only during the most critical timing window of the input signal.

The output Edge Accelerator is activated at the same time as the input Edge Accelerator. It monitors the NCA9700 output port, that is port B in case of the A to B transition. Since the output port is normally at logic 0 before a LOW-to-HIGH signal transition takes place, the capacitance of the output port needs to be fully charged from the V_{OL} level to the target voltage level. The output Edge Accelerator current flowing out of the output pin at port B does most of the charging as the charge current via the pull-up resistor(s) is typically smaller. Therefore, unlike in case of the input Edge Accelerator, the charging characteristic of the output port bus capacitor is fully linear till the Edge Accelerator gets deactivated. As for the input Edge Accelerator, this happens when the stop level $V_{stop(eacc)}$ of the output signal, here $0.8V_{CCB}$, is reached.

In Fig. 3, the NCA9700 I/O pin voltages and Edge Accelerator currents for LOW-to-HIGH transitions on the I²C clock and data signals are shown. The timing relations between input and output signals, assuming that the bus capacitance at port A is much lower than the bus capacitance at port B, are indicated. Clearly, a larger bus capacitance results in less steeper charging curve and a longer charging current pulse.

It may happen that when the output bus is very lightly loaded compared to the input bus, the accelerated output signal precedes the input signal. This results in the negative LOW-to-HIGH propagation delay, t_{PLH}, as seen for some cases reported in Table 9.

The activation times of the Edge Accelerators and their current capability depend on the bus capacitance values, pull-up resistance values, and the supply voltages at port A and port B. These parameters impact directly the charging times of the input bus and output bus capacitors and thus the transition times of the input and output signals.



(A) Example I²C system; arrows indicate the assumed signal flow.

(B) I/O pin voltages and corresponding Edge Accelerator currents assuming $C_{L(A)} << C_{L(B)}$ (for simplicity, static currents due to pull-up resistors are omitted in the shown current waveforms).

Fig. 3. The acceleration of LOW-to-HIGH I²C clock and data signal transitions by the NCA9700

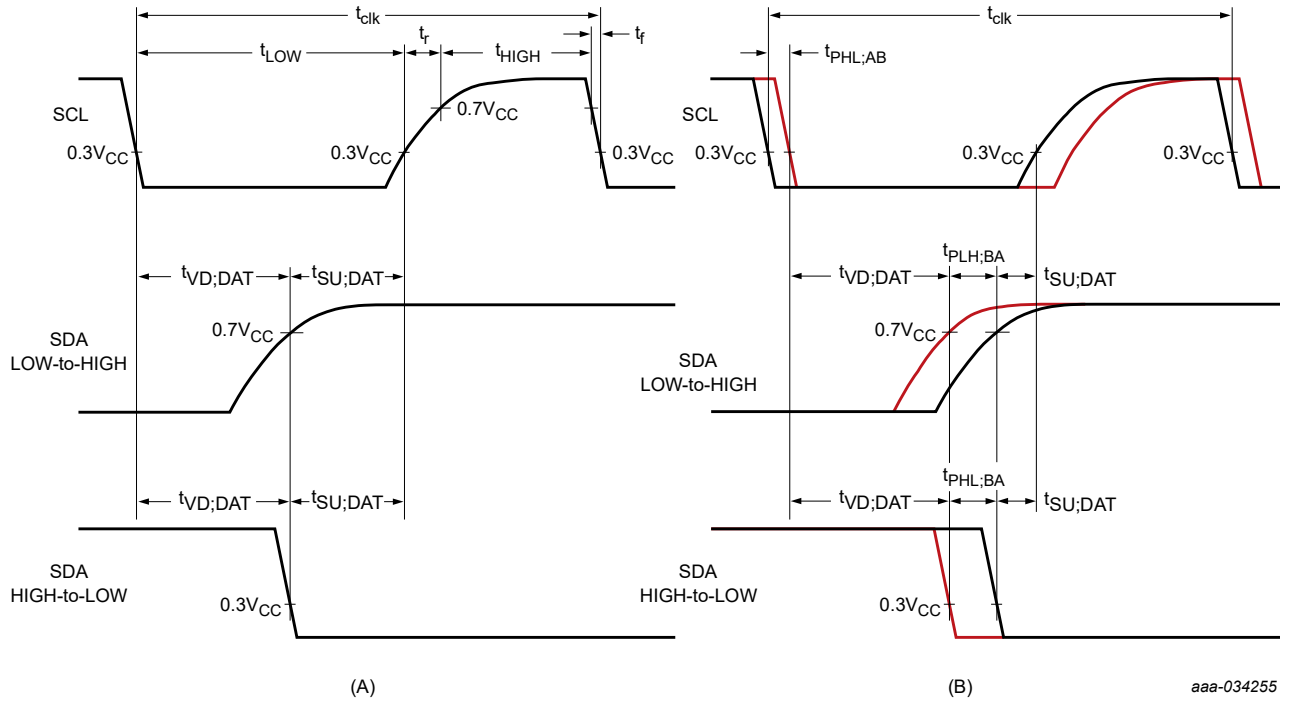
The current capability of the NCA9700 Edge Accelerators for clock and data channels is different. The currents of the input and output Edge Accelerators for the clock channel (SCLA and SCLB pins) are about 25 % to 30 % lower than the currents of the input and output Edge Accelerators for the data channel (SDAA and SDAB pins). This stems from the fact that the activation window of the input Edge Accelerator (corresponding to the input signal voltage levels from $0.425V_{CC}$ to $0.8V_{CC}$, where V_{CC} is V_{CCA} or V_{CCB}) lies outside the timing window of an I²C clock signal (corresponding to the input signal voltage range from 0 V to $0.3V_{CC}$, where V_{CC} is V_{CCA} or V_{CCB}) that is critical for I²C parameters such as the data set-up time (see next section for more details). The Edge Accelerator current is thus reduced to save the total device power.

Data set-up time gain

The timing of I²C signals is governed by strict specifications of the I²C protocol. The parameters such as:

- LOW and HIGH periodes, t_{LOW} and t_{HIGH} (for I²C clock signal, SCL)
- rise and fall times, t_r and t_f (for I²C clock and data signals, SCL and SDA)
- data valid time, $t_{VD;DAT}$
- data set-up time, $t_{SU;DAT}$

play the key role. The definitions of these parameters are shown in Fig. 4 (A), and their values for the I²C Fast-mode Plus are listed in Table 4.



(A) I²C system without an I²C repeater, see Fig. 5 (A)

(B) I²C system with an I²C repeater (black: port A signals, red: port B signals), see Fig. 5 (B).

Fig. 4. Timing diagram of I²C clock and data signals

Table 4. Critical timing parameters of the I²C protocol and their values for Fm+

Parameter	Description	Min	Max	Unit
t_{LOW}	LOW period of I²C clock signal	500	-	ns
t_{HIGH}	HIGH per period of I²C clock signal	260	-	ns
t_r	Rise time of I²C clock and data signals	-	120	ns
t_f	Fall time of I²C clock and data signals	$20x(V_{CC}/5.5)$	120	ns
$t_{VD;DAT}$	Data valid time	-	450	ns
$t_{SU;DAT}$	Data set-up time	50	-	ns

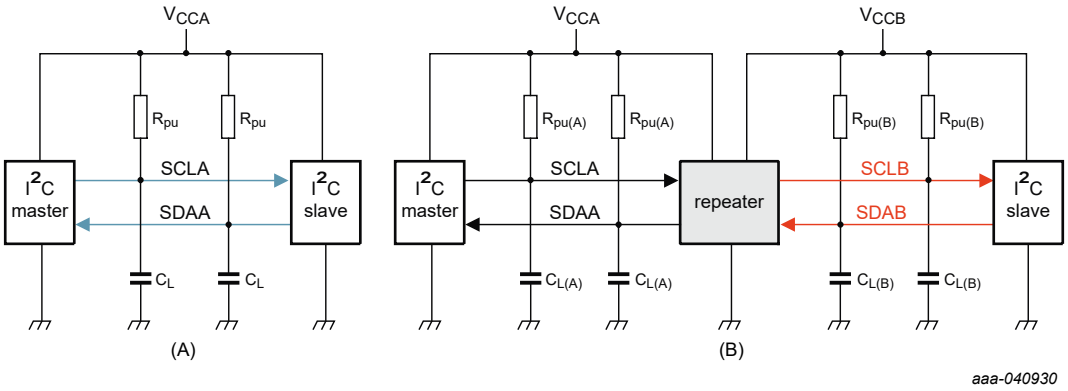
When an I²C repeater is introduced to the I²C system for bus capacitance buffering, the repeater propagation delays are added and the signal timing changed. The new situation is shown in Fig. 4 (B) with the depicted waveforms corresponding to the I²C system shown in Fig. 5 (B). Clearly, the timing budget is now reduced and reaching the target clock frequency of 1 MHz is often not possible. This is because in the Fm+ there is no time margin left for the repeater delays (i.e. in the worst case, $t_{LOW} + t_{HIGH} + t_r + t_f = t_{clk}$ = 1000 ns, which is, the clock period of 1 MHz clock).

The Edge Accelerators of the NCA9700 address exactly this problem. By the acceleration of I²C input and output signals, the timing margin is regained. In particular, the propagation delay of the NCA9700 repeater during a LOW-to-HIGH transition is considerably reduced. This is because the output Edge Accelerator, which speeds up the output signal, is activated as soon as a LOW-to-HIGH transition of the input signal is detected.

The impact of this is illustrated in the following figures. In Fig. 5, I²C systems with and without an I²C repeater are compared. The arrows in the figures indicate the signal flow reflecting the worst case situation from the I²C timing point of view, that is the I²C clock provided by the Master (A to B communication) and the I²C data read out from the Slave (B to A communication).[1]

1 Assuming that the repeater is symmetrical, an alternative worst-case timing-wise signal flow is: B to A for an I²C clock signal, and A to B for an I²C data signal.

In Fig. 6, the corresponding timing diagrams with the focus on the data set-up time parameter for the LOW-to-HIGH transition[2] are shown. The data set-up time is measured between I²C data and clock signals at port A of the I²C repeaters.

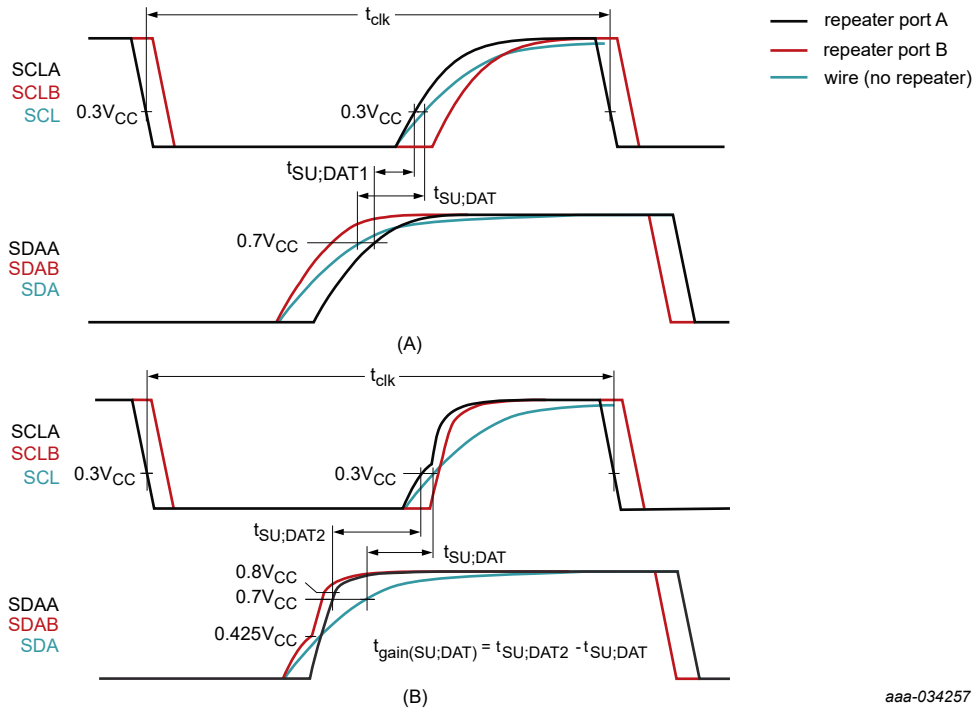


(A) system without an I²C repeater (the reference).

(B) system with an I²C repeater (traditional repeater or the NCA9700 repeater).

Arrows indicate the signal flow direction.

Fig. 5. I²C systems used in the comparison of the data set-up times



(A) traditional I²C repeater.

(B) the NCA9700 I²C repeater.

In both cases, the waveforms are compared to the no-repeater case (i.e. a repeater replaced by a wire).

Fig. 6. The comparison of data set-up times for an I²C system

In Fig. 6 (A), data and clock signals for an I²C system with a traditional I²C repeater are shown. They are compared with similar signals of the system without a repeater (i.e. a repeater replaced with a wire). The slopes of the data and clock signals in the system with a repeater are steeper

2 The LOW-to-HIGH transition improvement is addressed only.

because the effective I²C bus capacitance is reduced. The data set-up time of the I²C system with a traditional repeater, $t_{SU;DAT1}$, is very short.

In Fig. 6 (B), the same waveforms but for the NCA9700 replacing a traditional I²C repeater are presented, and compared with the waveforms of the system with no repeater (the same as in Fig. 6 (A)). The slopes of the input and output data and clock signals are much steeper thanks to the NCA9700 Edge Accelerators. Especially the timing of the data signal is improved (the start and stop levels of the input Edge Accelerator are indicated on the input data signal waveform). Besides, the data signal propagation delay is shorten considerably as the generation of the output signal is speeded up by the output Edge Accelerator. The data set-up time in this case, $t_{SU;DAT2}$, is much longer. To illustrate the true advantage of the NCA9700 repeater with respect to the no-repeater case, the data set-up time gain, $t_{gain(SU;DAT)}$, is introduced. This parameter is calculated as the difference between the data set-up times of the NCA9700 and a wire (no repeater case). The data set-up time gain is one of the key parameters of the NCA9700 and it is specified in Table 10.

Schmitt trigger inputs

Each I/O pin of the NCA9700 includes a Schmitt trigger comparator for detecting the logic level of an input signal. The same comparator activates also the NCA9700 input Edge Accelerator. When a positive going input signal (LOW-to-HIGH transition) crosses the comparator V_{T+} level, that is $0.425V_{CCA}$ and $0.425V_{CCB}$ for input stages at port A and B, respectively, it is interpreted as logic 1 (HIGH). Similarly, when a negative going input signal (HIGH-to-LOW transition) crosses the comparator V_{T-} level, that is $0.25V_{CCA}$ and $0.25V_{CCB}$ for input stages at port A and B, respectively, it is interpreted as logic 0 (LOW). The difference between switching levels of the input comparator, thus $V_{T+} - V_{T-}$, defines the comparator hysteresis. It is guaranteed that the comparator hysteresis is never smaller than $0.130V_{CC}$, which helps with noise rejection on input signals.

Integrated pull-up resistors

The NCA9700 has integrated pull-up resistors of 4.3 kΩ on all I/O pins. Therefore, no additional external pull-up resistors are required to pull-up I²C data and clock buses. However, a user may add external pull-up resistors on all or selected bus segments to reduce the effective pull-up resistance. This has a two-fold effect: it reduces the bus capacitor initial charging time (i.e. from 0V to $0.425V_{CC}$), defined by the bus RC time constant, and provides an extra current when the Edge Accelerator is already activated. This is especially relevant for heavy-loaded I²C buses but comes at the cost of extra static current consumption. It is recommended, though not required, to use external pull-up resistors on buses connected to port B. This improves the output signal settle time as the V_{OL} of the pins at port B are regulated.

As long as the NCA9700 supply is present, the internal resistors always pull the I²C buses up. This is to prevent that these buses are floating when the NCA9700 is disabled (EN = LOW) and no external pull-up resistors are present. When the supply at the NCA9700 port A or B is not available (below the supply V_{UVLO} level), the internal pull-up resistors are deactivated to block the leakage path from an I/O to supply pin.

Ultra-low power consumption

The NCA9700 implementation facilitates the system-level power consumption reduction. When disabled (EN = LOW), the IC keeps only internal bias/reference blocks active. This allows nearly a factor of 3 reduction of the total IC current consumption compared to the enable state (EN = HIGH).

The NCA9700 partial power down, when the supply of port A or port B is removed, is also possible. In this mode, the active power supply does not consume any current. Obviously, the IC drivers are switched off then so signal transmission is not possible.

No static voltage offset

The NCA9700 does not use a static offset voltage to determine the driving side of the NCA9700. The device self-locking is prevented by an innovative implementation technique of the buffers. As

a result, this simple and reliable solution eliminates constraints on the NCA9700 connectivity and communication with other system components.

Regulated output voltage

The NCA9700 pins at port B (SCLB and SDAB) have their V_{OL} level regulated to about $0.1V_{CCB}$. This allows keeping V_{OL} levels very low, even at port B of the repeater where the clock stretching and acknowledge from a Slave device must be handled properly. Since the V_{OL} level is supply-dependent rather than at the (nearly) fixed level, such a implementation relaxes the requirement on the external driver strength. It also makes the detection of the bus pull-down by an external driver more reliable especially when ground bouncing is present.

Clock stretching

Although the NCA9700 ports are symmetrical and can be exchanged, when I²C clock stretching is used, an I²C Master must be connected to port A and I²C Slaves to port B. Also, the NCA9700 clock channel needs to be used for the transmission of the I²C clock signal.

The I²C protocol assumes that the clock signal is always generated by the Master. But when the clock stretching is applied, a Slave is allowed to hold down the I²C clock bus to communicate to the Master that the Slave is not ready. This means that the clock bus at port B is concurrently driven by two independent drivers: the NCA9700 internal clock driver of port B (clock transfer from the Master from port A to port B) and the external driver at port B (clock bus held by the Slave is communicated from port B to port A). Therefore, for a successful transmission of logic LOW from port B to port A while clock stretching, a correct detection of the presence of an external driver is critical. For this, the NCA9700 V_{ILC}, contention LOW-level input voltage, needs to be satisfied. V_{ILC} defines the minimum input voltage at the NCA9700 SCLB pin required for the correct detection of the clock bus pull down by an external driver (i.e. an internal driver of an I²C Slave). The maximum V_{ILC} is equal to half of the V_{OL} level for the SCLB pin.

As already mentioned, the V_{OL} of the SCLB pin is regulated to about $0.1V_{CCB}$. For the clock stretching to be detected, an external driver needs to pull down the SCLB pin to V_{ILC} level or below. To calculate the required strength (resistance) of the internal pull- down MOSFET in the I²C Slave output driver, the V_{OL} value at given I_{OL} current from Table 8 can be used. Alternatively, a user can measure the V_{OL} level of the SCLB pin at the known effective pull-up resistance.

Acknowledgment signal handling

In the I²C protocol, each group of eight bits transmitted on the data bus must be followed by an acknowledgement (ACK) bit. The ACK bit is a logic 0 (LOW) and is sent by a receiver of the data (e.g. by an I²C Slave when an I²C Master sends data to the Slave). The correct acknowledgement signal handling means the correct detection of a bus pull-down initiated by an external driver (e.g. of an I²C Slave device) in different transmission conditions. This is fundamentally difficult when the V_{OL} level of the pin where the pull-down must be detected is low or when an edge accelerator is present, like in the NCA9700. The external pull-down detection is also influenced by system parameters, such a supply voltage, bus load capacitance, and pull-up resistance.

To resolve this, the NCA9700 provides a multi-level solution. If the ACK bit is proceeded by the last data bit (of a 8-bit package) being a logic 0 (an equivalent of a LOW to LOW transition), the NCA9700 uses the same mechanism as it is used on the clock pin (SCLB pin) for the clock stretching detection (which can also be seen as a LOW to LOW transition).

If the ACK bit is proceeded by the data bit being a logic 0 (LOW) but the ACK signal is a bit delayed with respect to the clock signal (I²C protocol defines the time window of $t_{VD;ACK}$, data valid acknowledgement time, for sending the acknowledgement), the data bus is released and it will be pulled up by pull-up resistor(s) and the Edge Accelerator. In this case, the pull-up elements will be working against the driver of an external device that tries to pull the bus down; as a result, the bus will probably settle at some intermediate level. For this situation the NCA9700 provides a timer-based solution. The 120 ns-timer (typical) is started at the same instance as the output Edge Accelerator on this pin is activated. The timer defines the time window in which the data bus

voltage is monitored by the NCA9700 internal circuitry. If the bus voltage remains below the start level of the output Edge Accelerator when the timer times out, the ACK signal is detected. If the data bus voltage crosses the Edge Accelerator start level before the timer times out, the timer is reset and re-started at the crossing level again. The bus voltage is again monitored and compared against the output Edge Accelerator stop level. If the stop level is not crossed before the timer times out, the ACK signal is detected.

If the ACK signal is proceeded by the data bit being a logic 1 (HIGH), the ACK signal sent by an external device is interpreted as a HIGH to LOW transition and it will be always resolved correctly by the NCA9700.

The timer-based solution for the acknowledgement signal handling is present at both the SDAA pin (port A) and the SDAB pin (port B). In this way, the ACK signals sent by both Master and Slave devices can be handled properly.

Active high enable input

The NCA9700 is disabled when the V_{CCA} and V_{CCB} supply voltages are below the supply V_{start} level. When the V_{start} level is reached and the EN pin is left unconnected, the NCA9700 will be enabled by default as the EN pin, referenced to the V_{CCA} supply, is pulled up internally. By driving the EN pin externally, enabling or disabling of the NCA9700 is possible under system control, for example to isolate a badly behaved I²C Slave on the system power up.

The logic level of the enable pin is sensed by a comparator with hysteresis. A small filter placed on the EN pin prevent incorrect switching on/off of the IC in case of noise on this pin.

The NCA9700 can be started correctly only when all buses connected to the repeater ports are in the idle state (i.e. pulled up). Not complying with this may lead to the device lockup. To prevent system failures, the EN pin should change state only when I²C buses are idle too.

It is not allowed in the application to drive the EN pin from the source with a voltage higher than the V_{CCA} supply voltage. Therefore, at the power up it is recommended to tight the EN pin to the V_{CCA} pin or left it floating so that the EN pin voltage will follow the supply.

Slew control for the falling edges

The HIGH-to-LOW transition times of output signals in an I²C repeater depend on the effective pull-up resistance at the given node and the resistance of the internal pull-down MOSFET. In the NCA9700, the internal pull-down MOSFETs are made strong to guarantee low V_{OL} levels over the full operating voltage range of the IC. Typically, this would result in very fast falling edges of output signals, especially for high supply voltages and low output capacitors, and could lead to EMI issues. To prevent this without compromising the timing of I²C signals, the output signals' falling edges are slew-controlled in the NCA9700. By this, a good independence on the I²C bus load conditions is achieved.

8.3. Functional modes

Table 5 describes the functionality of the NCA9700 voltage-translating repeater dependent on the state of the EN pin.

Table 5. Function table of the NCA9700

EN pin	Function
LOW	IC disabled; outputs disabled; buses at port A and port B pulled up (by internal pull-up resistors)
HIGH	IC enabled; outputs enabled: SCLA = SCLB SDAA = SDAB

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages and currents					
V_{CCA}	supply voltage port A		-0.5	+4.0	V
V_{CCB}	supply voltage port B		-0.5	+4.0	V
$V_{I(EN)}$	input voltage	EN pin	-0.5	+4.0	V
$V_{I/O}$	input/output voltage	I²C bus voltage port A and port B	-0.5	+4.0	V
I_{OL}	LOW-level output current	I/Os port A and port B	-	25	mA
T_{stg}	storage temperature		-65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	+125	°C
Electrostatic discharge					
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	-2000	+2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3	-1000	+1000	V

10. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCA}	supply voltage port A		1.08	3.6	V
V_{CCB}	supply voltage port B		1.08	3.6	V
$V_{I/O}$	input/output voltage	SCLA, SCLB	0	3.6	V
		SDAA, SDAB	0	3.6	V
		EN	0	V_{CCA}	V
T_{amb}	ambient temperature		-40	+85	°C

11. Static characteristics

Table 8. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);
V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V; unless otherwise specified; Internal pull-up resistors used.

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
Supplies						
V_{start}	start voltage	V_{CCA}; V_{CCA} rising; V_{CCB}= 1.08 V to 3.6 V or V_{CCB}; V_{CCB} rising; V_{CCA}= 1.08 V to 3.6 V	495	680	1080	mV
V_{UVLO}	undervoltage lockout voltage	V_{CCA}; V_{CCA} falling; V_{CCB}= 1.08 V to 3.6 V or V_{CCB}; V_{CCB} falling; V_{CCA}= 1.08 V to 3.6 V	-	485	800	mV
I_{CCA}	supply current port A	SCLA = SDAA = V_{CCA} (with internal pull-up resistors); SCLB = SDAB = open (with internal pull-up resistors); V_{CCB} = 1.2 V; EN = GND				
		V_{CCA} = 1.08 V	-	4	7	µA
		V_{CCA} = 1.2 V	-	5	8	µA
		V_{CCA} = 1.8 V	-	8	12	µA
		V_{CCA} = 3.6 V	-	17	24	µA
		SCLA = SDAA = V_{CCA} (with internal pull-up resistors); SCLB = SDAB = open (with internal pull-up resistors); V_{CCB} = 1.2 V; EN = V_{CCA}				
		V_{CCA} = 1.08 V	-	16	32	µA
		V_{CCA} = 1.2 V	-	18	34	µA
		V_{CCA} = 1.8 V	-	29	54	µA
		V_{CCA} = 3.6 V	-	51	94	µA
		SCLA = SDAA = GND; SCLB = SDAB = open (with internal pull-up resistors); V_{CCB} = 1.2 V; EN = V_{CCA}				
		V_{CCA} = 1.08 V	-	0.5	0.8	mA
		V_{CCA} = 1.2 V	-	0.6	0.9	mA
		V_{CCA} = 1.8 V	-	0.9	1.32	mA
		V_{CCA} = 3.6 V	-	1.9	2.7	mA
		SCLA = SDAA = open (with internal pull-up resistors); SCLB = SDAB = GND; V_{CCB} = 1.2 V; EN = V_{CCA}				
		V_{CCA} = 1.08 V	-	0.5	0.8	mA
		V_{CCA} = 1.2 V	-	0.6	0.9	mA
		V_{CCA} = 1.8 V	-	0.9	1.32	mA
		V_{CCA} = 3.6 V	-	1.9	2.7	mA

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
I_{CCB}	supply current port B	SCLB = SDAB = V_{CCB} (with internal pull-up resistors); SCLA = SDAA = open (with internal pull-up resistors); V_{CCA} = 1.2 V; EN = GND				
		V_{CCB} = 1.08 V	-	4	7	µA
		V_{CCB} = 1.2 V	-	5	8	µA
		V_{CCB} = 1.8 V	-	8	11	µA
		V_{CCB} = 3.6 V	-	17	24	µA
		SCLB = SDAB = V_{CCB} (with internal pull-up resistors); SCLA = SDAA = open (with internal pull-up resistors); V_{CCA} = 1.2 V; EN = V_{CCA}				
		V_{CCB} = 1.08 V	-	13	27	µA
		V_{CCB} = 1.2 V	-	15	27	µA
		V_{CCB} = 1.8 V	-	25	40	µA
		V_{CCB} = 3.6 V	-	44	72	µA
		SCLB = SDAB = GND; SCLA = SDAA = open (with internal pull-up resistors); V_{CCA} = 1.2 V; EN = V_{CCA}				
		V_{CCB} = 1.08 V	-	0.5	0.8	mA
		V_{CCB} = 1.2 V	-	0.6	0.9	mA
		V_{CCB} = 1.8 V	-	0.9	1.32	mA
		V_{CCB} = 3.6 V	-	1.9	2.7	mA
		SCLB = SDAB = open (with internal pull-up resistors); SCLA = SDAA = GND; V_{CCA} = 1.2 V; EN = V_{CCA}				
		V_{CCB} = 1.08 V	-	0.2	0.4	mA
		V_{CCB} = 1.2 V	-	0.3	0.5	mA
		V_{CCB} = 1.8 V	-	0.5	0.8	mA
		V_{CCB} = 3.6 V	-	1.1	1.6	mA
$I_{CC(tot)}$	total supply current	I_{CCA} + I_{CCB}; SCLA = SDAA = V_{CCA} (with internal pull-up resistors); SCLB = SDAB = V_{CCB} (with internal pull-up resistors); V_{CCA} = V_{CCB} = 1.2 V				
		EN = V_{CCA}	-	35	-	µA
		EN = GND	-	11	-	µA

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
Input and output SCLA, SDAA, SCLB, SDAB pins						
V_{T+}	positive-going threshold voltage	input of I/O circuit; input edge accelerator start voltage; SCLA; SDAA; SCLB; SDAB; V_{CC}: V_{CCA} or V_{CCB} = 1.08 V to 3.6 V	$0.35V_{CC}$	$0.43V_{CC}$	$0.50V_{CC}$	V
V_{T-}	negative-going threshold voltage	input of I/O circuit; SCLA; SDAA; SCLB; SDAB; V_{CC}: V_{CCA} or V_{CCB} = 1.08 V to 3.6 V	$0.19V_{CC}$	$0.25V_{CC}$	$0.32V_{CC}$	V
V_{HYS}	hysteresis voltage	input of I/O circuit; SCLA; SDAA; SCLB; SDAB; (V_{T+} - V_{T-}) V_{CC}: V_{CCA} or V_{CCB} = 1.08 V to 3.6 V	$0.13V_{CC}$	$0.17V_{CC}$	$0.22V_{CC}$	V
$V_{stop\ (eacc)}$	edge accelerator stop voltage	SCLA; SDAA; SCLB; SDAB; V_{CC}: V_{CCA} or V_{CCB} = 1.08 V to 3.6 V	$0.70V_{CC}$	$0.80V_{CC}$	$0.89V_{CC}$	V
$I_{O(eacc)}$	edge accelerator output current	SCLA; V_I = $0.5V_{CCA}$ or SCLB; V_I = $0.5V_{CCB}$				
		V_{CCA} or V_{CCB} = 1.08 V	-	-1.6	-	mA
		V_{CCA} or V_{CCB} = 1.2 V	-	-2.3	-	mA
		V_{CCA} or V_{CCB} = 1.8 V	-	-6.3	-	mA
		V_{CCA} or V_{CCB} = 3.6 V	-	-19	-	mA
		SDAA; V_I = $0.5V_{CCA}$ or SDAB; V_I = $0.5V_{CCB}$				
		V_{CCA} or V_{CCB} = 1.08 V	-	-2.2	-	mA
		V_{CCA} or V_{CCB} = 1.2 V	-	-3.2	-	mA
		V_{CCA} or V_{CCB} = 1.8 V	-	-8.0	-	mA
		V_{CCA} or V_{CCB} = 3.6 V	-	-23	-	mA
V_{OL}	LOW-level output voltage	SCLA; SDAA				
		I_{OL} = 0 mA (internal current only); V_{IB} = 0 V or V_{IA} = 0 V	-	5	45	mV
		I_{OL} = 2 mA (external current; internal current added); V_{IB} = 0 V or V_{IA} = 0 V	-	30	190	mV
		SCLB; SDAB				
		I_{OL} = 0 mA (internal current only); V_{IA} = 0 V				
		V_{CCB} = 1.08 V to 1.2 V	65	$0.1V_{CCB}$	175	mV
		V_{CCB} = 1.8 V	125		235	mV
		V_{CCB} = 3.6 V	300		400	mV
		I_{OL} = 2 mA (external current; internal current added); V_{IA} = 0 V				
		V_{CCB} = 1.08 V to 1.2 V	65	$0.1V_{CCB}$	175	mV
		V_{CCB} = 1.8 V	125		235	mV
		V_{CCB} = 3.6 V	300		400	mV
V_{ILC}	contention LOW-level input voltage	SCLB				
		clock stretching; V_{CCB} = 1.08 V to 1.2 V	-	-	$0.45V_{OL(SCLB)min}$	mV
		clock stretching; V_{CCB} = 1.8 V	-	-	$0.50V_{OL(SCLB)min}$	mV
		clock stretching; V_{CCB} = 3.6 V	-	-	$0.60V_{OL(SCLB)min}$	mV

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
R_{pu}	pull-up resistance	internal pull-up resistance SCLA; SCLB; SDAA; SDAB				
		V_{CCA} or V_{CCB} = 1.08 V	3.2	4.4	6.0	kΩ
		V_{CCA} or V_{CCB} = 1.2 V	3.1	4.3	5.9	kΩ
		V_{CCA} or V_{CCB} = 1.8 V	3.0	4.25	5.8	kΩ
		V_{CCA} or V_{CCB} = 3.6 V	2.9	4.2	5.7	kΩ
		external pull-up resistance SCLA; SCLB; SDAA; SDAB	0.3	-	-	kΩ
I_I	input leakage current	SCLA; SDAA				
		V_I = V_{CCA}; EN = GND	-	-	1	µA
		V_I = 3.6 V; V_{CCA} = 0 V	-	-	1	µA
		SCLB; SDAB				
		V_I = V_{CCB}; EN = GND	-	-	1	µA
		V_I = 3.6 V; V_{CCB} = 0 V	-	-	1	µA
$C_{I/O}$	input/output capacitance	SCLA; SDAA				
		V_I = 3.6 V or 0 V; V_{CCA} = 3.6 V; f = 1 MHz; EN = GND	-	-	5	pF
		V_I = 3.6 V or 0 V; V_{CCA} = 0 V; f = 1 MHz	-	-	7	pF
		SCLB; SDAB				
		V_I = 3.6 V or 0 V; V_{CCB} = 3.6 V; f = 1 MHz; EN = GND	-	-	6	pF
		V_I = 3.6 V or 0 V; V_{CCB} = 0 V; f = 1 MHz	-	-	8	pF
Enable						
$V_{T+(EN)}$	positive-going threshold voltage	EN pin	$0.36V_{CCA}$	$0.55V_{CCA}$	$0.68V_{CCA}$	V
$V_{T-(EN)}$	negative-going threshold voltage	EN pin	$0.2V_{CCA}$	$0.33V_{CCA}$	$0.44V_{CCA}$	V
$R_{pu(EN)}$	pull-up resistance	EN pin	1.67	2.30	4.20	MΩ
I_I	input leakage current	V_I = V_{CCA}	-	-	1	µA
		V_I = 0 V; V_{CCA}= 3.6 V	-2	-	-	µA
C_I	input capacitance	V_I = 3.6 V; V_{CCA} = 3.6 V; f = 1 MHz	-	-	5	pF

[1] Typical values are measured at T_{amb} = 25 °C, V_{CCA} = 1.2 V and V_{CCB} = 1.2 V; unless otherwise specified.

12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);
For waveforms see Fig. 7; For test circuits see Fig. 8.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C						Unit
			Port A: 10 pF Port B: 160 pF[1]			Port A: 85 pF Port B: 85 pF[2]			
			Min	Typ[3]	Max	Min	Typ[3]	Max	
$f_{clk(max)}$	maximum clock frequency	SCLA; SCLB [4]	1000	-	-	1000	-	-	kHz
t_{PLH}	LOW to HIGH propagation delay	SCLA; SCLB; V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V							
		port A to port B	10	53	124	-6	37	59	ns
		port B to port A	-36	-11	11	-7	37	60	ns
		SDAA; SDAB; V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V							
		port A to port B	7	39	97	-6	23	38	ns
		port B to port A	-30	-11	9	-5	26	43	ns
t_{PHL}	HIGH to LOW propagation delay	SCLA; SCLB; V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V							
		port A to port B	20	55	117	18	67	109	ns
		port B to port A	20	57	118	23	82	128	ns
		SDAA; SDAB; V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V							
		port A to port B	24	67	143	22	72	130	ns
		port B to port A	20	57	123	23	88	132	ns
$t_{TLH(in)}$	input LOW to HIGH transition time	SCLA, SCLB input; V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V							
		port A to port B	7	14	16	28	47	71	ns
		port B to port A	48	78	110	28	49	72	ns
		SDAA, SDAB input; V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V							
		port A to port B	7	14	16	28	47	69	ns
		port B to port A	48	75	112	28	48	74	ns

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C						Unit
			Port A: 10 pF Port B: 160 pF[1]			Port A: 85 pF Port B: 85 pF[2]			
			Min	Typ[3]	Max	Min	Typ[3]	Max	
$t_{TLH(out)}$	output LOW to HIGH transition time	SCLA, SCLB output; V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V							
		port A to port B	8	32	66	4	16	37	ns
		port B to port A	0	3	7	4	15	37	ns
		SDAA, SDAB output; V_{CCA} = 1.08 V to 3.6 V; V_{CCB} = 1.08 V to 3.6 V							
		port A to port B	7	25	54	3	14	33	ns
		port B to port A	0	3	6	3	13	33	ns
SR_f	falling slew rate	SCLA, SDAA outputs; V_{CCA} = 1.08 V to 3.6 V	-	0.040	0.350	-	0.040	0.265	V/ns
		SCLB, SDAB outputs; V_{CCB} = 1.08 V to 3.6 V	-	0.035	0.350	-	0.050	0.280	V/ns

[1] Times are specified with loads: 10 pF and 160 pF at the port A and port B, respectively; internal pull-up resistors (4.3 kΩ, typical) and external pull-up resistors (1.65 kΩ) are used for effective pull-up resistance of 1.2 kΩ at the port A and port B.
The pull-up voltages for the port A and port B are V_{CCA} and V_{CCB}, respectively. See Table 12 (configuration 1)
[2] Times are specified with loads: 85 pF and 85 pF at the port A and port B, respectively; internal pull-up resistors (4.3 kΩ, typical) and external pull-up resistors (1.65 kΩ) are used for effective pull-up resistance of 1.2 kΩ at the port A and port B.
The pull-up voltages for the port A and port B are V_{CCA} and V_{CCB}, respectively. See Table 12 (configuration 2)
[3] Typical values are measured at T_{amb} = 25 °C; V_{CCA} = 1.2 V; and V_{CCB} = 1.2 V; unless otherwise specified.
[4] FM+, FM and SM modes are fully supported for V_{CC} = 1.08 V to 3.6 V.

Table 10. Data set-up time gain

1.2 V to 1.2 V translation from port A to port B; at recommended operating conditions; voltages are referenced to GND (ground = 0 V); For test circuit see Fig. 9. .

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
$t_{gain(SU;DAT)}$	data set-up time gain	clock channel: port A to port B; data channel: port B to port A; see Fig. 9 [2]				
		$C_{L(A)}$ = 10 pF; $C_{L(B)}$ = 160 pF [3]	23	45	-	ns
		$C_{L(A)}$ = 85 pF; $C_{L(B)}$ = 85 pF [4]	85	104	-	ns

[1] Typical values are measured at T_{amb} = 25 °C
[2] Data from Table 10 hold also for the alternative signal flow direction,
that is: clock channel: port B to port A, data channel: port A to port B;
In this case, the values of the load capacitance at port A and port B should be exchanged.
[3] See Table 13, configuration 1 and configuration 2.
[4] See Table 13, configuration 1 and configuration 3.

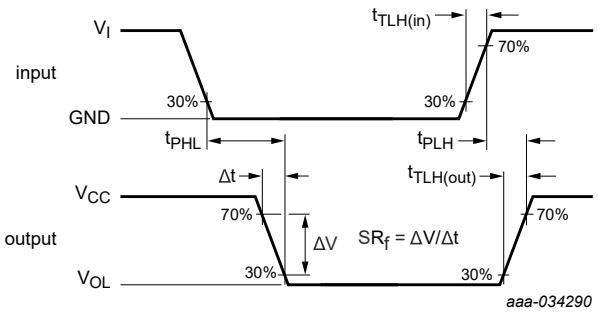
Table 11. Switching characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); For test circuit see Fig. 8. .

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
$t_{ramp-up}$	supply ramp-up time	V_{CCA}; V_{CCB}; see Fig. 11 (A)	30	-	-	µs
t_{en}	enable time	EN; see Fig. 11 (B)	-	450	1100	ns
t_{dis}	disable time	EN; see Fig. 11 (B)	-	100	150	ns

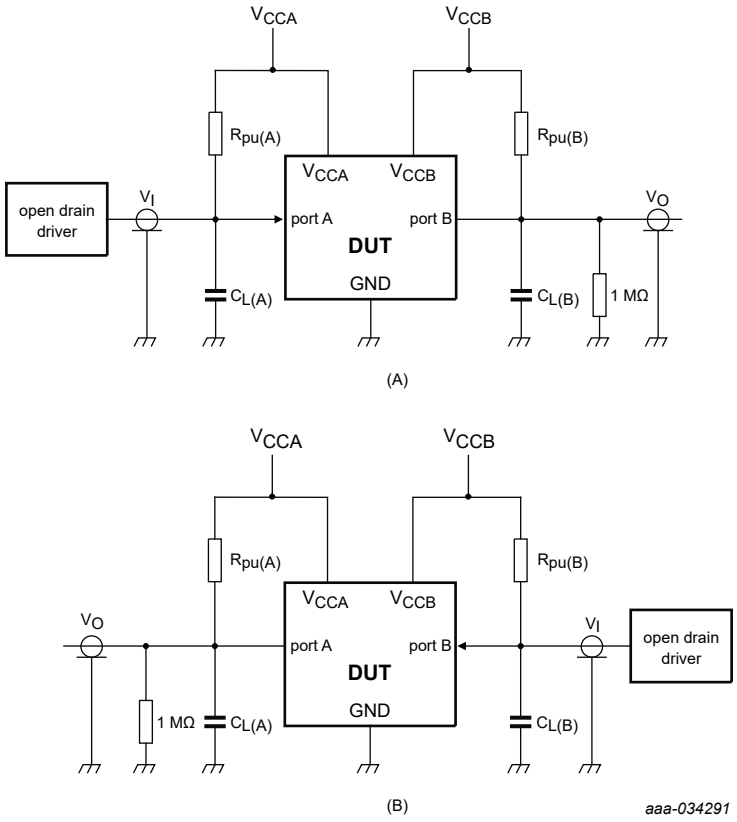
[1] Typical values are measured at V_{CCA} = 1.2 V and V_{CCB} = 1.2 V at T_{amb} = 25 °C

12.1. Waveforms and test circuits



V_{OL} is the typical output voltage level that occur with the output load.

Fig. 7. The port A to port B and port B to port A propagation delay times, input/output transition times and slew rate



The test circuits are used in two configurations with their parameters as described in Table 12.

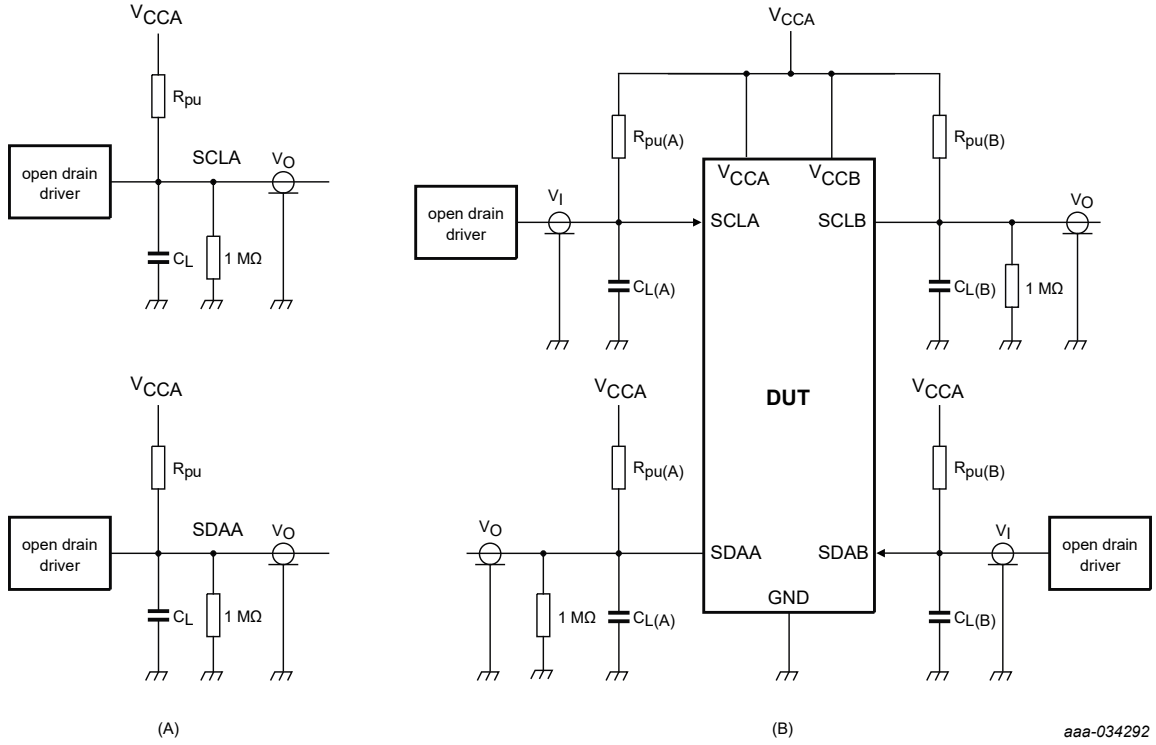
(A) from A to B

(B) from B to A

Fig. 8. Test circuits for dynamic parameters measurements

Table 12. Test circuit configurations for the NCA9700 dynamic parameters measurements

Configuration	Supplies	Bus capacitance	Pull-up resistance
1	V_{CCA} = 1.2 V V_{CCB} = 1.2 V	$C_{L(A)}$ = 10 pF $C_{L(B)}$ = 160 pF	$R_{pu(A)}$ = 1.65 kΩ $R_{pu(B)}$ = 1.65 kΩ
2	V_{CCA} = 1.08 V V_{CCB} = 2.5 V	$C_{L(A)}$ = 85 pF $C_{L(B)}$ = 85 pF	$R_{pu(A)}$ = 1.65 kΩ $R_{pu(B)}$ = 1.65 kΩ

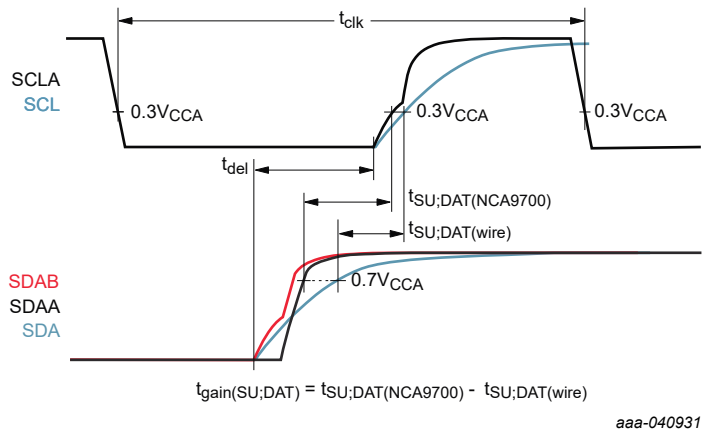


The test circuits are used in two configurations with their parameters as described in Table 13.
(A) set-up without an I²C repeater (the reference)
(B) set-up with the NCA9700 as the DUT

Fig. 9. Test circuits for the data set-up time gain measurement

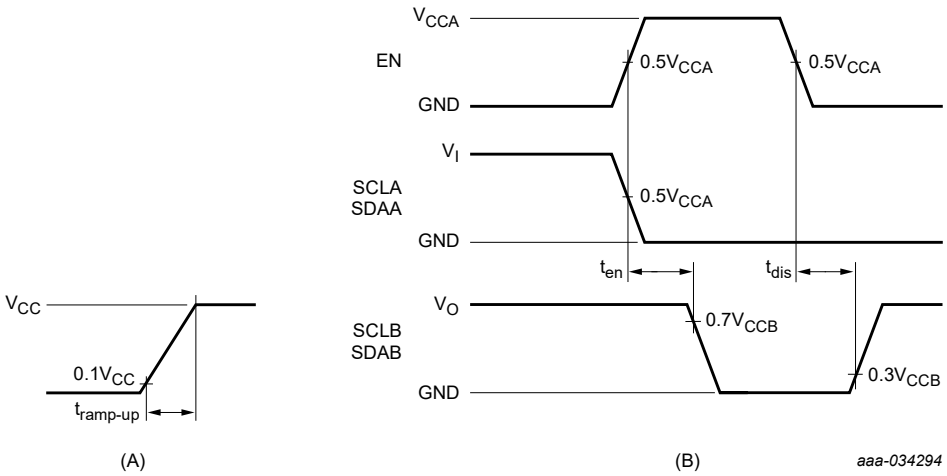
Table 13. Test circuit configurations for the NCA9700 data set-up time gain parameters measurements

Configuration	Supplies	Bus capacitance	Pull-up resistance
1; see Fig. 9 (A)	V_{CCA} = 1.2 V	C_L = 170 pF	R_{pu} = 1.2 kΩ (4.3 kΩ||1.65 kΩ)
2; see Fig. 9 (B)	V_{CCA} = 1.2 V V_{CCB} = 1.2 V	$C_{L(A)}$ = 10 pF $C_{L(B)}$ = 160 pF	$R_{pu(A)}$ = 1.65 kΩ $R_{pu(B)}$ = 1.65 kΩ
3; see Fig. 9 (B)	V_{CCA} = 1.2 V V_{CCB} = 1.2 V	$C_{L(A)}$ = 85 pF $C_{L(B)}$ = 85 pF	$R_{pu(A)}$ = 1.65 kΩ $R_{pu(B)}$ = 1.65 kΩ



t_{del} is an arbitrary delay between the input data and clock signals; Here: t_{del} = 300 ns.

Fig. 10. The definition of the data set-up time gain



(A) ramp-up time (V_{CC} = V_{CCA} or V_{CCB})

(B) enable and disable times (the HIGH-to-LOW transition on port A pins is synchronized with the detected LOW-to-HIGH transition on the EN pin)

Fig. 11. The definitions of ramp-up time and enable and disable times

13. Application information

Fig. 12 shows a generic application schematic of the NCA9700. The NCA9700 is placed between the I²C Master and I²C Slave, both operating with the clock frequency of 1 MHz. The supplies V_{CCA} and V_{CCB} can be the same or different; the external pull-up resistors can be present or absent; the pull-up resistors can be all of the same value or different. As shown in the figure, the EN pin is driven by the I²C Master. However, it can also be left unconnected (it will be pulled up internally) or tied externally to the V_{CCA} supply.

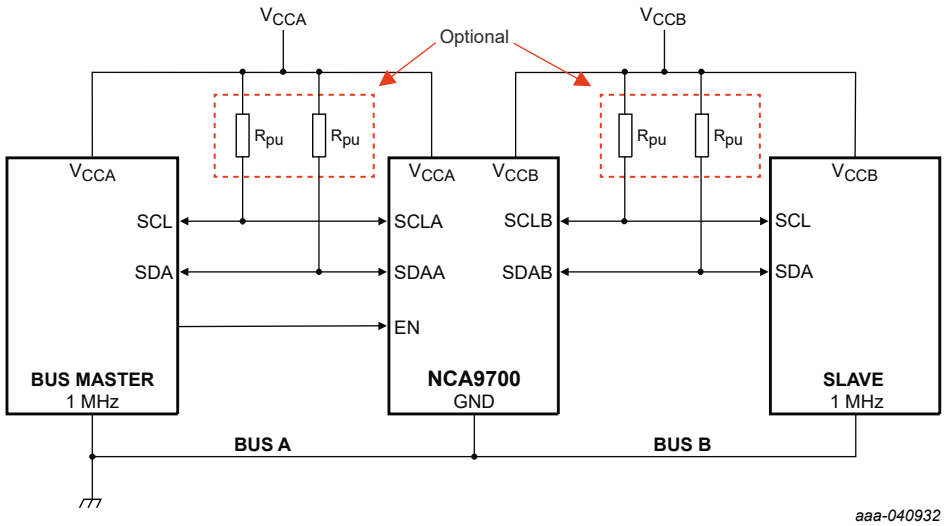


Fig. 12. Typical application of the NCA9700

An application example of the NCA9700 in a single-rail system with the 1.2 V supply is shown in Fig. 13. There is no signal level translation here. The external 1.65 kΩ pull-up resistors (giving effective nominal pull-up resistance of 1.2 kΩ) are used at buses A and B to improve the I²C signal timing. This application example corresponds to the first set-up (Table 12; configuration 1) for which the NCA9700 parameters listed in Table 9 are measured; the port A and port B load capacitances are 10 pF and 160 pF, respectively.

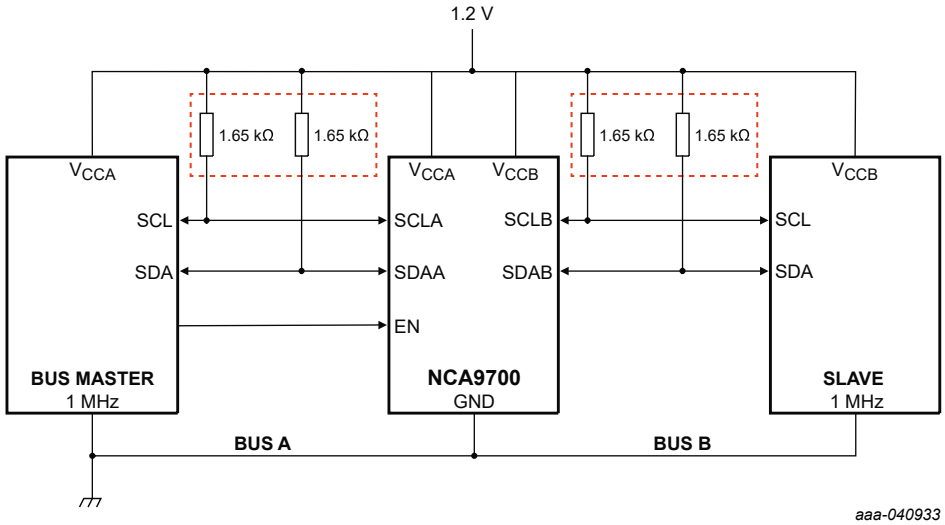


Fig. 13. The application example of the NCA9700 in a single-rail system with the 1.2 V supply

In Fig. 14, the application example of the NCA9700 as a voltage translating buffer is shown. The signal levels are up-converted from 1.0 V to 2.5 V. The external pull-up resistors are omitted implying that the bus pull-up is taken care by the internal pull-up resistors only, even if the NCA9700 is disabled.

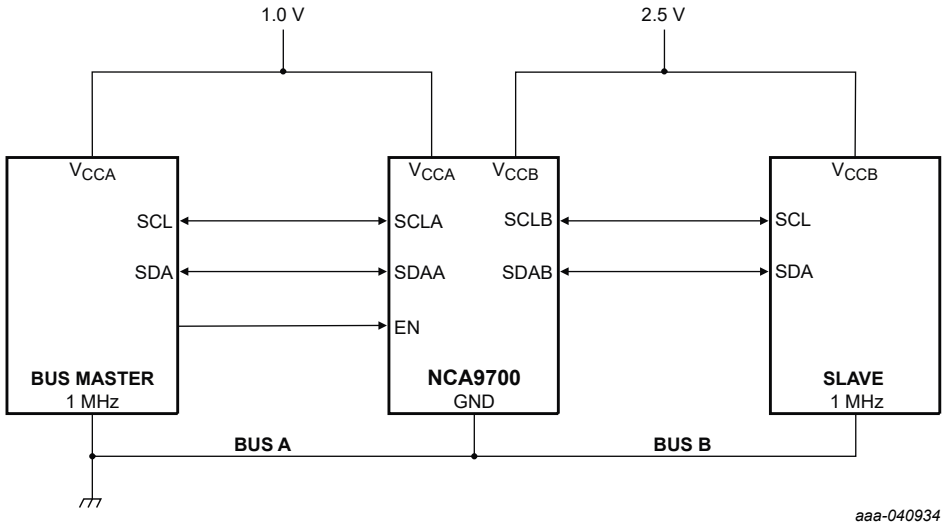


Fig. 14. The application example of the NCA9700 in a system with the up-level voltage translation from 1.0 V to 2.5 V

Multiple NCA9700 repeaters can be connected in series or in star with full flexibility on how the connections between the repeaters are realized. For example, port B of the first NCA9700 can be connected to port A or port B of the second NCA9700, etc. If the clock stretching is used, port B of the first NCA9700 must be connected to port A of the second NCA9700, and so on. Also, the I²C Master must always be connected to port A of the first NCA9700 and the I²C Slave to port B of the last NCA9700.

For certain bus capacitances there are recommended pull-up resistances, see Table 14

Table 14. Recommended pull-up resistance

C_{bus} (pF)	R_{pu} (Ω)
85	3000
160	1650
400	600

14. Power supply recommendations

For the correct operation of the NCA9700, the supply voltages on the V_{CCA} and V_{CCB} pins must always be within the recommended operating voltage range. For both pins, the range is the same and equals 1.08 V to 3.6 V. Furthermore, there are no restrictions for the selection of the supply voltages of the V_{CCA} and V_{CCB} pins as long as they are from the recommended voltage range. So the V_{CCA} voltage may be greater, equal, or smaller than the V_{CCB} voltage.

At the IC power up, one must assure that the supplies ramp up time complies with $t_{ramp-up}$ parameter (see Table 11). There are no supply sequencing requirements for the NCA9700. So, the supply for port A can be provided before, after, or at the same time as the supply for port B.

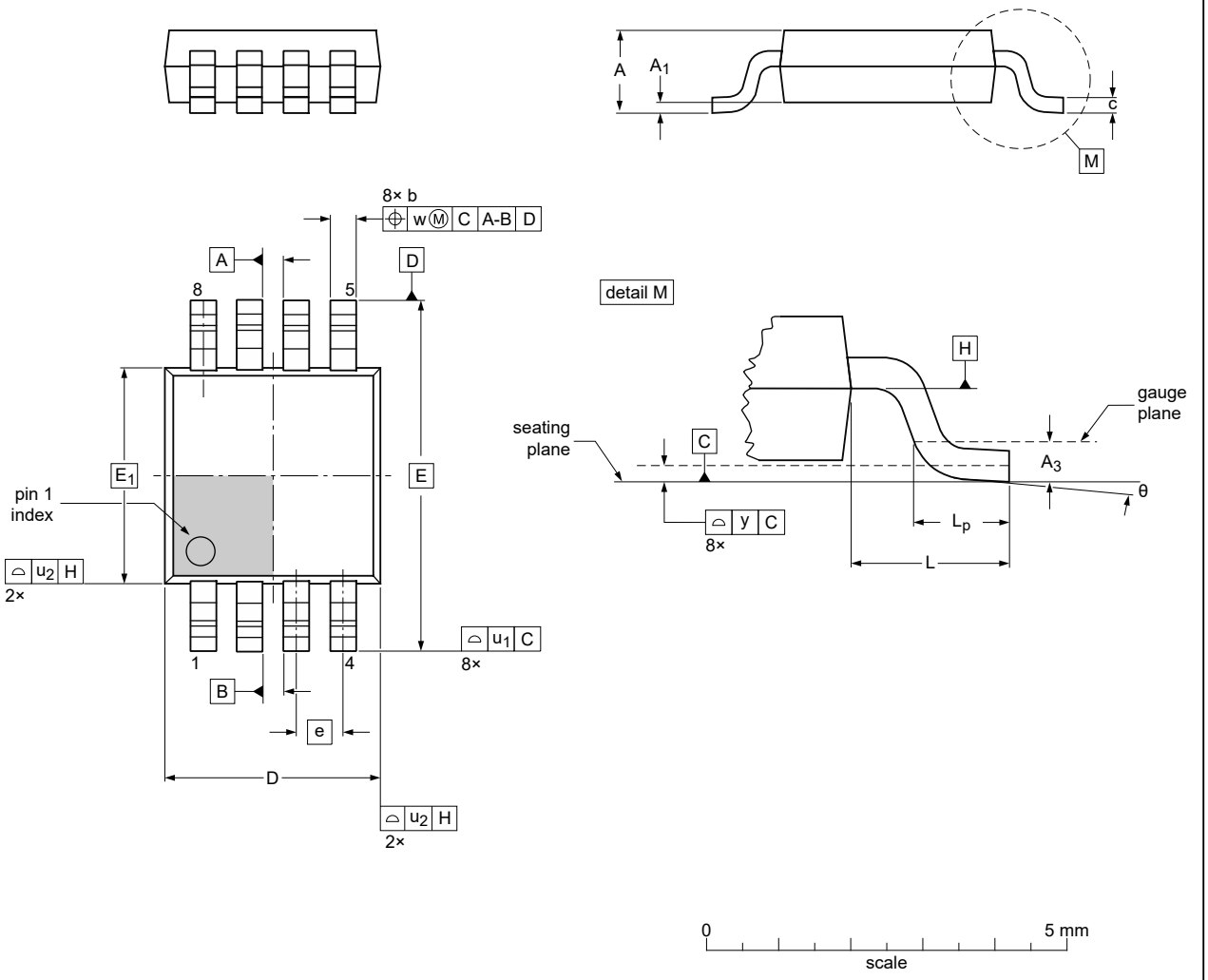
The supply start up level (V_{start}) defines the voltage at which the NCA9700 gets activated and starts drawing current. The supply under-voltage level (V_{UVLO}) defines the voltage at which the NCA9700 is deactivated and becomes nearly currentless.[3] Though the NCA9700 supply start level is lower than the minimal operating supply voltage, the correct operation of the NCA9700 and the NCA9700 parameters are guaranteed only for the supplies within the recommended supply voltage range.

It is recommended to use decoupling capacitors of value 0.1 µF or 1 µF for the V_{CCA} and V_{CCB} supplies. They should be placed as close as possible to the V_{CCA} and V_{CCB} pins of the IC to reduce current loops.

3 In the supply under-voltage, the IC current of port A or port B is in the nA-range and depends on V_{CCA} and V_{CCB} supplies, respectively.

15. Package outline

TSSOP8: plastic, thin shrink small outline package; 8 leads; 0.65 mm pitch; 3 mm × 3 mm × 1.1 mm body **SOT505-3**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_3	b	c	$D^{(1)}$	E	$E_1^{(2)}$	e	L	L_p	u_1	u_2	w	y	θ
mm	max	1.1	0.15	0.25 BSC	0.45	0.28	3.0 BSC	4.9 BSC	3.00 BSC	0.65 BSC	0.94 REF	0.7	0.25	0.2	0.13	0.1	6°
	nom		0.10		0.35												
	min		0.05		0.25	0.15						0.4					0°

Notes:
1. Plastic protrusions or gate burrs of 0.15 mm maxmimum per end are not included for dimension D.
2. Plastic protrusions or interlead flash of 0.25 mm maximum per end are not included for dimension E_1.
3. D and E_1 dimensions are determined at datum H.

sot505-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT505-3						23-11-22

Fig. 15. Package outline SOT505-3 (TSSOP8)

16. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
I²C	Inter-Integrated Circuit
PCB	Printed Circuit Board
PMBus	Power Management Bus
PRR	Pulse Rate Repetition
SMBus	System Management Bus

17. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCA9700 v.1	20240910	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 10 September 2024

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