74LV4052

Dual 4-channel analog multiplexer/demultiplexer

Rev. 7 — 29 March 2024 Product data sheet

1. General description

The 74LV4052 is a dual single-pole quad-throw analog switch suitable for use in 4:1 multiplexer/demultiplexer applications. Each switch features four independent inputs/outputs (nY0, nY1, nY2 and nY3) and a common input/output (nZ). A digital enable input ($\overline{E}$) and two digital select inputs (S0, S1) are common to both switches. When $\overline{E}$ is HIGH, the switches are turned off. Digital inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC}.

2. Features and benefits

- Wide supply voltage range from 1.0 to 6.0 V
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Optimized for low-voltage applications: 1.0 V to 6.0 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low ON resistance:
  - 145 Ω (typical) at V_{CC} - V_{EE} = 2.0 V
  - 90 Ω (typical) at V_{CC} - V_{EE} = 3.0 V
  - 60 Ω (typical) at V_{CC} - V_{EE} = 4.5 V
- Logic level translation:
  - To enable 3 V logic to communicate with ± 3 V analog signals
- Typical ‘break before make’ built in
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4052D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4052PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

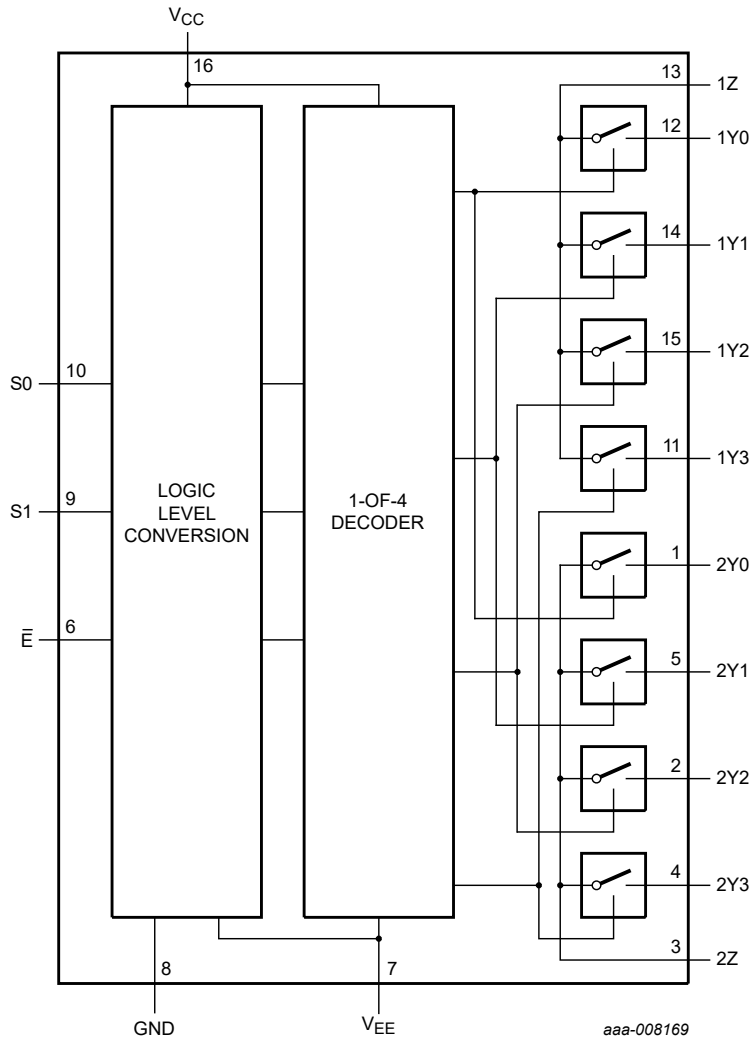


Fig. 1. Functional diagram

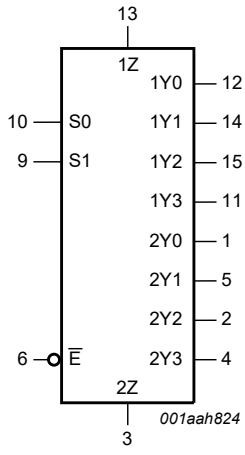


Fig. 2. Logic symbol

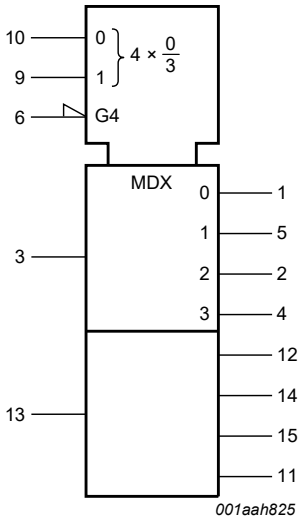


Fig. 3. IEC logic symbol

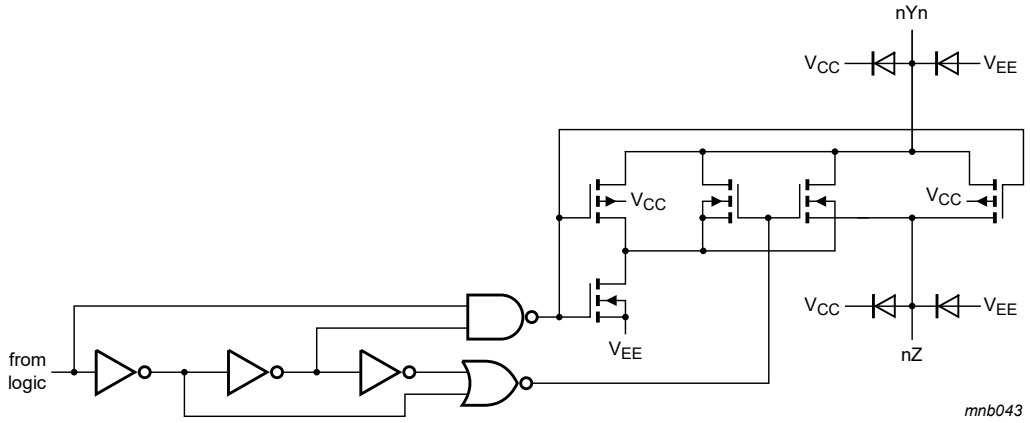
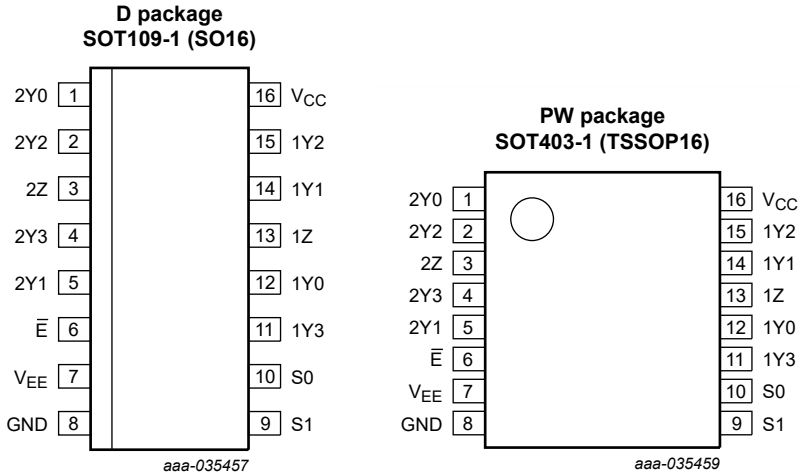


Fig. 4. Schematic diagram (one switch)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0, 2Y1, 2Y2, 2Y3	1, 5, 2, 4	independent input or output
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	negative supply voltage
GND	8	ground (0 V)
S0, S1	10, 9	select logic input
1Y0, 1Y1, 1Y2, 1Y3	12, 14, 15, 11	independent input or output
1Z, 2Z	13, 3	common input or output
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input			Channel on
$\overline{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage		[1]	-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	[2]	-	±20	mA
I_{SK}	switch clamping current	V_{SW} < -0.5 V or V_{SW} > V_{CC} + 0.5 V	[2]	-	±20	mA
I_{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; source or sink current	[2]	-	±25	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[3]	-	500	mW

[1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current flows out of terminals nYn. In this case, there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE}.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	see Fig. 5	[1]	1	3.3	6	V
V_I	input voltage			0	-	V_{CC}	V
V_{SW}	switch voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 6.0 V		-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to 6.0 V. However, LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

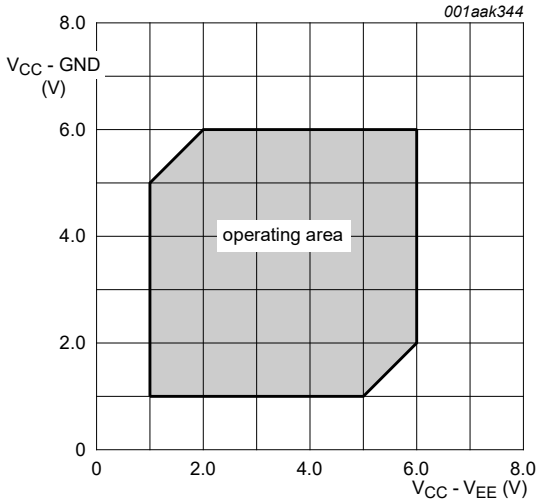


Fig. 5. Guaranteed operating area as a function of the supply voltages

9. Static characteristics

Table 6. Static characteristics

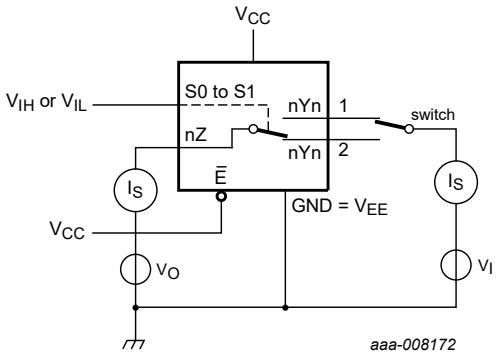
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V	3.15	-	-	3.15	-	V
		V_{CC} = 6.0 V	4.20	-	-	4.20	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V	-	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.80	-	1.80	V
I_I	input leakage current	V_I = V_{CC} or GND						
		V_{CC} = 3.6 V	-	-	1.0	-	1.0	µA
		V_{CC} = 6.0 V	-	-	2.0	-	2.0	µA
$I_{S(OFF)}$	OFF-state leakage current	V_I = V_{IH} or V_{IL}; see Fig. 6						
		V_{CC} = 3.6 V	-	-	1.0	-	1.0	µA
		V_{CC} = 6.0 V	-	-	2.0	-	2.0	µA
$I_{S(ON)}$	ON-state leakage current	V_I = V_{IH} or V_{IL}; see Fig. 7						
		V_{CC} = 3.6 V	-	-	1.0	-	1.0	µA
		V_{CC} = 6.0 V	-	-	2.0	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A						
		V_{CC} = 3.6 V	-	-	20	-	40	µA
		V_{CC} = 6.0 V	-	-	40	-	80	µA
ΔI_{CC}	additional supply current	per input; V_I = V_{CC} - 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	pF
C_{sw}	switch capacitance	independent pins nYn	-	5	-	-	-	pF
		common pins nZ	-	12	-	-	-	pF

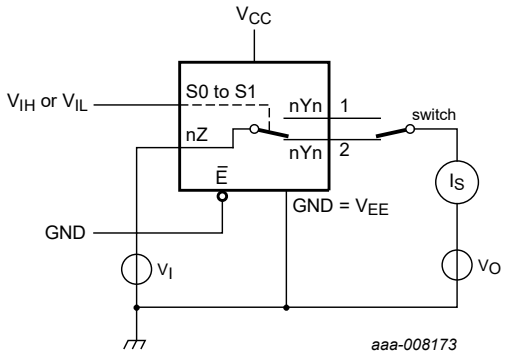
[1] Typical values are measured at T_{amb} = 25 °C.

9.1. Test circuits



$V_I = V_{CC}$ or V_{EE} and $V_O = V_{EE}$ or V_{CC}.

Fig. 6. Test circuit for measuring OFF-state leakage current



$V_I = V_{CC}$ or V_{EE} and V_O = open circuit.

Fig. 7. Test circuit for measuring ON-state leakage current

9.2. ON resistance

Table 7. ON resistance

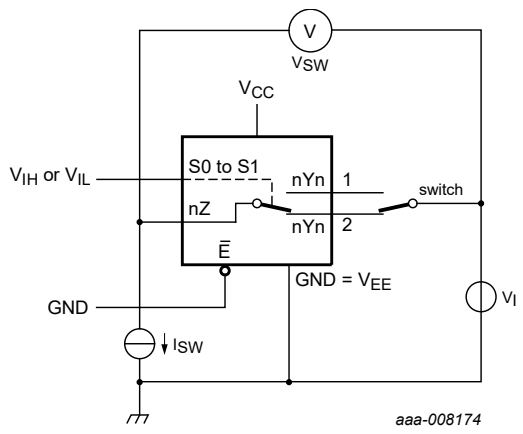
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit and graph see Fig. 8 and Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = 0 V to V_{CC} - V_{EE}						
		V_{CC} = 1.2 V; I_{SW} = 100 µA [2]	-	-	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 µA	-	145	325	-	375	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 µA	-	90	200	-	235	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 µA	-	80	180	-	210	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 µA	-	60	135	-	160	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 µA	-	55	125	-	145	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0 V to V_{CC} - V_{EE}						
		V_{CC} = 1.2 V; I_{SW} = 100 µA [2]	-	-	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 µA	-	5	-	-	-	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 µA	-	4	-	-	-	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 µA	-	4	-	-	-	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 µA	-	3	-	-	-	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 µA	-	2	-	-	-	Ω

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND						
		V_{CC} = 1.2 V; I_{SW} = 100 µA [2]	-	225	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 µA	-	110	235	-	270	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 µA	-	70	145	-	165	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 µA	-	60	130	-	150	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 µA	-	45	100	-	115	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 µA	-	40	85	-	100	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = V_{CC} - V_{EE}						
		V_{CC} = 1.2 V; I_{SW} = 100 µA [2]	-	250	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 µA	-	120	320	-	370	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 µA	-	75	195	-	225	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 µA	-	70	175	-	205	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 µA	-	50	130	-	150	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 µA	-	45	120	-	135	Ω

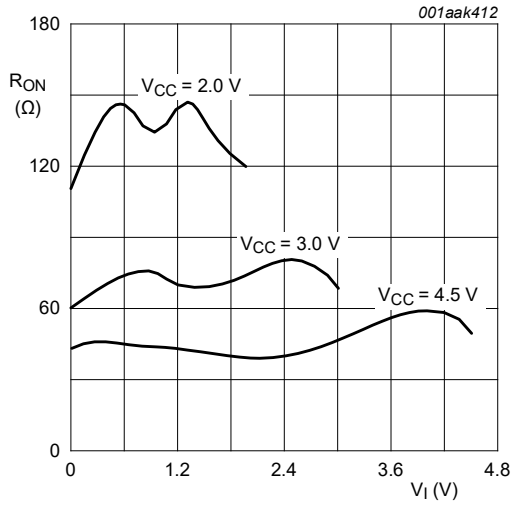
[1] Typical values are measured at T_{amb} = 25 °C.
[2] When supply voltages (V_{CC} - V_{EE}) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, only use these devices for transmitting digital signals.

9.3. On resistance test circuit and graph



R_{ON} = V_{SW} / I_{SW}.

Fig. 8. Test circuit for measuring R_{ON}



V_i = 0 V to V_{CC} - V_{EE}

Fig. 9. Typical R_{ON} as a function of input voltage

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 12.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nYn to nZ, nZ to nYn; see Fig. 10 [2]						
		V_{CC} = 1.2 V	-	25	-	-	-	ns
		V_{CC} = 2.0 V	-	9	17	-	20	ns
		V_{CC} = 2.7 V	-	6	13	-	15	ns
		V_{CC} = 3.0 V to 3.6 V [3]	-	5	10	-	12	ns
		V_{CC} = 4.5 V	-	4	9	-	10	ns
		V_{CC} = 6.0 V	-	3	7	-	8	ns
t_{en}	enable time	$\overline{E}$, Sn to nYn, nZ; see Fig. 11 [2]						
		V_{CC} = 1.2 V	-	190	-	-	-	ns
		V_{CC} = 2.0 V	-	65	121	-	146	ns
		V_{CC} = 2.7 V	-	48	89	-	108	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF [3]	-	30	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V [3]	-	36	71	-	86	ns
		V_{CC} = 4.5 V	-	32	60	-	73	ns
		V_{CC} = 6.0 V	-	25	46	-	56	ns
t_{dis}	disable time	$\overline{E}$, Sn to nYn, nZ; see Fig. 11 [2]						
		V_{CC} = 1.2 V	-	125	-	-	-	ns
		V_{CC} = 2.0 V	-	43	80	-	95	ns
		V_{CC} = 2.7 V	-	33	59	-	71	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF [3]	-	22	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V [3]	-	26	48	-	57	ns
		V_{CC} = 4.5 V	-	23	41	-	49	ns
		V_{CC} = 6.0 V	-	18	32	-	38	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [4]	-	57	-	-	-	pF

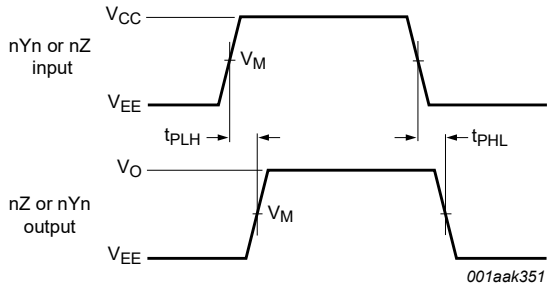
[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma((C_L + C_{sw}) \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz, f_o = output frequency in MHz
C_L = output load capacitance in pF
C_{sw} = maximum switch capacitance in pF;
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

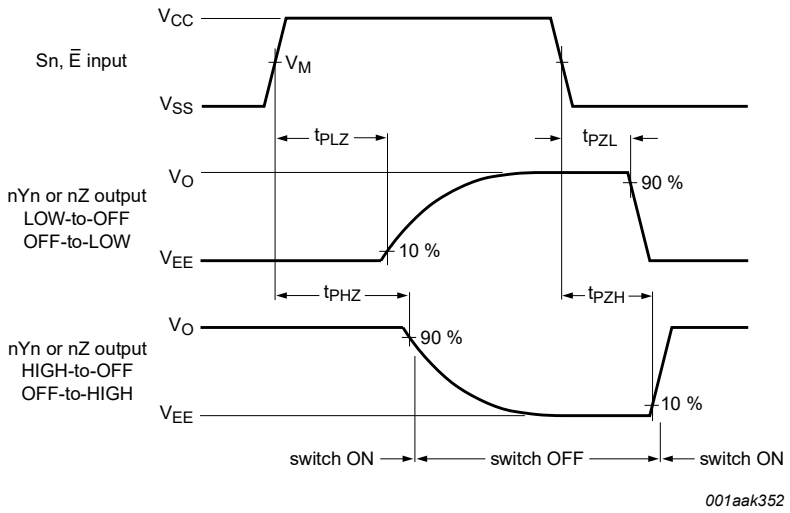
10.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 10. nYn, nZ to nZ, nYn propagation delays



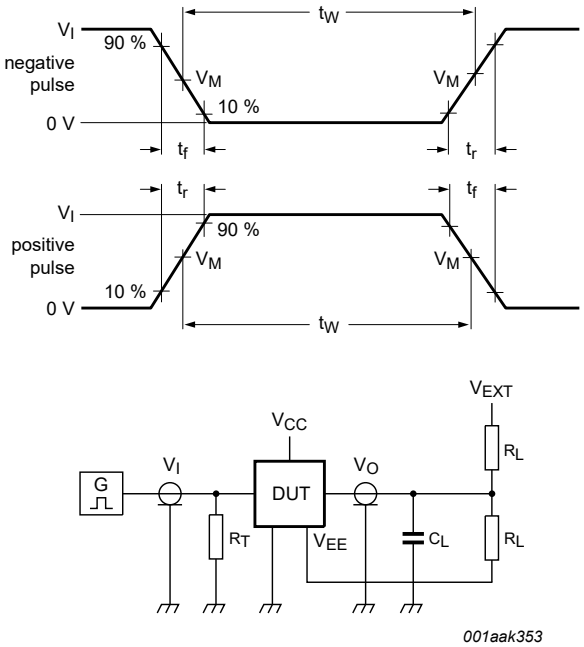
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 11. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
> 3.6 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 12. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 6 ns	50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 6 ns	15 pF, 50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$
> 3.6 V	V_{CC}	≤ 6 ns	50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$

10.2. Additional dynamic parameters

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 6.0$ ns; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; C_L = 50 pF; R_L = 10 kΩ; see Fig. 13				
		V_{CC} = 3.0 V; V_I = 2.75 V (p-p)	-	0.8	-	%
		V_{CC} = 6.0 V; V_I = 5.5 V (p-p)	-	0.4	-	%
		f_i = 10 kHz; C_L = 50 pF; R_L = 10 kΩ; see Fig. 13				
		V_{CC} = 3.0 V; V_I = 2.75 V (p-p)	-	2.4	-	%
		V_{CC} = 6.0 V; V_I = 5.5 V (p-p)	-	1.2	-	%
$f_{(-3dB)}$	-3 dB frequency response	C_L = 50 pF; R_L = 50 Ω; see Fig. 14 and Fig. 15 [1]				
		V_{CC} = 3.0 V	-	180	-	MHz
		V_{CC} = 6.0 V	-	200	-	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{iso}	isolation (OFF-state)	f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Fig. 16 and Fig. 17 [2]				
		V_{CC} = 3.0 V	-	-50	-	dB
		V_{CC} = 6.0 V	-	-50	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Fig. 18				
		V_{CC} = 3.0 V	-	0.11	-	V
		V_{CC} = 6.0 V	-	0.12	-	V
Xtalk	crosstalk	between switches; f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Fig. 19 [2]				
		V_{CC} = 3.0 V	-	-60	-	dB
		V_{CC} = 6.0 V	-	-60	-	dB

[1] To obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50 Ω), adjust f_i voltage.
[2] To obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600 Ω), adjust f_i voltage.

10.2.1. Test circuits

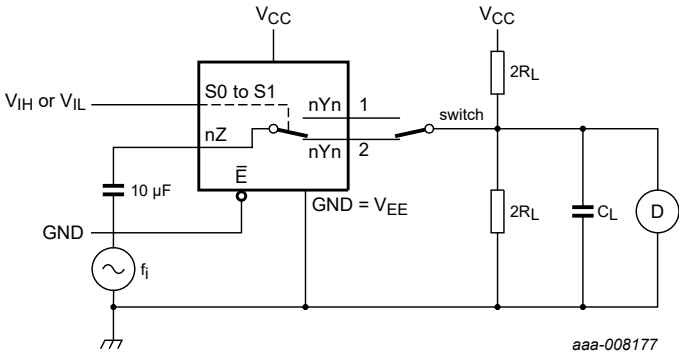


Fig. 13. Test circuit for measuring total harmonic distortion

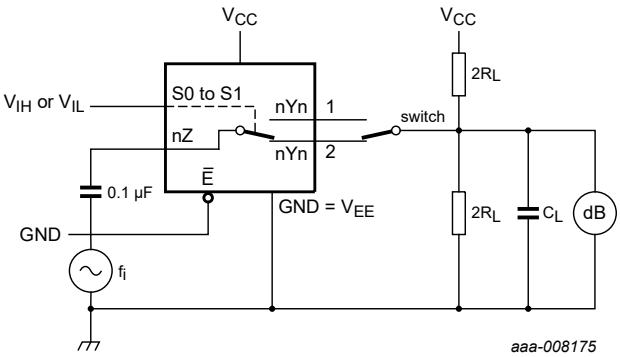
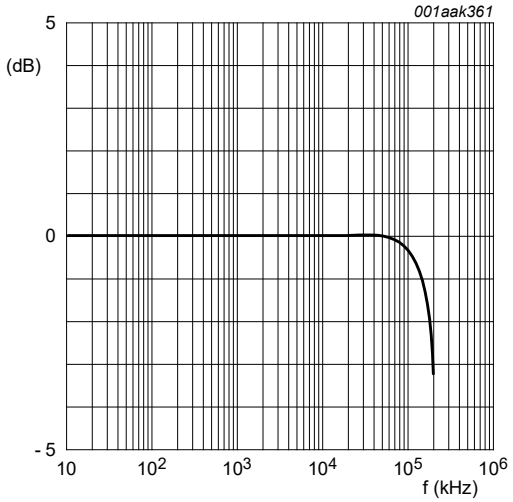


Fig. 14. Test circuit for measuring frequency response



V_{CC} = 3.0 V; GND = 0 V; V_{EE} = - 3.0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig. 15. Typical frequency response

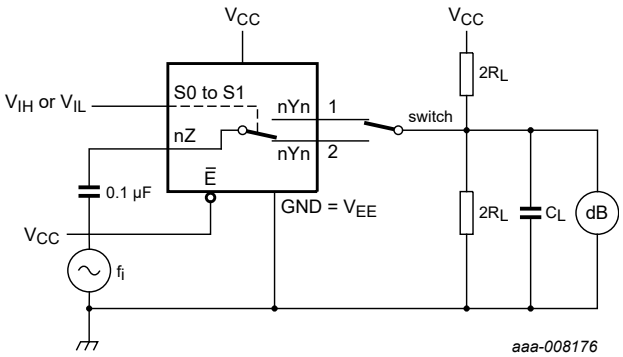
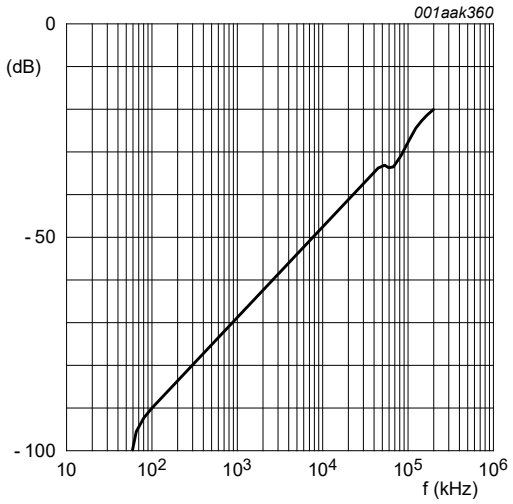
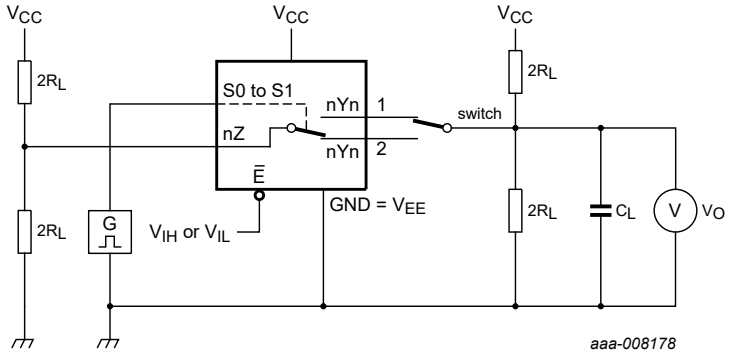


Fig. 16. Test circuit for measuring isolation (OFF-state)

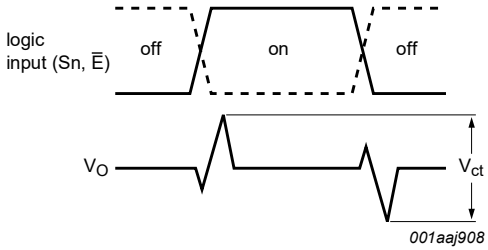


V_{CC} = 3.0 V; GND = 0 V; V_{EE} = - 3.0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig. 17. Typical isolation (OFF-state) as function of frequency



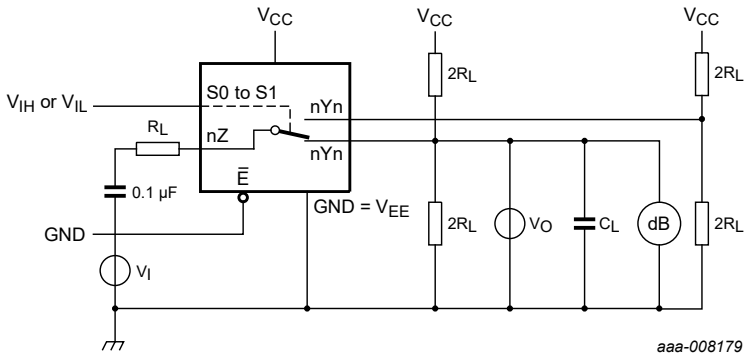
a. Test circuit



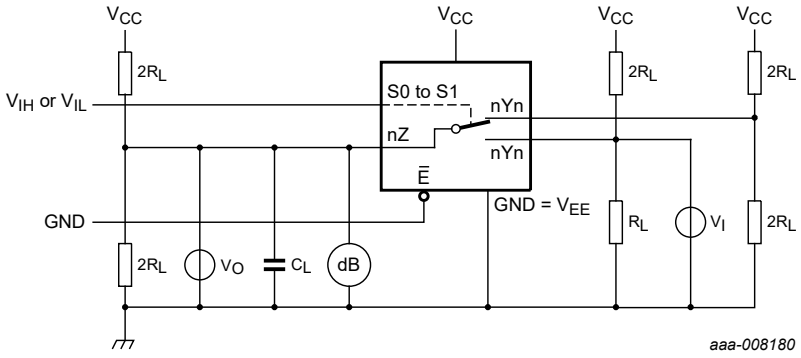
b. Input and output pulse definitions

V_I may be connected to Sn or $\overline{E}$.

Fig. 18. Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch on channel.

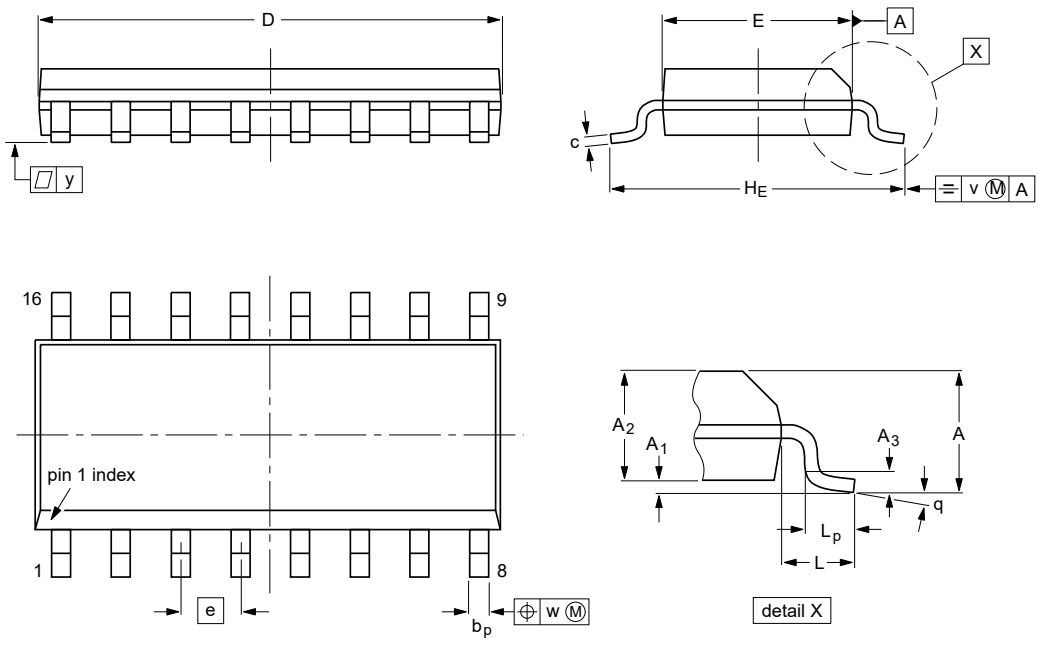


b. Switch off channel.

Fig. 19. Test circuit for measuring crosstalk between switches

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

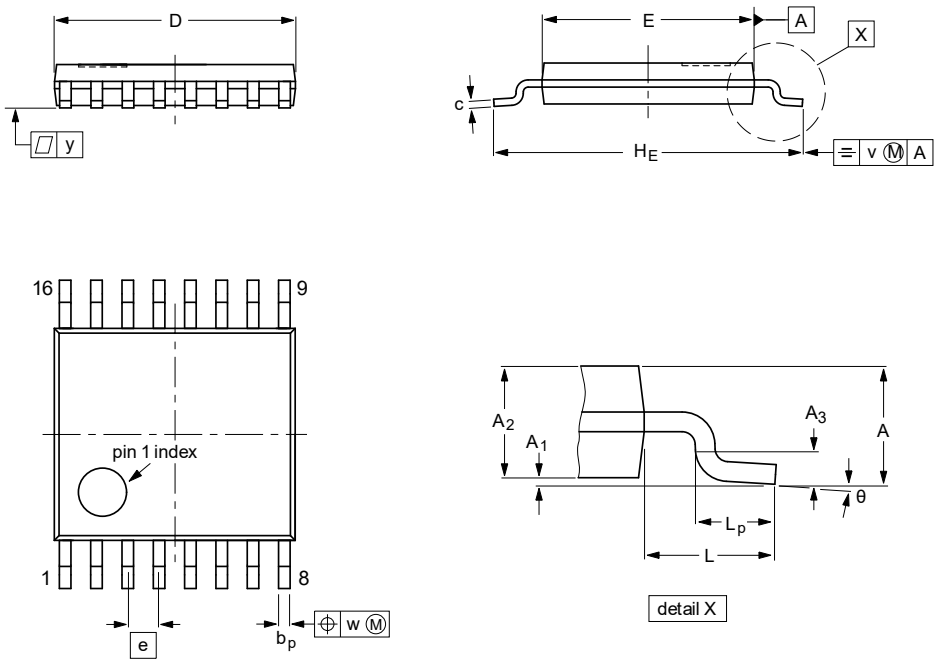
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

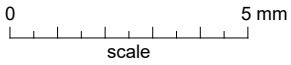
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 20. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 21. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4052 v.7	20240329	Product data sheet	-	74LV4052 v.6
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 20 and Fig. 21: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LV4052 v.6	20210924	Product data sheet	-	74LV4052 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated. • Type number 74LV4052DB (SOT338-1/SSOP16) removed.			
74LV4052 v.5	20160317	Product data sheet	-	74LV4052 v.4
Modifications:	• Type number 74LV4052N (SOT38-4) removed.			
74LV4052 v.4	20130701	Product data sheet	-	74LV4052 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74LV4052 v.3	19980623	Product specification	-	74LV4052 v.2
74LV4052 v.2	19970715	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 29 March 2024

单击下面可查看定价，库存，交付和生命周期等信息

>>Nexperia(安世)