

74HC4046A-Q100

Phase-locked loop with VCO

Rev. 3 — 19 February 2024

Product data sheet

1. General description

The 74HC4046A-Q100 is a high-speed Si-gate CMOS device. It is specified in compliance with JEDEC standard no 7A.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Low power consumption
- VCO-Inhibit control for ON/OFF keying and for low standby power consumption
- Center frequency up to 17 MHz (typical) at $V_{CC} = 4.5\text{ V}$
- Choice of three phase comparators:
 - PC1: EXCLUSIVE-OR
 - PC2: Edge-triggered J-K flip-flop
 - PC3: Edge-triggered RS flip-flop
- Excellent Voltage Controlled Oscillator (VCO) linearity
- Low frequency drift with supply voltage and temperature variations
- Operating power supply voltage range:
 - VCO section 3.0 V to 6.0 V
 - Digital section 2.0 V to 6.0 V
- Zero voltage offset due to operational amplifier buffering
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Applications

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
74HC4046APW-Q100	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Block diagram

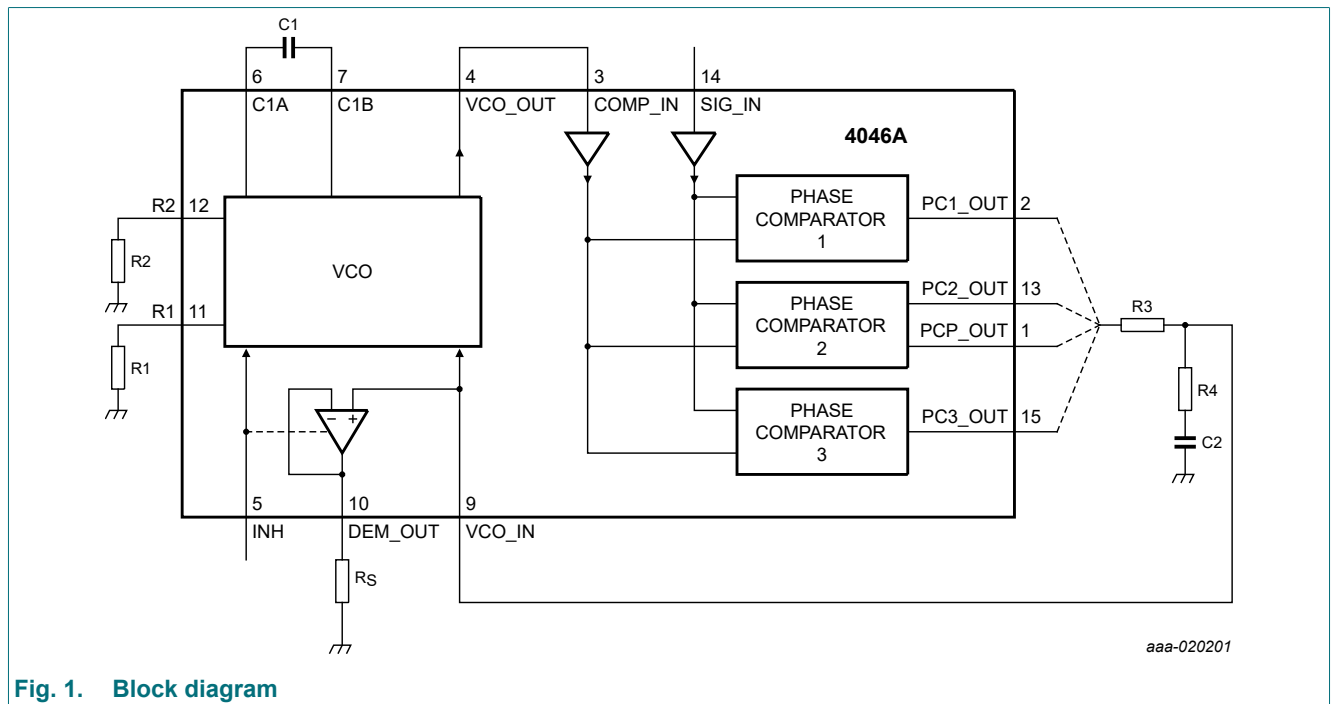


Fig. 1. Block diagram

6. Functional diagram

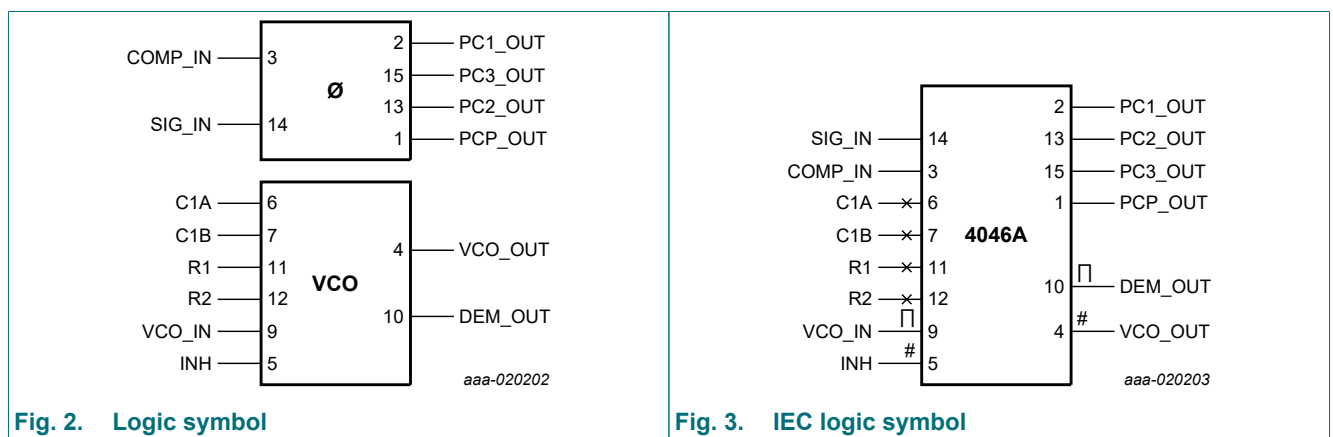


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

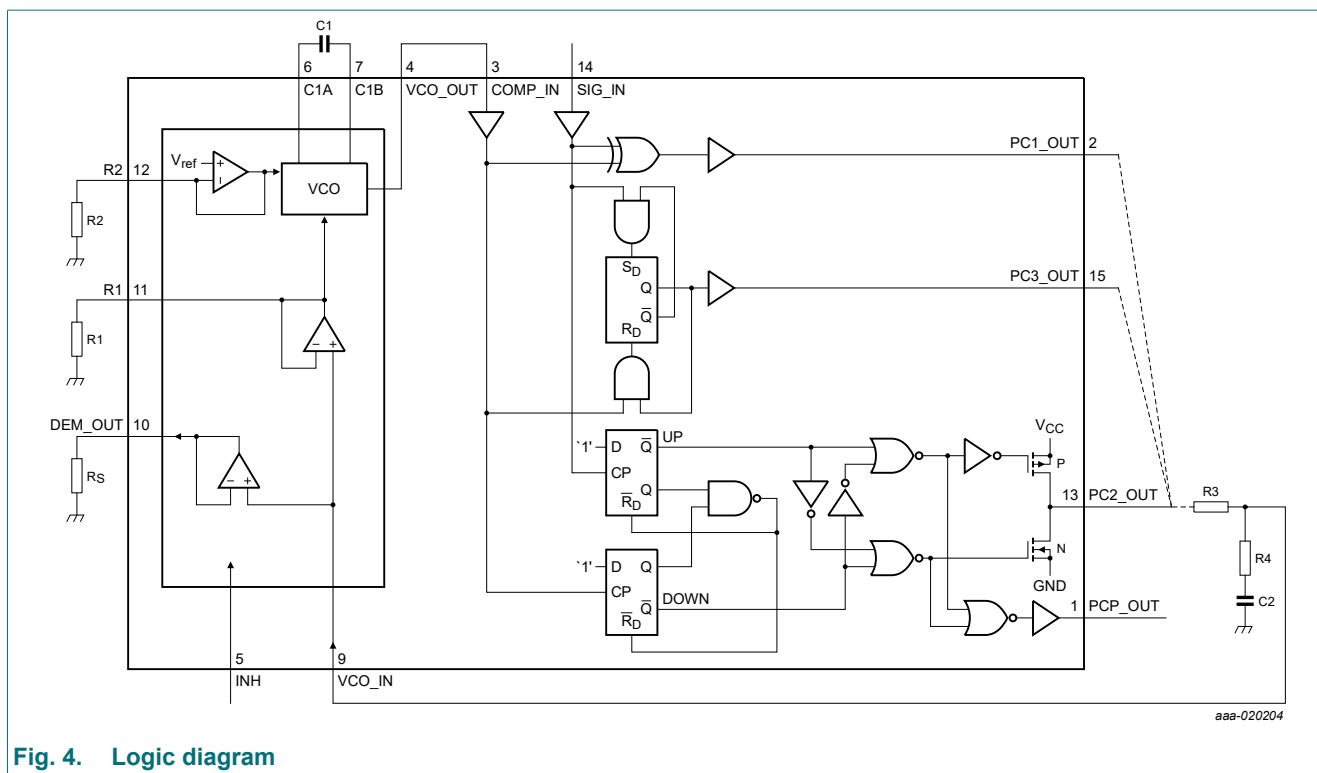
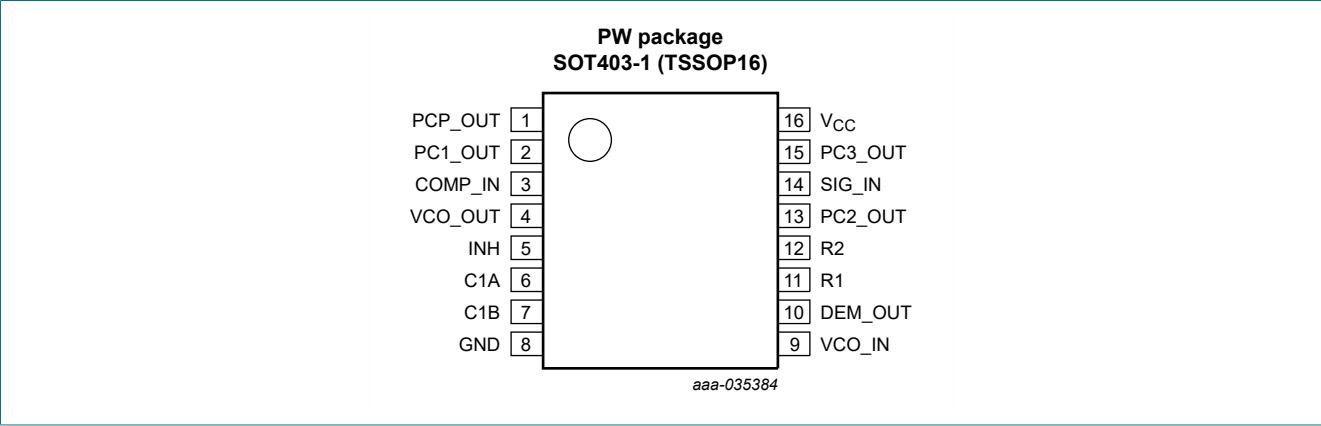


Fig. 4. Logic diagram

7. Pinning information

7.1. Pinning



7.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
PCP_OUT	1	phase comparator pulse output
PC1_OUT	2	phase comparator 1 output
COMP_IN	3	comparator input
VCO_OUT	4	VCO output
INH	5	inhibit input
C1A	6	capacitor C1 connection A
C1B	7	capacitor C1 connection B
GND	8	ground (0 V)
VCO_IN	9	VCO input
DEM_OUT	10	demodulator output
R1	11	resistor R1 connection
R2	12	resistor R2 connection
PC2_OUT	13	phase comparator 2 output
SIG_IN	14	signal input
PC3_OUT	15	phase comparator 3 output
V _{CC}	16	supply voltage

8. Functional description

The 74HC4046A-Q100 is a phase-locked-loop circuit that comprises a linear VCO and three different phase comparators (PC1, PC2 and PC3). It has a common signal input amplifier and a common comparator input (see Fig. 1). The signal input can be directly coupled to a large voltage signal, or indirectly coupled (with a series capacitor) to a small voltage signal. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 74HC4046A-Q100 forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op amp techniques.

8.1. VCO

The VCO requires one external capacitor C1 (between pins C1A and C1B) and one external resistor R1 (between pins R1 and GND). Alternatively, it requires two external resistors R1 and R2 (between pins R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if necessary (see Fig. 4).

The high input impedance of the VCO simplifies the design of the low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin DEM_OUT. In contrast to conventional techniques, where the DEM_OUT voltage is one threshold voltage lower than the VCO input voltage, the DEM_OUT voltage equals the VCO input. If DEM_OUT is used, a series resistor (R_s) should be connected from pin DEM_OUT to GND. If unused, DEM_OUT should be left open. The VCO output (pin VCO_OUT) can be connected directly to the comparator input (pin COMP_IN) or connected via a frequency divider. When the VCO input DC level is held constant, the VCO output signal has a duty cycle of 50 % (maximum expected deviation 1 %). A LOW-level at the inhibit input (pin INH) enables the VCO and demodulator, while a HIGH-level turns off both to minimize standby power consumption.

8.2. Phase comparators

The input signal can be coupled to the self-biasing amplifier at pin SIG_IN, when the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

8.2.1. Phase Comparator 1 (PC1)

This circuit is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50 % duty cycle to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEM_OUT} = \frac{V_{CC}}{\pi} (\Phi_{SIG_IN} - \Phi_{COMP_IN})$$

where:

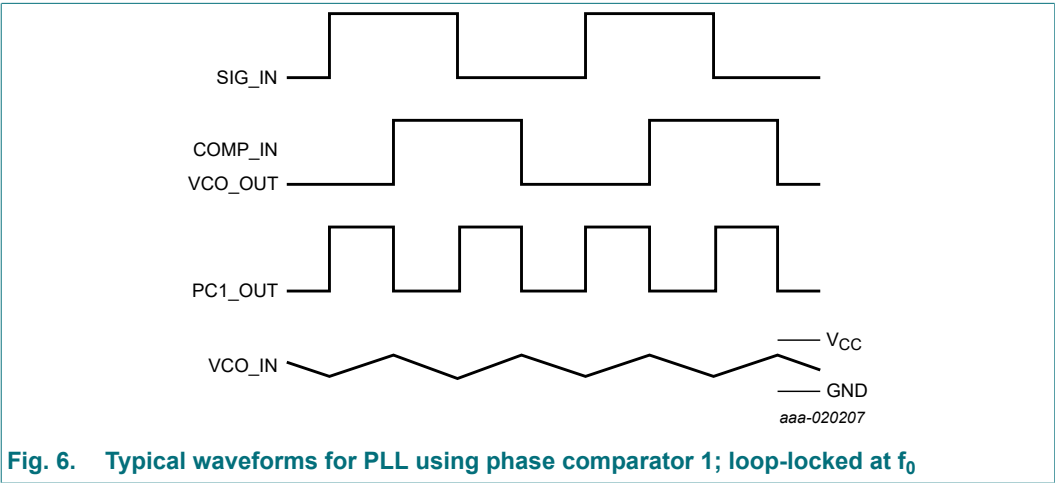
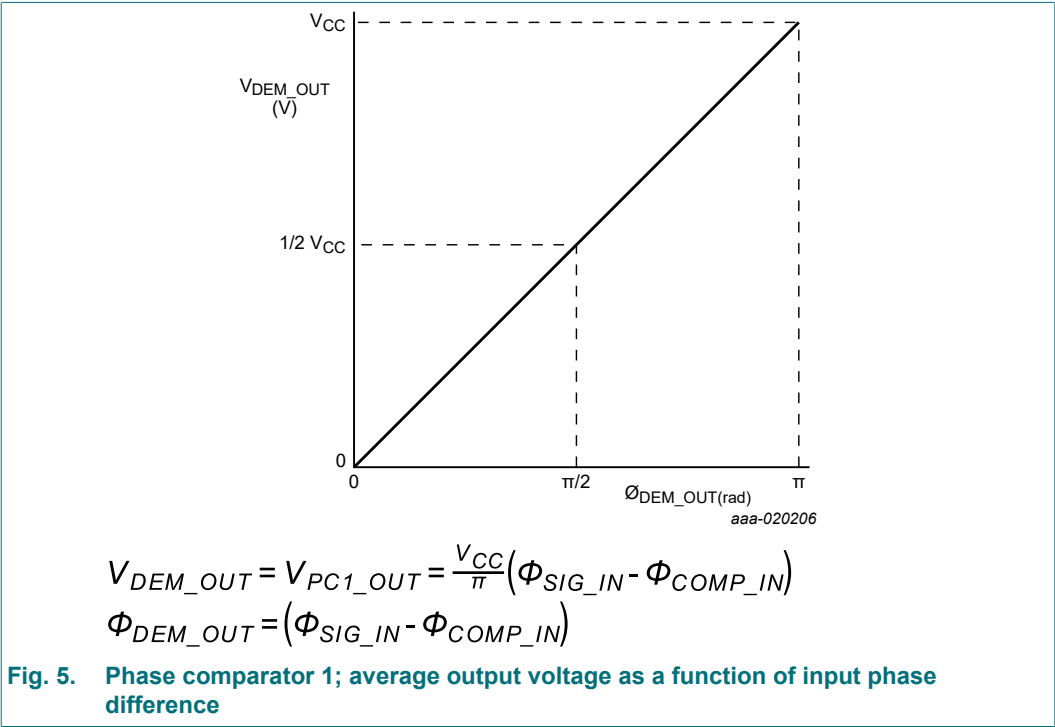
- V_{DEM_OUT} is the demodulator output at pin DEM_OUT
- $V_{DEM_OUT} = V_{PC1_OUT}$ (via low-pass filter)

The phase comparator gain is: $K_p = \frac{V_{CC}}{\pi} (V/rad)$

PC1 is fed to the VCO input via the low-pass filter and provided at the demodulator output at pin DEM_OUT ($V_{\text{DEM_OUT}}$). The average output voltage from PC1 is the result of the phase differences of signals (SIG_IN) and the comparator input (COMP_IN). These phase differences are shown in Fig. 5. The average of $V_{\text{DEM_OUT}}$ is equal to $0.5V_{\text{CC}}$ when no signal or noise is present at SIG_IN. Using this input, the VCO oscillates at the center frequency (f_0). Typical waveforms for the PC1 loop locked at f_0 are shown in Fig. 6.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL locks when it was initially out-of-lock. The frequency lock range ($2f_L$) is the frequency range of the input signals on which the loop stays locked when it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration remains locked even with very noisy input signals. Typical behavior of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO center frequency.



8.2.2. Phase Comparator 2 (PC2)

PC2 is a positive edge-triggered phase and frequency detector. When the PLL uses this comparator, positive signal transitions control the loop and the duty cycles of SIG_IN and COMP_IN are not important. PC2 comprises two D-type flip-flops, control gating and a 3-state output stage. The circuit functions as an up-down counter (see Fig. 4) where SIG_IN causes an up-count and COMP_IN a down count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEM_OUT} = \frac{V_{CC}}{4\pi} (\phi_{SIG_IN} - \phi_{COMP_IN})$$

where:

- V_{DEM_OUT} is the demodulator output at pin DEM_OUT
- $V_{DEM_OUT} = V_{PC2_OUT}$ (via low-pass filter)

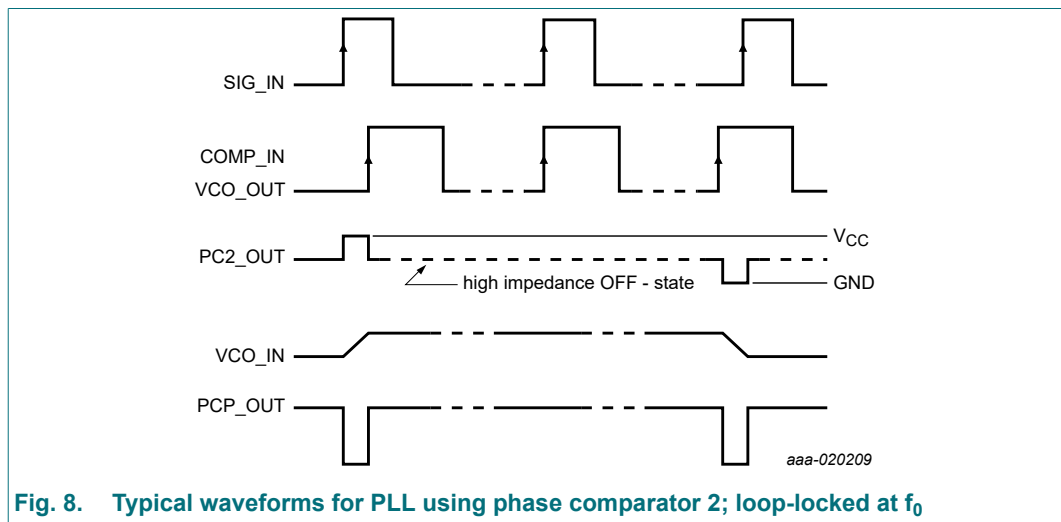
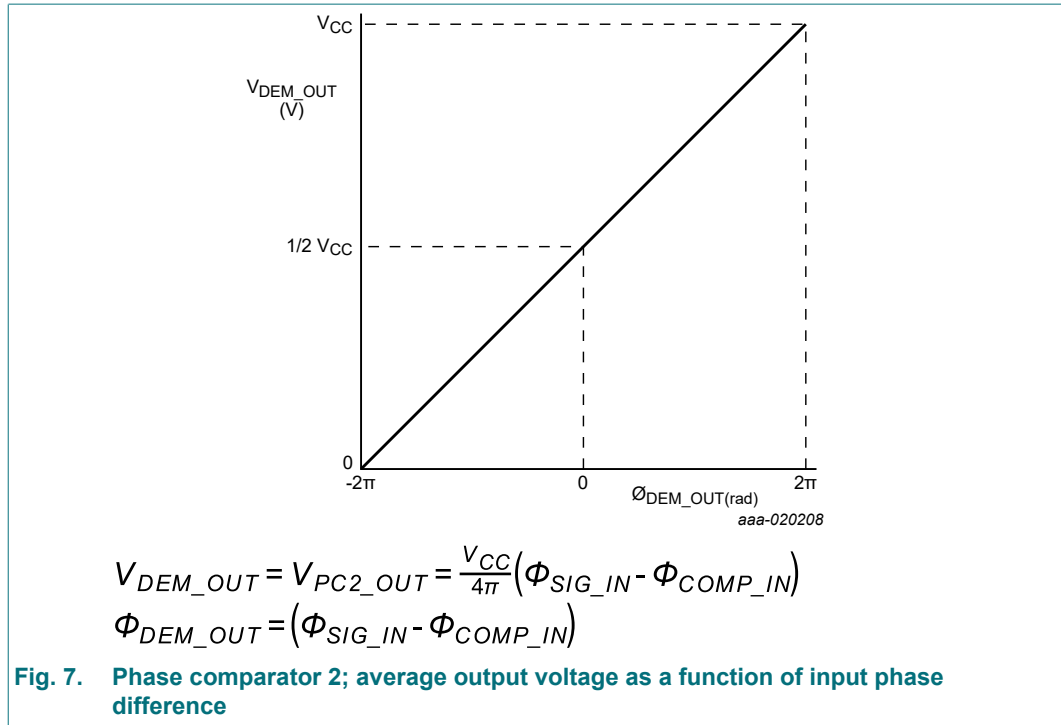
The phase comparator gain is: $K_p = \frac{V_{CC}}{4\pi} (V/rad)$

V_{DEM_OUT} is the resultant of the initial phase differences of SIG_IN and COMP_IN as shown in Fig. 7. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 8.

When the SIG_IN and COMP_IN frequencies are equal but the phase of SIG_IN leads that of COMP_IN, the p-type output driver at PC2_OUT is held 'ON'. The time that it is held 'ON' corresponds with the phase difference (ϕ_{DEM_OUT}). When the phase of SIG_IN lags that of COMP_IN, the n-type driver is held 'ON'.

When the SIG_IN frequency is higher than the COMP_IN frequency, the p-type output driver is held 'ON' for most of the input signal cycle time. For the remainder of the cycle time, both n- and p-type drivers are 'OFF' (3-state). If the SIG_IN frequency is lower than the COMP_IN frequency, the n-type driver is held 'ON' for most of the cycle. The voltage at capacitor (C2) of the low-pass filter, connected to PC2_OUT, varies until the phase and frequency of the signal and comparator inputs are equal. At this stable point, the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO_IN input is in a high-impedance state. In this condition, the signal at the phase comparator pulse output (PCP_OUT) is a HIGH level and can be used for indicating a locked condition.

Thus for PC2 no phase difference exists between SIG_IN and COMP_IN over the full frequency range of the VCO. The power dissipation due to the low-pass filter is reduced because both n- and p-type output drivers are 'OFF' for most of the signal input cycle. The PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_IN the VCO adjust, via PC2, to its lowest frequency.



8.2.3. Phase Comparator 3 (PC3)

PC3 is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, positive signal transitions control the loop and the duty factors of SIG_IN and COMP_IN are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEM_OUT} = \frac{V_{CC}}{2\pi} (\phi_{SIG_IN} - \phi_{COMP_IN})$$

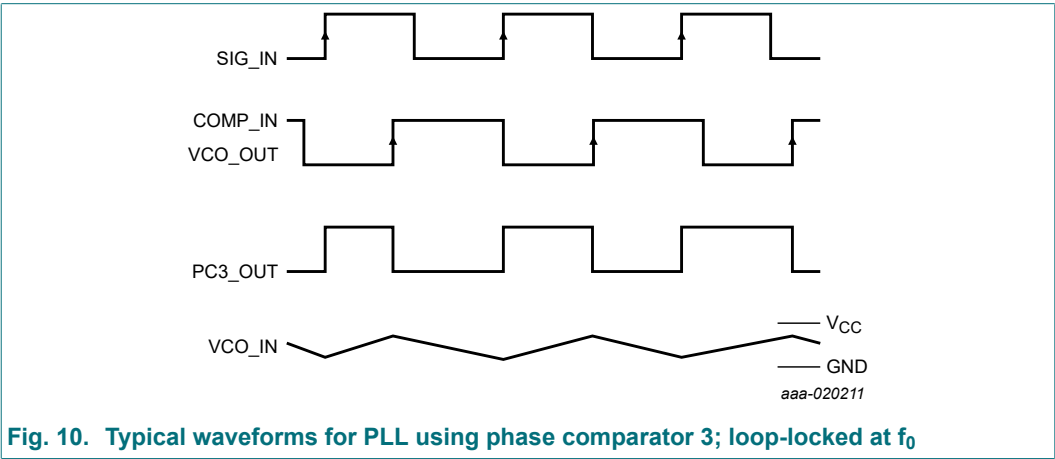
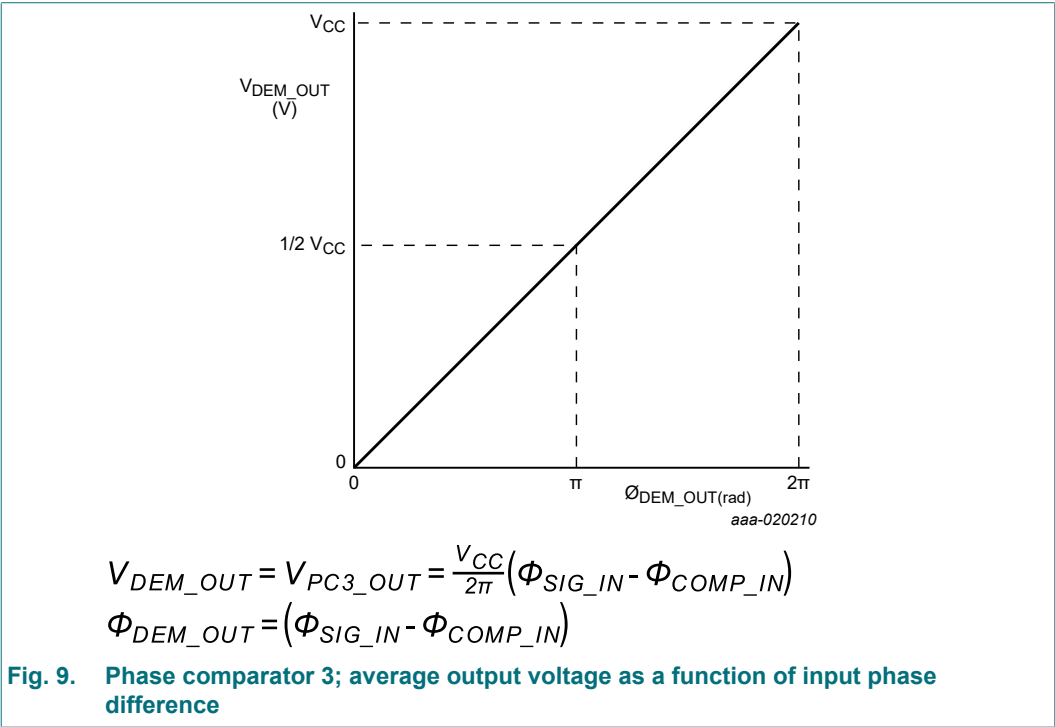
where:

- V_{DEM_OUT} is the demodulator output at pin DEM_OUT
- $V_{DEM_OUT} = V_{PC3_OUT}$ (via low-pass filter)

The phase comparator gain is: $K_p = \frac{V_{CC}}{2\pi} (V/rad)$

PC3 is fed to the VCO via the low-pass filter and present at the demodulator output at pin DEM_OUT. The average output from PC3 is the resultant of the phase differences of SIG_IN and COMP_IN, see Fig. 9. Typical waveforms for the PC3 loop locked at f_0 are shown in Fig. 10.

The phase-to-output response characteristic of PC3 (Fig. 9) differs from PC2 in that the phase angle between SIG_IN and COMP_IN varies between 0° and 360° . It is 180° at the center frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences. As a result, the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at SIG_IN, the VCO adjusts to its lowest frequency via PC3.



9. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [1]	-	500	mW

[1] For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

10. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		3.0	5.0	6.0	V
		when VCO is not used	2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rate	pin INH				
		V _{CC} = 2.0 V	-	-	625	ns/V
		V _{CC} = 4.5 V	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	ns/V
T _{amb}	ambient temperature		-40	+25	+125	°C

11. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Phase comparator section										
V _{IH}	HIGH-level input voltage	SIG_IN, COMP_IN; DC coupled								
		V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	SIG_IN, COMP_IN; DC coupled								
		V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	PCP_OUT, PCn_OUT; V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	PCP_OUT, PCn_OUT; V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	SIG_IN, COMP_IN; V _I = V _{CC} or GND								
		V _{CC} = 2.0 V	-	-	±3	-	±4	-	±5	µA
		V _{CC} = 3.0 V	-	-	±7	-	±9	-	±11	µA
		V _{CC} = 4.5 V	-	-	±18	-	±23	-	±27	µA
		V _{CC} = 6.0 V	-	-	±30	-	±38	-	±45	µA
I _{OZ}	OFF-state output current	PC2_OUT; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND								
		V _{CC} = 6.0 V	-	-	±0.5	-	±5	-	±10	µA
R _I	input resistance	SIG_IN, COMP_IN; V _I at self-bias operating point; ΔV _I = 0.5 V; see Fig. 11 , Fig. 12 and Fig. 13								
		V _{CC} = 3.0 V	-	800	-	-	-	-	-	kΩ
		V _{CC} = 4.5 V	-	250	-	-	-	-	-	kΩ
		V _{CC} = 6.0 V	-	150	-	-	-	-	-	kΩ

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
VCO section										
V _{IH}	HIGH-level input voltage	INH								
		V _{CC} = 3.0 V	2.1	1.7	-	2.1	-	2.1	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	INH								
		V _{CC} = 3.0 V	-	1.3	0.9	-	0.9	-	0.9	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	VCO_OUT; V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	VCO_OUT; V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		C1A, C1B; V _I = V _{IH} or V _{IL}								
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.40	-	0.47	-	0.54	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.40	-	0.47	-	0.54	V
I _I	input leakage current	INH, VCO_IN; V _I = V _{CC} or GND								
		V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
R1	resistor 1	V _{CC} = 3.0 V to 6.0 V [1]	3	-	300	-	-	-	-	kΩ
R2	resistor 2	V _{CC} = 3.0 V to 6.0 V [1]	3	-	300	-	-	-	-	kΩ
C1	capacitor 1	V _{CC} = 3.0 V to 6.0 V	40	-	no limit	-	-	-	-	pF
V _{VCO_IN}	input voltage on pin VCO_IN	VCO_IN; over the range specified for R1; for linearity see Fig. 21 and Fig. 22								
		V _{CC} = 3.0 V	1.1	-	1.9	-	-	-	-	V
		V _{CC} = 4.5 V	1.1	-	3.4	-	-	-	-	V
		V _{CC} = 6.0 V	1.1	-	4.9	-	-	-	-	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Demodulator section										
R _s	series resistance	at R _s > 300 kΩ, the leakage current can influence V _{DEM_OUT}								
		V _{CC} = 3.0 V to 6.0 V	50	-	300	-	-	-	-	kΩ
V _{offset}	offset voltage	VCO_IN to DEM_OUT; V _I = V _{VCO_IN} = 0.5V _{CC} ; values taken over R _s range; see Fig. 14								
		V _{CC} = 3.0 V	-	±30	-	-	-	-	-	mV
		V _{CC} = 4.5 V	-	±20	-	-	-	-	-	mV
		V _{CC} = 6.0 V	-	±10	-	-	-	-	-	mV
R _{dyn}	dynamic resistance	DEM_OUT; V _{DEM_OUT} = 0.5V _{CC}								
		V _{CC} = 3.0 V to 6.0 V	-	25	-	-	-	-	-	Ω
General										
I _{CC}	supply current	VCO disabled; COMP_IN, INH and SIG_IN at V _{CC} ; VCO_IN at GND; I _I at pins COMP_IN and SIGN_IN to be excluded								
		V _{CC} = 6.0 V	-	-	8	-	80	-	160	μA
C _I	input capacitance	INH	-	3.5	-	-	-	-	-	pF

[1] The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

11.1. Graphs

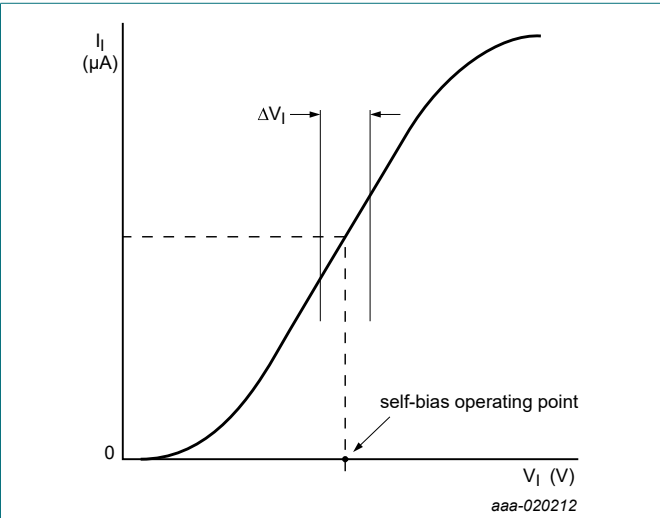


Fig. 11. Typical input resistance curve at SIG_IN and COMP_IN

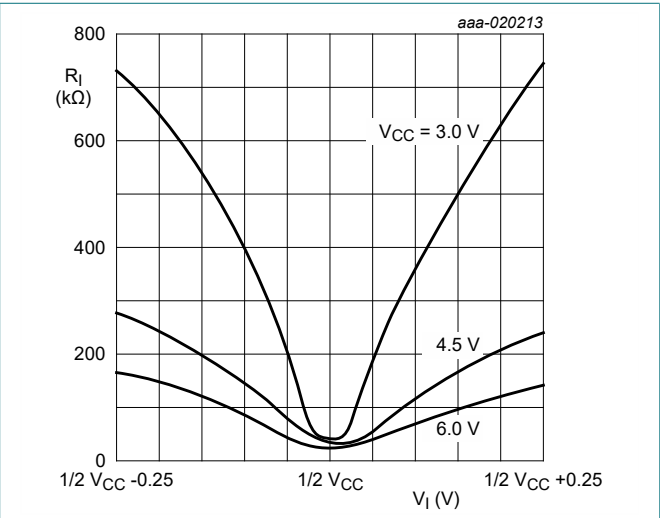


Fig. 12. Input resistance at SIG_IN, COMP_IN with $\Delta V_I = 0.5$ V at self-bias point

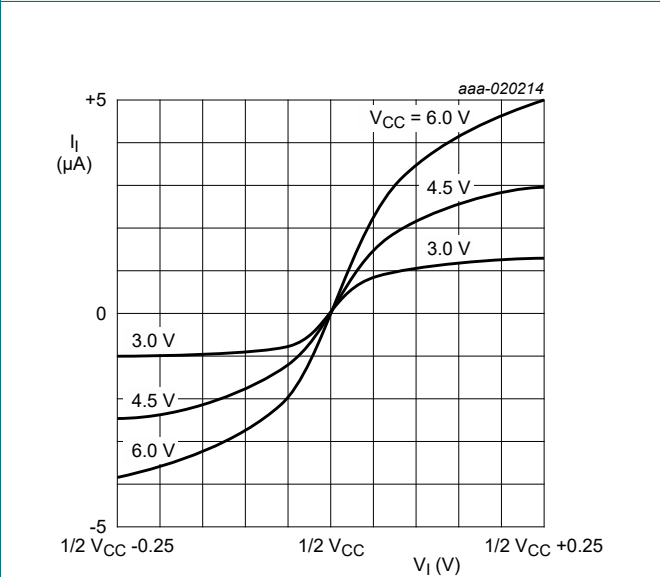


Fig. 13. Input current at SIG_IN, COMP_IN with $\Delta V_I = 0.5$ V at self-bias point

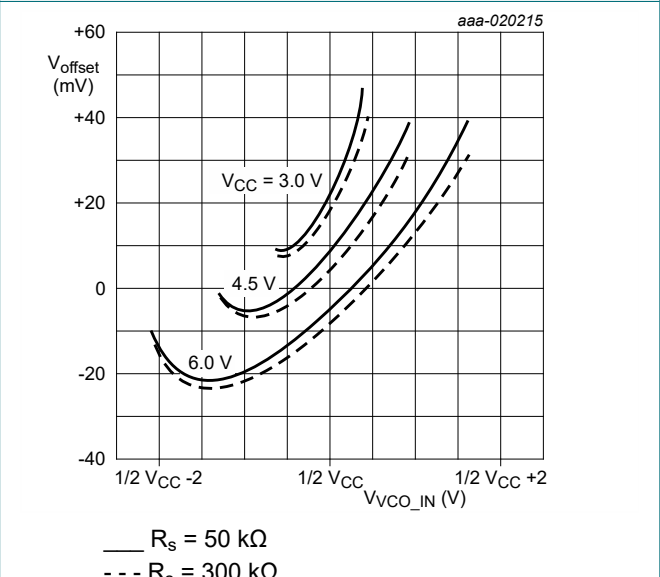


Fig. 14. Offset voltage at demodulator output as a function of V_{VCO_IN} and R_s

12. Dynamic characteristics

Table 6. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Typ	Max	Min	Max	
Phase comparator section											
t _{pd}	propagation delay	SIG_IN, COMP_IN to PC1_OUT; see Fig. 15 [1]									
		V _{CC} = 2.0 V	-	63	200	-	-	250	-	300	ns
		V _{CC} = 4.5 V	-	23	40	-	-	50	-	60	ns
		V _{CC} = 6.0 V	-	18	34	-	-	43	-	51	ns
		SIG_IN, COMP_IN to PCP_OUT; see Fig. 15 [1]									
		V _{CC} = 2.0 V	-	96	340	-	-	425	-	510	ns
		V _{CC} = 4.5 V	-	35	68	-	-	85	-	102	ns
		V _{CC} = 6.0 V	-	28	58	-	-	72	-	87	ns
		SIG_IN, COMP_IN to PC3_OUT; see Fig. 15 [1]									
		V _{CC} = 2.0 V	-	77	270	-	-	340	-	405	ns
		V _{CC} = 4.5 V	-	28	54	-	-	68	-	81	ns
		V _{CC} = 6.0 V	-	22	46	-	-	58	-	69	ns
t _{en}	enable time	SIG_IN, COMP_IN to PC2_OUT; see Fig. 16 [1]									
		V _{CC} = 2.0 V	-	83	280	-	-	350	-	420	ns
		V _{CC} = 4.5 V	-	30	56	-	-	70	-	84	ns
		V _{CC} = 6.0 V	-	24	48	-	-	60	-	71	ns
t _{dis}	disable time	SIG_IN, COMP_IN to PC2_OUT; see Fig. 16 [1]									
		V _{CC} = 2.0 V	-	99	325	-	-	405	-	490	ns
		V _{CC} = 4.5 V	-	36	65	-	-	81	-	98	ns
		V _{CC} = 6.0 V	-	29	55	-	-	69	-	83	ns
t _t	transition time	PC1_OUT, PC3_OUT, PCP_OUT; see Fig. 15 [1]									
		V _{CC} = 2.0 V	-	19	75	-	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	-	16	-	19	ns
V _{i(p-p)}	peak-to-peak input voltage	SIGN_IN, COMP_IN; AC coupled; f _i = 1 MHz									
		V _{CC} = 2.0 V	-	9	-	-	-	-	-	-	mV
		V _{CC} = 3.0 V	-	11	-	-	-	-	-	-	mV
		V _{CC} = 4.5 V	-	15	-	-	-	-	-	-	mV
		V _{CC} = 6.0 V	-	33	-	-	-	-	-	-	mV

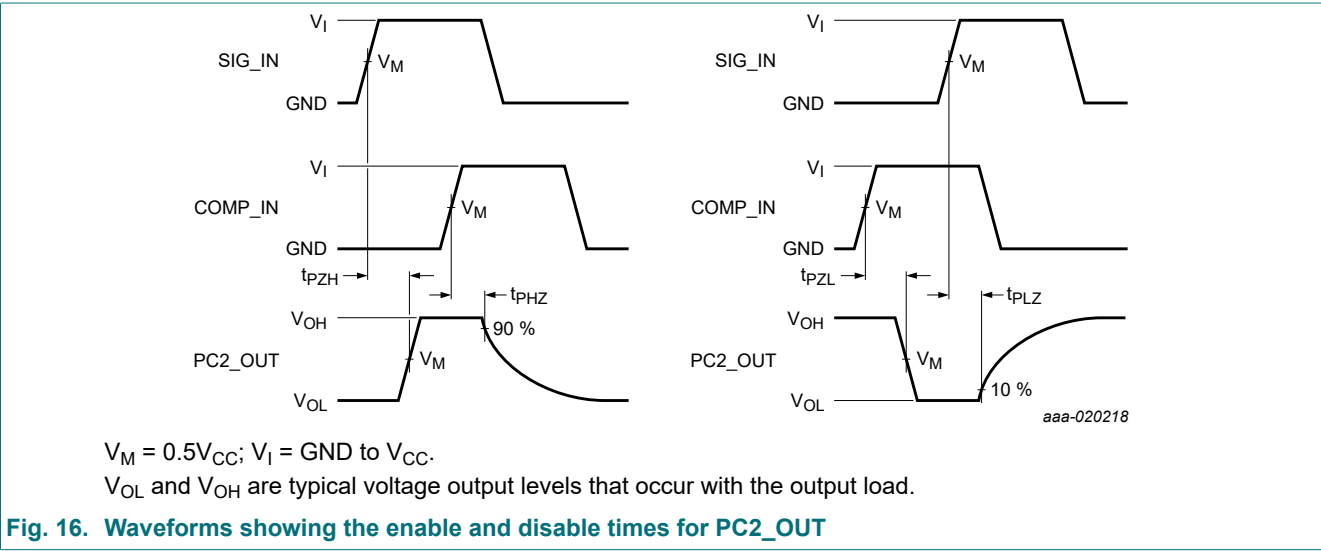
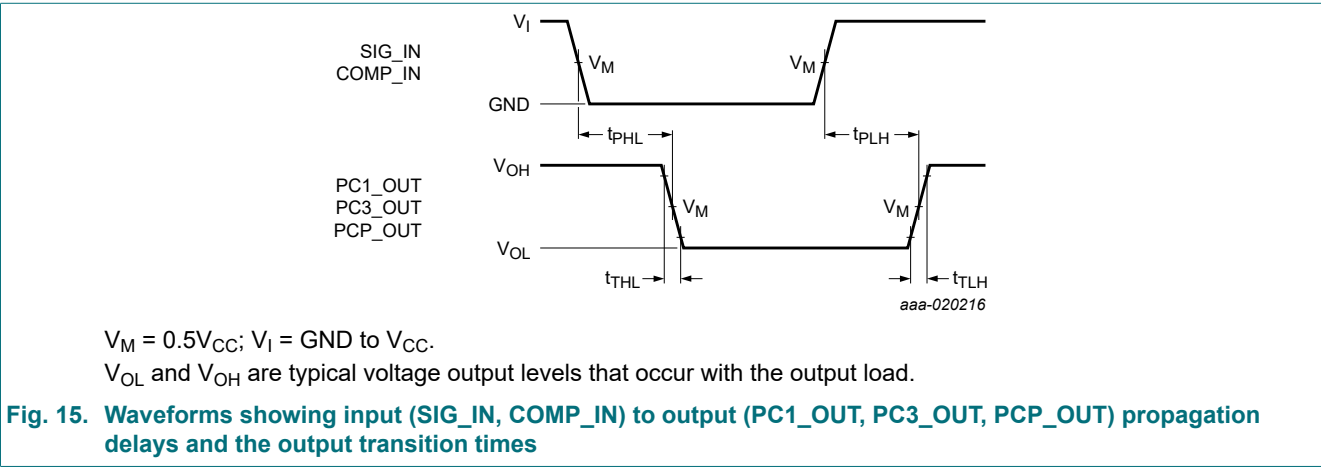
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Typ	Max	Min	Max	
VCO section											
f ₀	center frequency	V _{VCO_IN} = 0.5V _{CC} ; duty cycle = 50 %; R1 = 3 kΩ; R2 = ∞ Ω; C1 = 40 pF; see Fig. 19 and Fig. 20									
		V _{CC} = 3.0 V	7.0	10.0	-	-	-	-	-	-	MHz
		V _{CC} = 4.5 V	11.0	17.0	-	-	-	-	-	-	MHz
		V _{CC} = 5.0 V	-	19.0	-	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	13.0	21.0	-	-	-	-	-	-	MHz
Δf/f	relative frequency variation	R1 = 100 kΩ; R2 = ∞ Ω; C1 = 100 pF; see Fig. 21 and Fig. 22									
		V _{CC} = 3.0 V	-	1.0	-	-	-	-	-	-	%
		V _{CC} = 4.5 V	-	0.4	-	-	-	-	-	-	%
		V _{CC} = 6.0 V	-	0.3	-	-	-	-	-	-	%
Δf/ΔT	frequency variation with temperature	V _{VCO_IN} = 0.5V _{CC} ; R1 = 100 kΩ; R2 = ∞ Ω; C1 = 100 pF; see Fig. 17 and Fig. 18									
		V _{CC} = 3.0 V	-	-	-	-	0.20	-	-	-	%/K
		V _{CC} = 4.5 V	-	-	-	-	0.15	-	-	-	%/K
		V _{CC} = 6.0 V	-	-	-	-	0.14	-	-	-	%/K
δ	duty cycle	VCO_OUT; V _{CC} = 3.0 V to 6.0 V	-	50	-	-	-	-	-	-	%
General											
C _{PD}	power dissipation capacitance	[2] [3]	-	24	-	-	-	-	-	-	pF

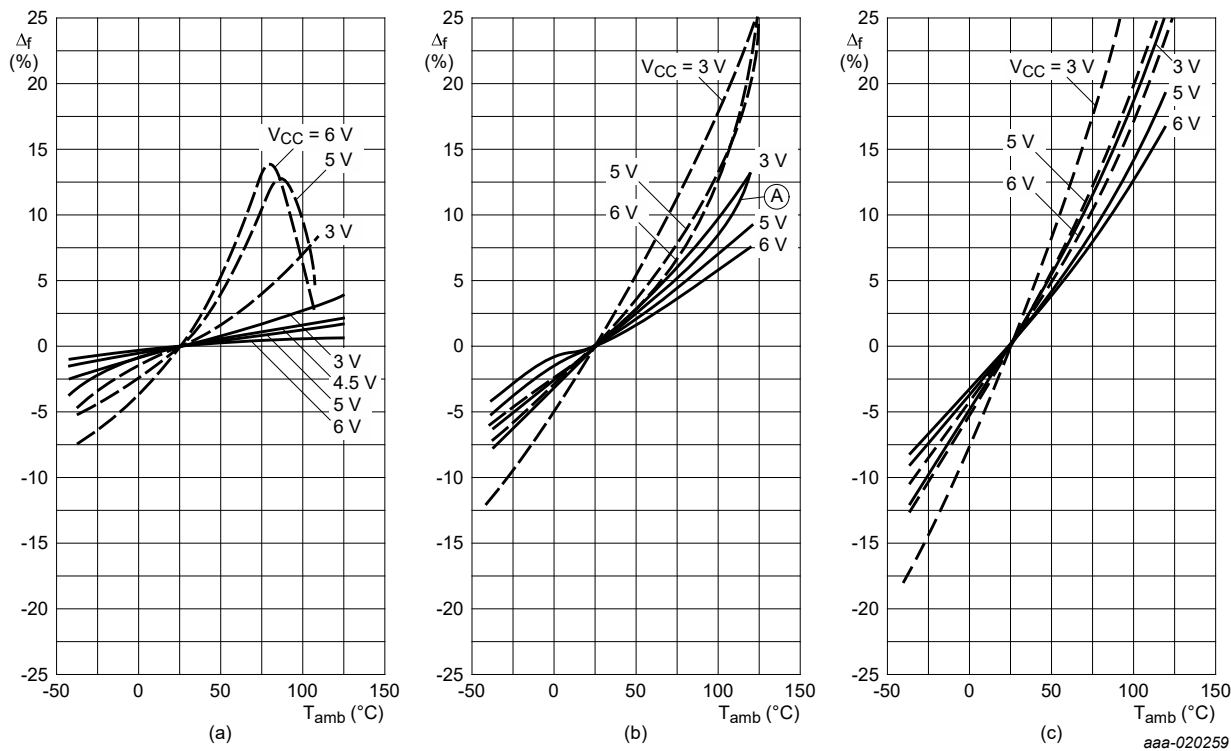
[1] t_{pd} is the same as t_{PLH} and t_{PHL}. t_{dis} is the same as t_{PLZ} and t_{PHZ}. t_{en} is the same as t_{PZL} and t_{PZH}. t_t is the same as t_{TLH} and t_{THL}.

[2] Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections, see Fig. 23, Fig. 24 and Fig. 25

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
Σ(C_L × V_{CC}² × f_o) = sum of outputs.

12.1. Waveforms and graphs





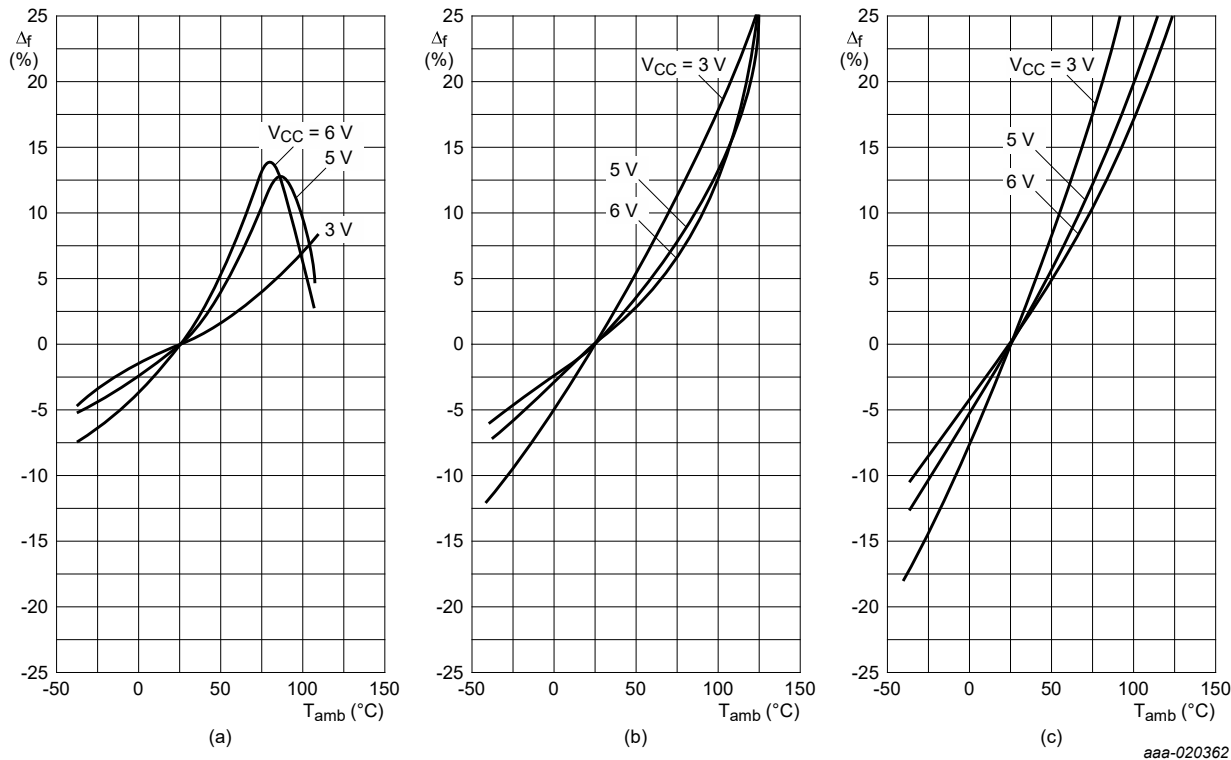
To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

In (b), the frequency stability for $R1 = R2 = 10\text{ k}\Omega$ at 5 V is also given (curve A). The total VCO bias current sets this curve, and is not simply the addition of the two 10 k Ω stability curves. C1 = 100 pF; $V_{VCO_IN} = 0.5V_{CC}$; This curve is set as follows:

___ Without offset $R2 = \infty\ \Omega$: (a) $R1 = 3\text{ k}\Omega$; (b) $R1 = 10\text{ k}\Omega$; (c) $R1 = 300\text{ k}\Omega$.

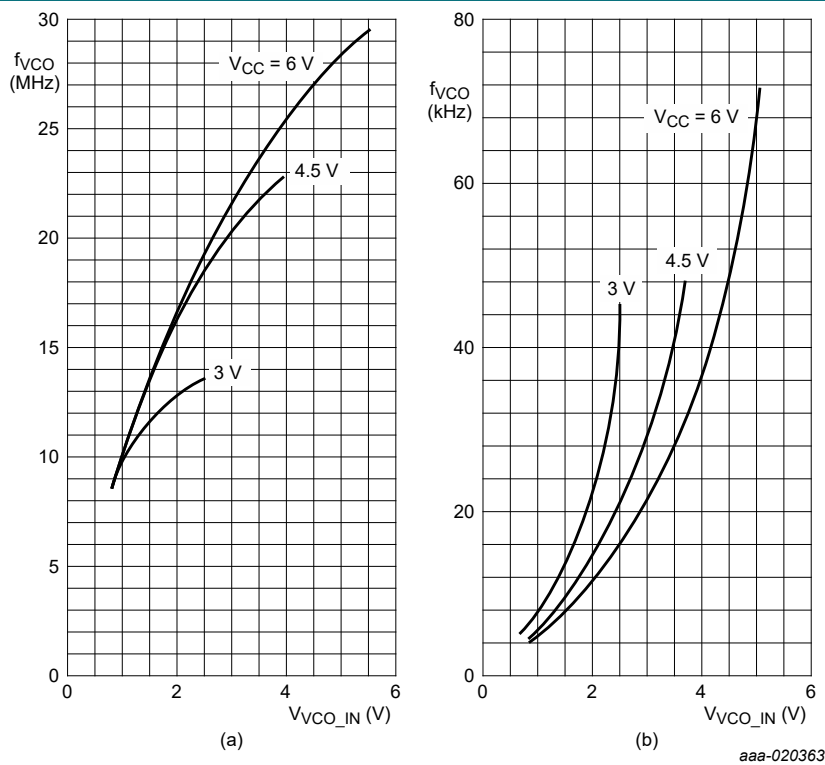
--- With offset $R1 = \infty\ \Omega$: (a) $R2 = 3\text{ k}\Omega$; (b) $R2 = 10\text{ k}\Omega$; (c) $R2 = 300\text{ k}\Omega$.

Fig. 17. Frequency stability of the VCO as a function of ambient temperature



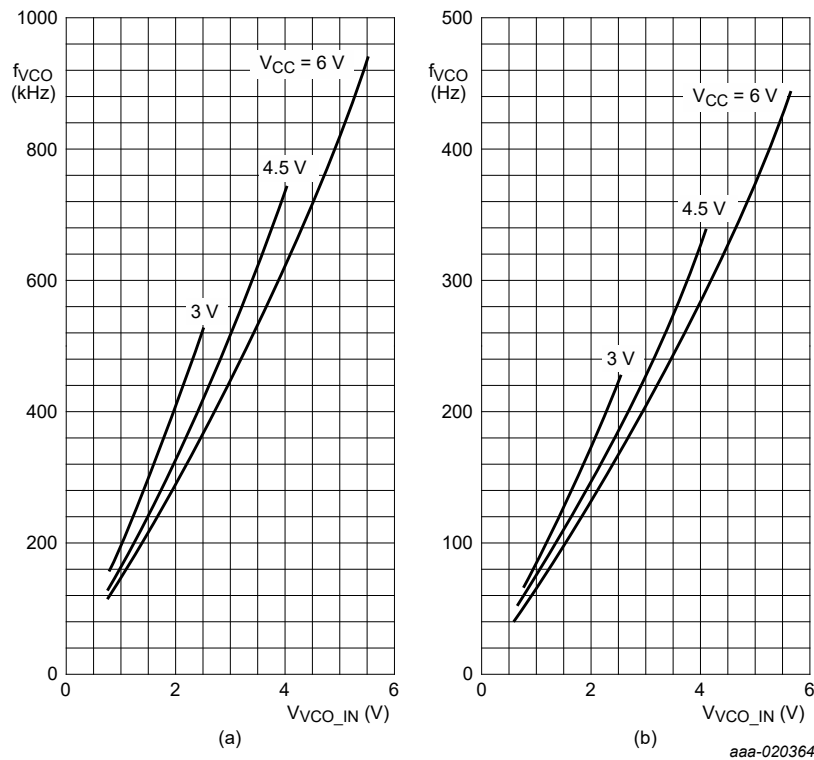
To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.
___ With offset; $R1 = \infty\ \Omega$: (a) $R2 = 3\text{ k}\Omega$; (b) $R2 = 10\text{ k}\Omega$; (c) $R2 = 300\text{ k}\Omega$.

Fig. 18. Frequency stability of the VCO as a function of ambient temperature



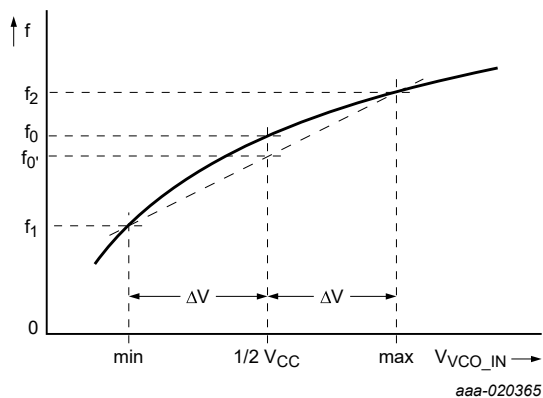
To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.
(a) $R1 = 3\text{ k}\Omega$; $C1 = 40\text{ pF}$ (b) $R1 = 3\text{ k}\Omega$; $C1 = 100\text{ nF}$

Fig. 19. Graphs showing VCO frequency as a function of the VCO input voltage



To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.
(a) R1 = 300 kΩ; C1 = 40 pF (b) R1 = 300 kΩ; C1 = 100 nF

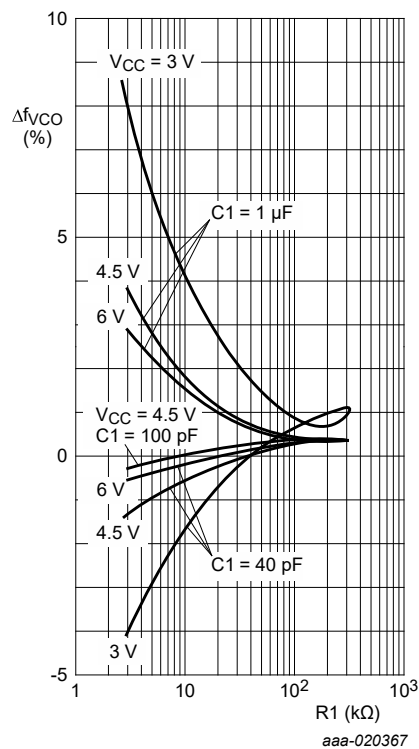
Fig. 20. Graphs showing VCO frequency as a function of the VCO input voltage



$\Delta V = 0.5 \text{ V}$ over the V_{CC} range.

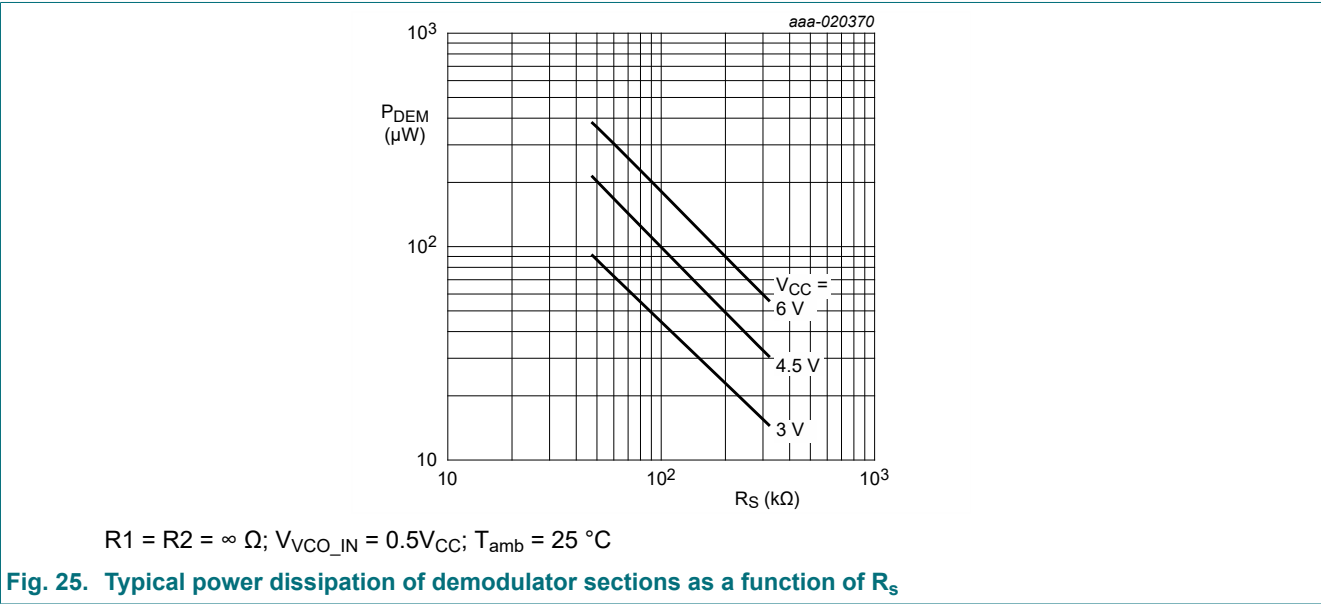
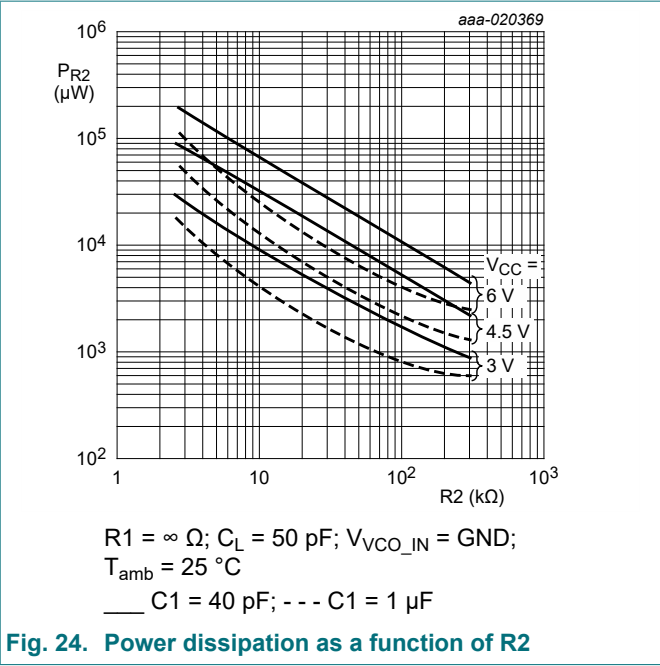
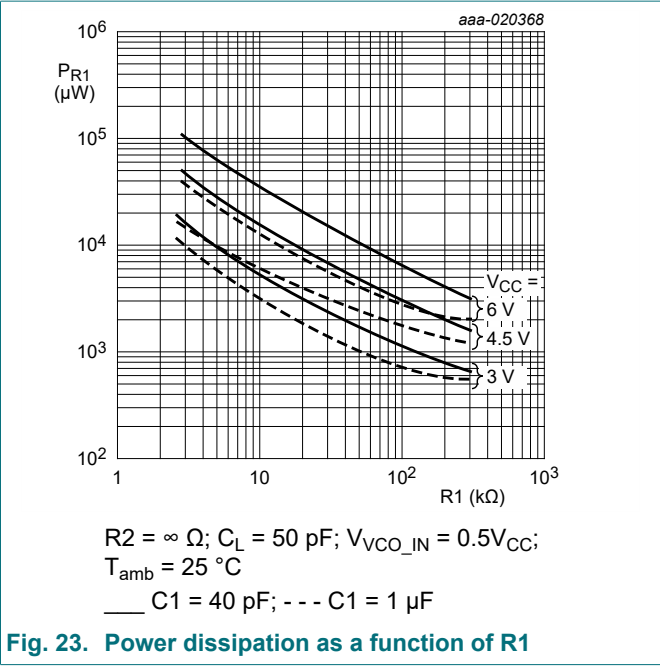
$$f_0 = \frac{f_1 + f_2}{2}$$
$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100 \%$$

Fig. 21. Definition of VCO frequency linearity



$R2 = \infty \Omega$; $\Delta V = 0.5 \text{ V}$

Fig. 22. Frequency linearity as a function of R1, C1



13. Application information

This information is a guide for the approximation of values of external components to be used with the 74HC4046A-Q100 in a phase-locked-loop system.

References should be made to [Fig. 29](#), [Fig. 30](#) and [Fig. 31](#) as indicated in [Table 8](#).

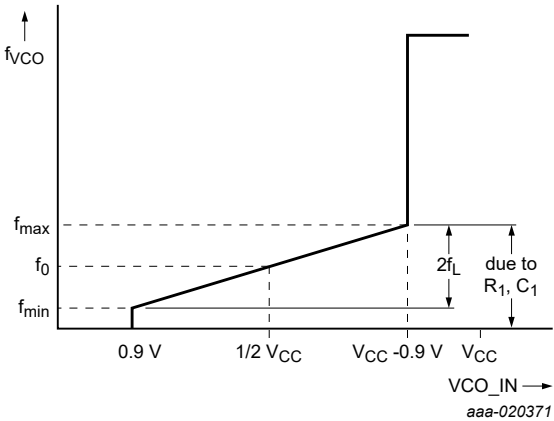
Values of the selected components should be within the ranges shown in [Table 7](#).

Table 7. Survey of components

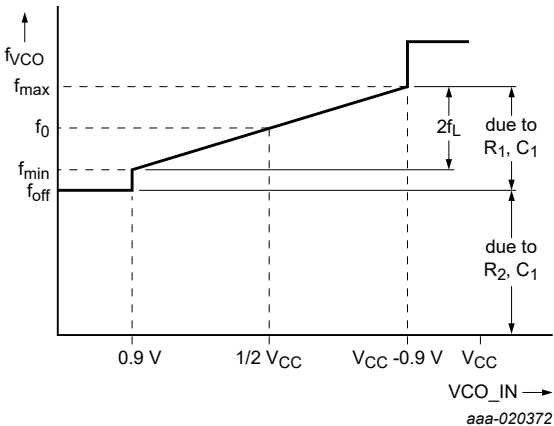
Component	Value
R1	between 3 k Ω and 300 k Ω
R2	between 3 k Ω and 300 k Ω
R1 + R2	parallel value > 2.7 k Ω
C1	> 40 pF

Table 8. Design considerations for VCO section

Subject	Phase comparator	Design consideration
VCO frequency without extra offset	PC1, PC2 or PC3	VCO frequency characteristic. With $R2 = \infty \Omega$ and $R1$ within the range $3 \text{ k}\Omega < R1 < 300 \text{ k}\Omega$, the characteristics of the VCO operation is as shown in Fig. 26a. (Due to $R1$, $C1$ time constant a small offset remains when $R2 = \infty \Omega$).
	PC1	Selection of $R1$ and $C1$. Given f_0 , determine the values of $R1$ and $C1$ using Fig. 29.
	PC2 or PC3	Given f_{max} and f_0 , determine the values of $R1$ and $C1$ using Fig. 29; use Fig. 31 to obtain $2f_L$ and then use it to calculate f_{min} .
VCO frequency with extra offset	PC1, PC2 or PC3	VCO frequency characteristic. With $R1$ and $R2$ within the ranges $3 \text{ k}\Omega < R1 < 300 \text{ k}\Omega$ and $3 \text{ k}\Omega < R2 < 300 \text{ k}\Omega$. The characteristics of the VCO operation are as shown in Fig. 26b.
	PC1, PC2 or PC3	Selection of $R1$, $R2$ and $C1$. Given f_0 and f_L determine the value of product $R1C1$ by using Fig. 31. Calculate f_{off} from the equation $f_{\text{off}} = f_0 - 1.6f_L$. Obtain the values of $C1$ and $R2$ by using Fig. 30. Calculate the value of $R1$ from the value of $C1$ and the product $R1C1$.
PLL conditions no signal at pin SIG_IN	PC1	VCO adjusts to f_0 with $\Phi_{\text{DEM_OUT}} = 90^\circ$ and $V_{\text{VCO_IN}} = 0.5V_{\text{CC}}$; see Fig. 5
	PC2	VCO adjusts to f_0 with $\Phi_{\text{DEM_OUT}} = -360^\circ$ and $V_{\text{VCO_IN}} = \text{minimum}$, see Fig. 7
	PC3	VCO adjusts to f_0 with $\Phi_{\text{DEM_OUT}} = -360^\circ$ and $V_{\text{VCO_IN}} = \text{minimum}$, see Fig. 9



a. Operating without offset; f_0 = center frequency; $2f_L$ = frequency lock range.

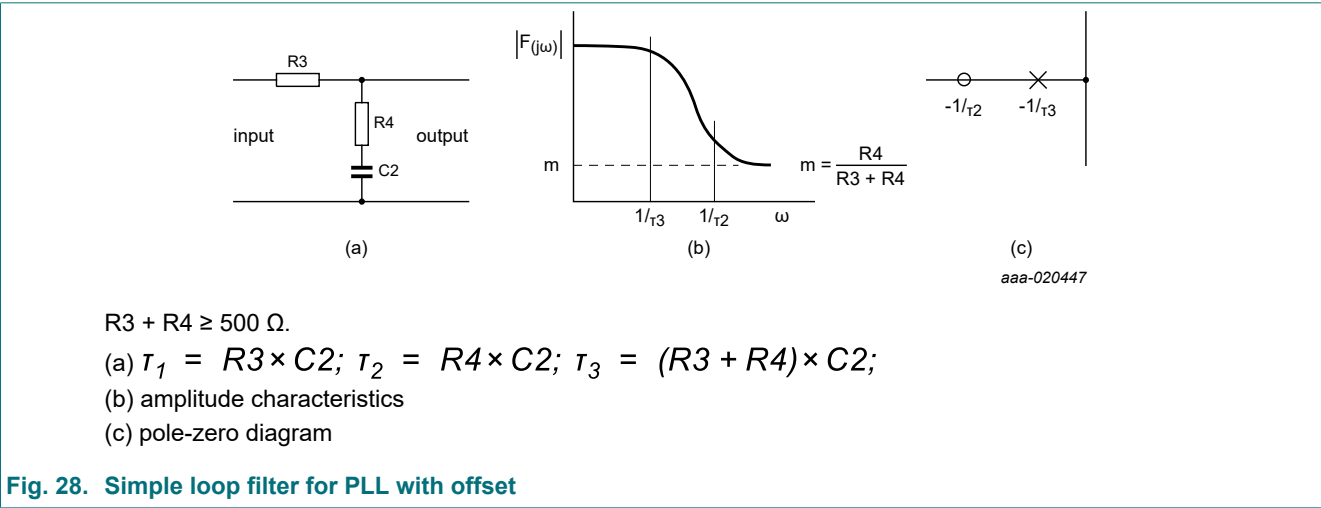
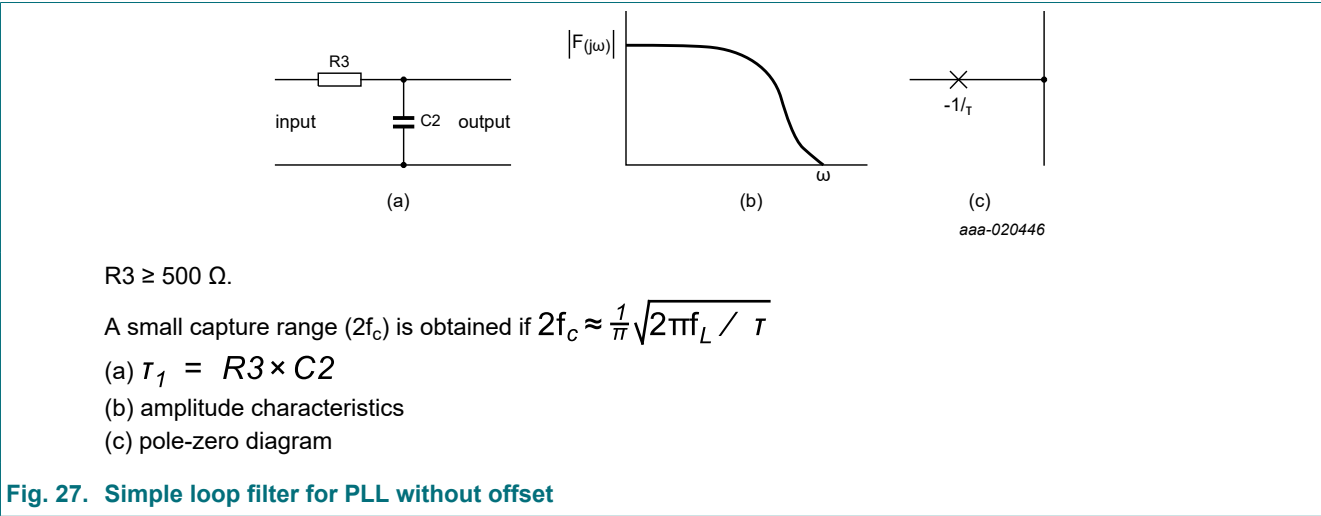


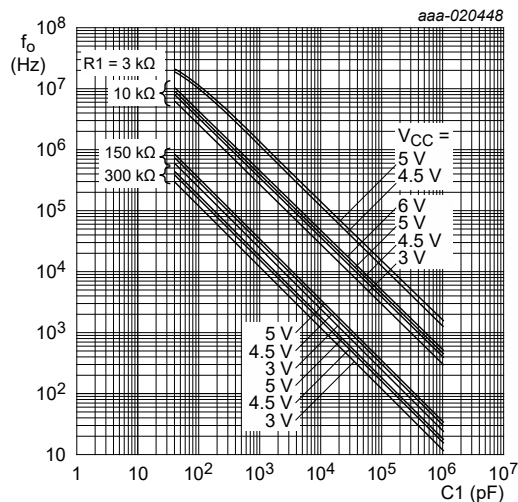
b. Operating with offset; f_0 = center frequency; $2f_L$ = frequency lock range.

Fig. 26. Frequency characteristic of VCO

Table 9. General design considerations

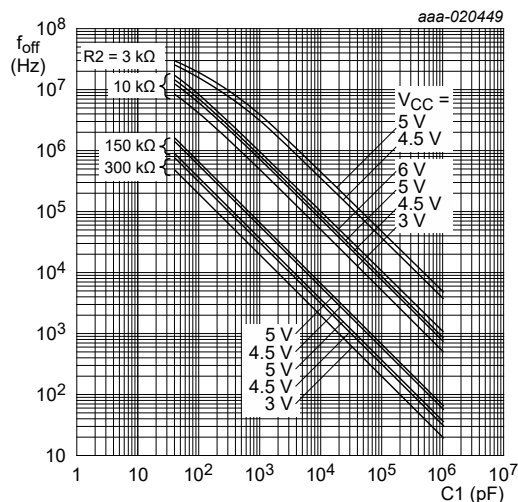
Subject	Phase comparator	Design consideration
PLL frequency capture range	PC1, PC2 or PC3	Loop filter component selection, see Fig. 27 and Fig. 28
PLL locks on harmonics at center frequency	PC1 or PC3	yes
	PC2	no
Noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$; large ripple content at $\Phi_{\text{DEM_OUT}} = 90^\circ$
	PC2	$f_r = f_i$; small ripple content at $\Phi_{\text{DEM_OUT}} = 0^\circ$
	PC3	$f_r = f_i$; large ripple content at $\Phi_{\text{DEM_OUT}} = 180^\circ$





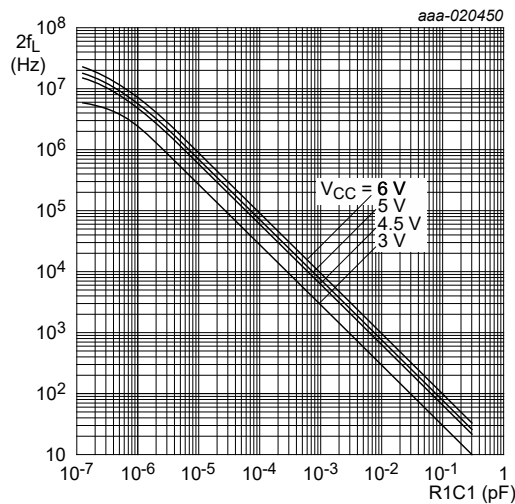
To obtain optimum VCO performance, C_1 must be as small as possible but larger than 100 pF. Interpolation for various values of R_1 can be easily calculated because a constant $R_1 C_1$ product produces almost the same VCO output frequency.
 $R_2 = \infty \Omega$; $V_{VCO_IN} = 0.5V_{CC}$; $INH = GND$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig. 29. Typical value of VCO center frequency (f_0) as a function of C_1



To obtain optimum VCO performance, C_1 must be as small as possible but larger than 100 pF. Interpolation for various values of R_2 can be easily calculated because a constant $R_2 C_1$ product produces almost the same VCO output frequency.
 $R_1 = \infty \Omega$; $V_{VCO_IN} = 0.5V_{CC}$; $INH = GND$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig. 30. Typical value of frequency offset as a function of C_1



$V_{VCO_IN} = 0.9\text{ V to } (V_{CC} - 0.9)\text{ V}; R2 = \infty\ \Omega.$

VCO gain: $K_V = \frac{2f_L}{V_{VCO_IN\ range}}\ 2\pi\ (\text{rad/s/V})$

Fig. 31. Typical frequency lock range ($2f_L$) as a function of the product $R1C1$

13.1. PLL design example

The frequency synthesizer used in the design example shown in [Fig. 32](#) has the following parameters:

- Output frequency: 2 MHz to 3 MHz
- Frequency steps: 100 kHz
- Settling time: 1 ms
- Overshoot: < 20 %

The open loop gain is:

$$H(s) \times G(s) = K_p(s) \times K_f(s) \times K_o(s) \times K_n$$

where:

- $K_p(s)$ = phase comparator gain
- $K_f(s)$ = low-pass filter transfer gain
- $K_o(s) = K_v/s$ VCO gain
- $K_n = 1/n$ divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{\min} = \frac{f_{\text{OUT}}}{f_{\text{step}}} = \frac{2 \text{ MHz}}{100 \text{ kHz}} = 20$$

$$N_{\max} = \frac{f_{\text{OUT}}}{f_{\text{step}}} = \frac{3 \text{ MHz}}{100 \text{ kHz}} = 30$$

The values of R1, R2 and C1; R2 = 10 kΩ (adjustable) set the VCO.

The values can be determined using the information in [Table 8](#) and [Table 9](#).

With $f_0 = 2.5 \text{ MHz}$ and $f_L = 500 \text{ kHz}$, the following values ($V_{CC} = 5.0 \text{ V}$) are given:

- R1 = 10 kΩ
- R2 = 10 kΩ
- C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2\pi}{0.9 - (V_{CC} - 0.9)} = \frac{1 \text{ MHz}}{3.2} \times 2\pi \approx 2 \times 10^6 \text{ rad/s/V}$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4\pi} = 0.4 \text{ V/rad}$$

The transfer gain of the filter is calculated as follows:

$$K_f(s) = \frac{1 + \tau_2(s)}{1 + (\tau_1 + \tau_2)(s)}$$

Where:

$$\tau_1 = R3 \times C2$$

$$\tau_2 = R4 \times C2$$

The characteristic equation is: $1 + H(s) \times G(s) = 0$

It results in:

$$S^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} \times S + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0$$

The natural frequency ω_n is defined as:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}$$

and the damping value (ζ) given as: $\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}$

In Fig. 33, the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine ω_n . Fig. 33 shows that the damping ratio $\zeta = 0.45$ produces an overshoot of less than 20 % and settle to within 5 % at $\omega_n t = 5$. The required settling time is 1 ms. It results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3 \text{ rad/s}$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{(\omega_n)^2}$$

The maximum overshoot occurs at N_{\max} :

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011 \text{ s}$$

When $C2 = 470 \text{ nF}$, then:

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n \times C2} = 315 \Omega$$

$R3$ can be calculated: $R3 = \frac{\tau_1}{C2} - R4 = 2 \text{ k}\Omega$

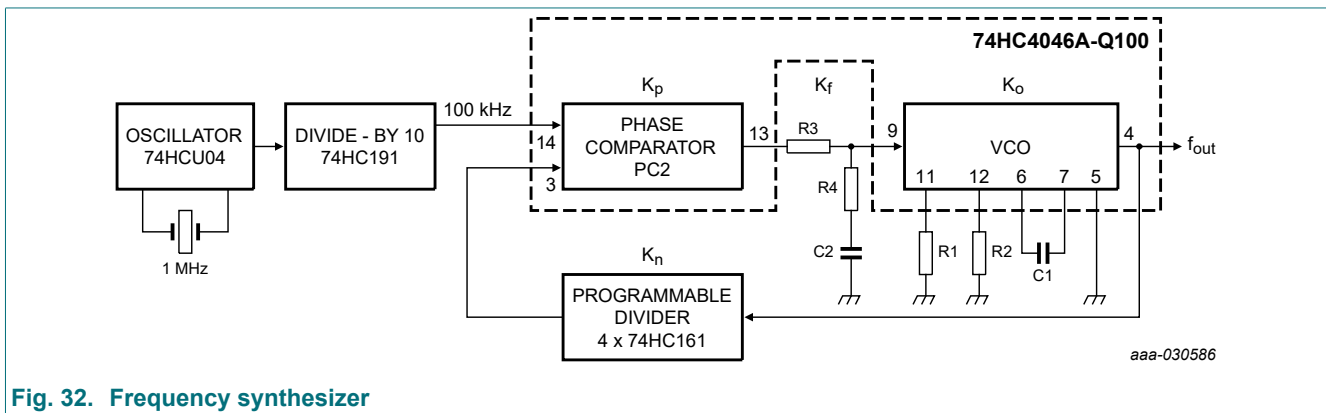


Fig. 32. Frequency synthesizer

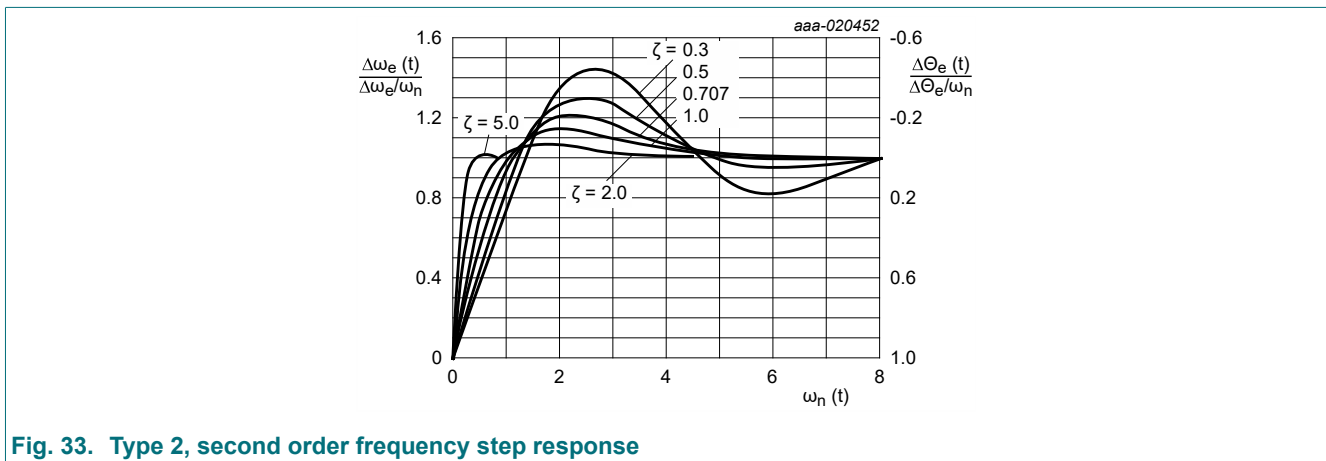
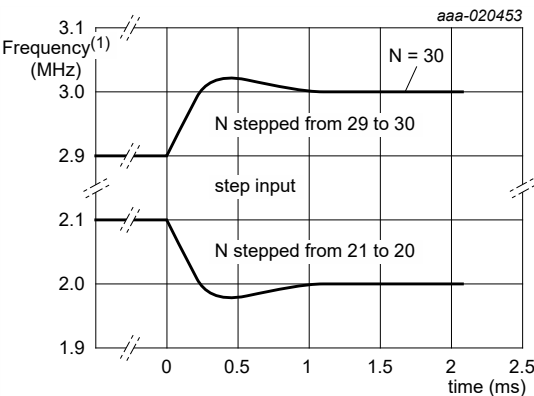


Fig. 33. Type 2, second order frequency step response



The output frequency is proportional to the VCO control voltage. As a result, the PLL frequency response can be observed with an oscilloscope by monitoring pin VCO_IN of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin VCO_IN using a simple RC filter. The filter has a long time constant when compared with the phase detector sampling rate, but short when compared with the PLL response time.

Fig. 34. Frequency compared to the time response

14. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1

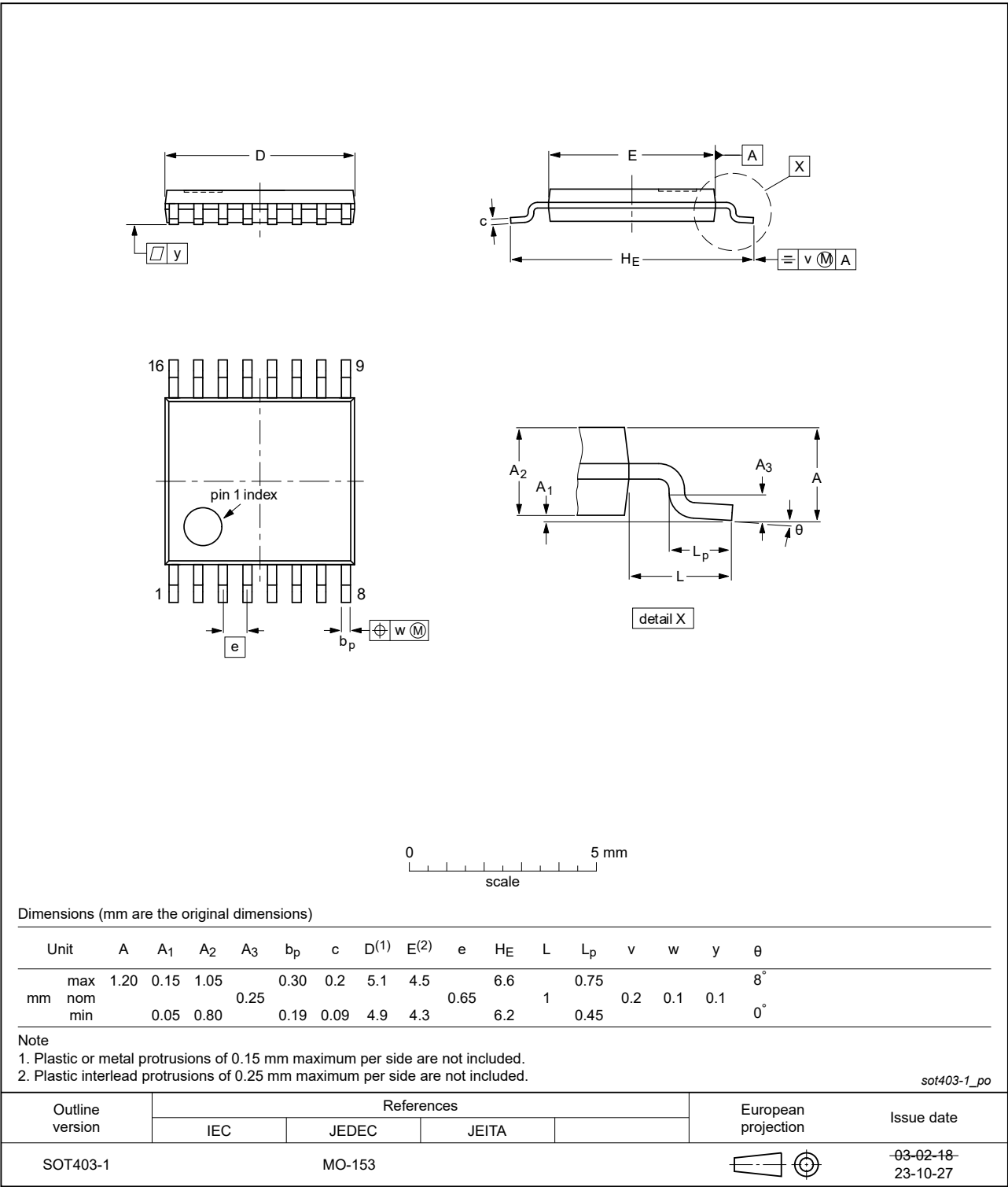


Fig. 35. Package outline SOT403-1 (TSSOP16)

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductors
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
PLL	Phase-Locked Loop
VCO	Voltage Controlled Oscillator

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4046A_Q100 v.3	20240219	Product data sheet	-	-
Modifications:	<ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard.Fig. 35: Aligned TSSOP package outline drawing to JEDEC MO-153.			
74HC4046A_Q100 v.2	20230608	Product data sheet	-	-
Modifications:	<ul style="list-style-type: none">Section 2 updated.			
74HC4046A_Q100 v.1	20191127	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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