



PSMN1R5-25MLH

N-channel 25 V, 1.81 mΩ, 150 A logic level MOSFET in LPAK33 using NextPowerS3 technology

30 September 2019

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LPAK33 package. NextPowerS3 technology delivers low $R_{DS(on)}$, low I_{DSS} leakage and high efficiency. Rated to 150 A and optimized with low gate resistance (R_G) for fast-switching applications.

2. Features and benefits

- Optimized for low $R_{DS(on)}$ and low gate resistance (R_G)
- Fast switching – reduced switching losses
- Strong linear-mode (SOA) rating
- Low leakage < 1 μA at 25 °C
- Low spiking and ringing for low EMI designs
- Optimized for 4.5 V gate drive
- 150 A continuous $I_{D(max)}$ rating
- High reliability copper-clip bonded and solder die attach LPAK33 package
- Qualified to 175 °C
- Exposed leads for optimal visual solder inspection

3. Applications

- Synchronous buck regulator
- Synchronous rectifier in AC-DC and DC-DC applications
- BLDC (brushless) motor control
- eFuse and battery protection
- OR-ing and hot-swap

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	25	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	150	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	106	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	1.46	1.81	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	2.1	2.7	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13		1	5.6	11.2	nC
Q _{G(tot)}	total gate charge			7.7	17	28	nC

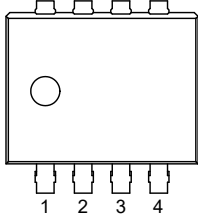
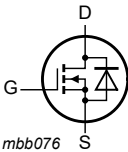
N-channel 25 V, 1.81 mΩ, 150 A logic level MOSFET in LPAK33 using NextPowerS3 technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
S	softness factor	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; Fig. 16	-	0.88	-	

[1] 150A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK33 (SOT1210)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R5-25MLH	LPAK33	Plastic, single ended surface mounted package (LPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R5-25MLH	1H525L

8. Limiting values

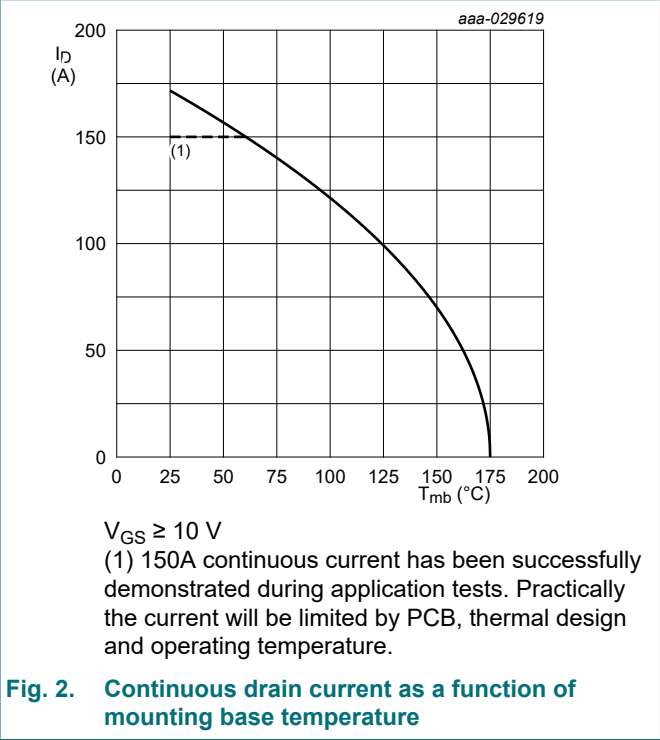
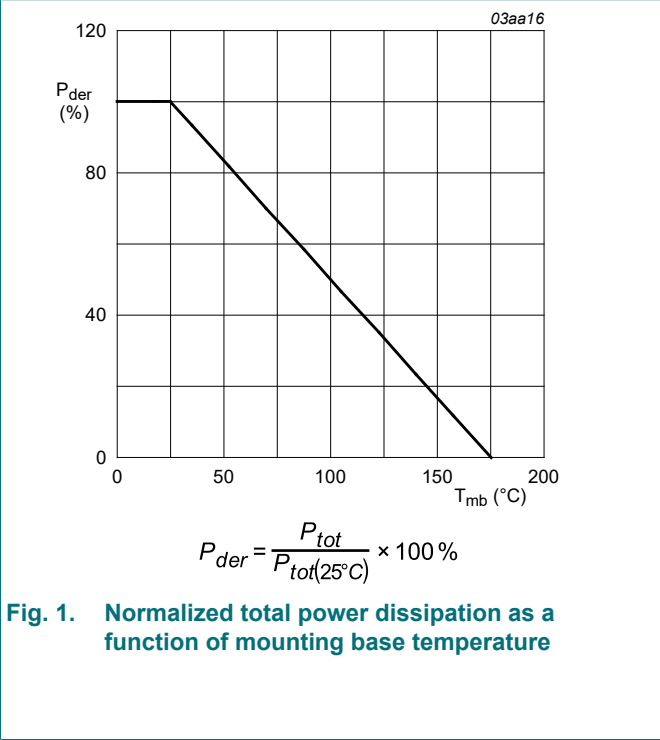
Table 5. Limiting values

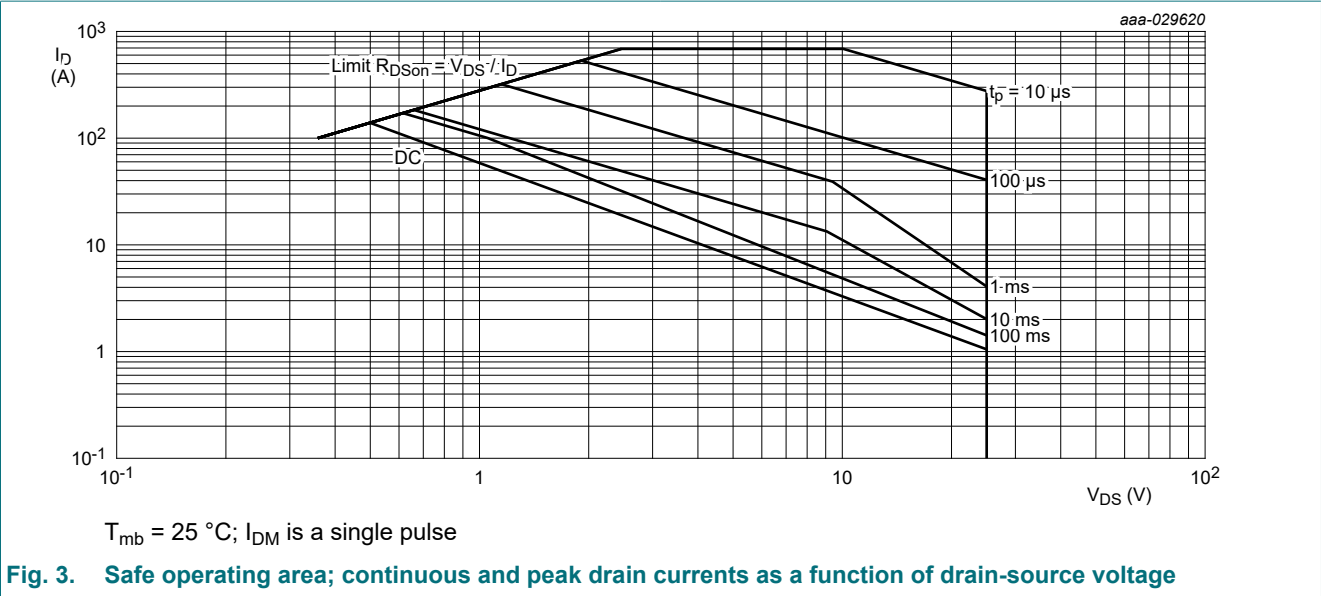
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	106	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	150	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	121	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	687	A
T_{stg}	storage temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	106	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	687	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 25 A; V _{sup} ≤ 25 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 811 μs	[2]	-	330	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 25 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	87	A

- [1] 150A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

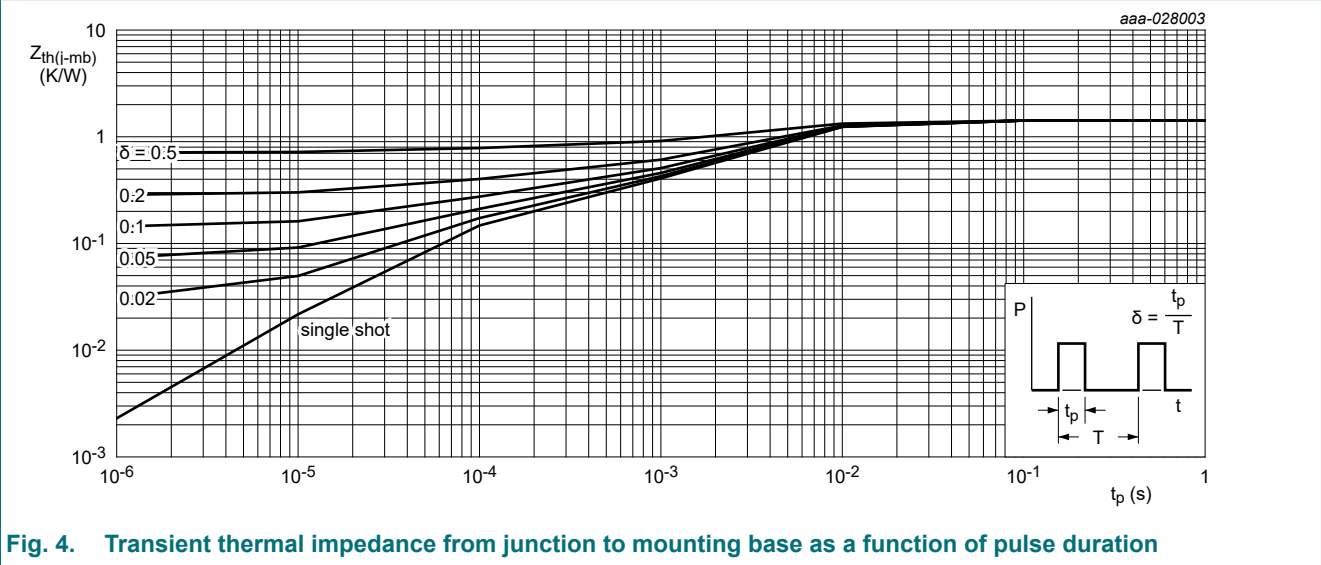


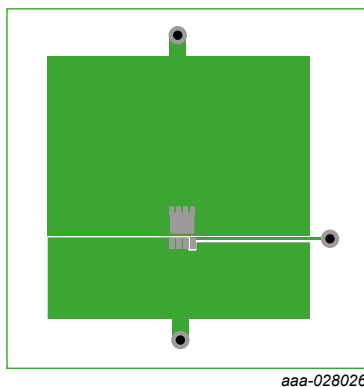


9. Thermal characteristics

Table 6. Thermal characteristics

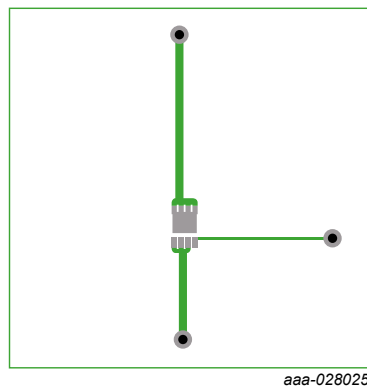
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	1.12	1.42	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	50	-	K/W
		Fig. 6		-	130	-	K/W





Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$	25	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$	1.2	1.73	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25^\circ C \leq T_j \leq 150^\circ C$	-	-4	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	-	1	μA
		$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 125^\circ C$	-	2.5	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C$; Fig. 10	-	1.46	1.81	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 150^\circ C$; Fig. 11	-	-	3.2	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25^\circ C$; Fig. 10	-	2.1	2.7	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 150^\circ C$; Fig. 11	-	-	4.8	mΩ
R_G	gate resistance	$f = 1 MHz; T_j = 25^\circ C$	0.5	1.2	3	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V$; Fig. 12 ; Fig. 13	7.7	17	28	nC
		$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 10 V$; Fig. 12 ; Fig. 13	15.8	35	58	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$; $T_j = 25^\circ C$	-	18	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 12 ; Fig. 13		1.5	5.5	10.5	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			0.86	3.2	6.1	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			0.6	2.2	4.2	nC
Q_{GD}	gate-drain charge			1	5.6	11.2	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; Fig. 12 ; Fig. 13		-	2.8	-	V
C_{iss}	input capacitance	$V_{DS} = 12\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$; Fig. 14		1267	2111	3167	pF
C_{oss}	output capacitance			872	1454	2181	pF
C_{rss}	reverse transfer capacitance			62	230	552	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}$; $R_L = 0.4\text{ Ω}$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5\text{ Ω}$		-	14	-	ns
t_r	rise time			-	25	-	ns
$t_{d(off)}$	turn-off delay time			-	18	-	ns
t_f	fall time			-	14	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$		-	23	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 15		-	0.78	1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/μs}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; Fig. 16		-	30	-	ns
Q_r	recovered charge		[1]	-	23	-	nC
t_a	reverse recovery rise time			-	16	-	ns
t_b	reverse recovery fall time			-	14	-	ns
S	softness factor			-	0.88	-	

[1] includes capacitive recovery

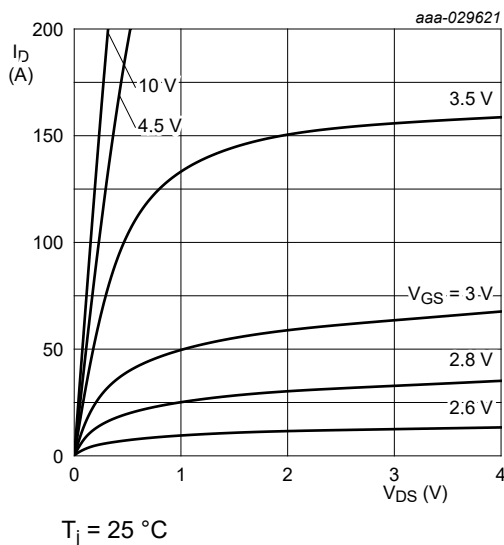


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

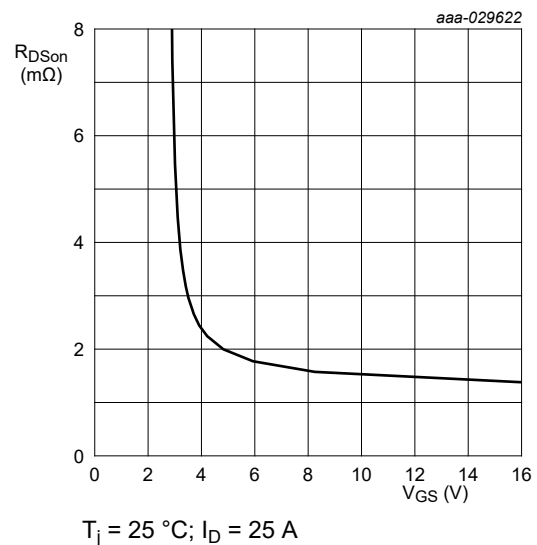


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

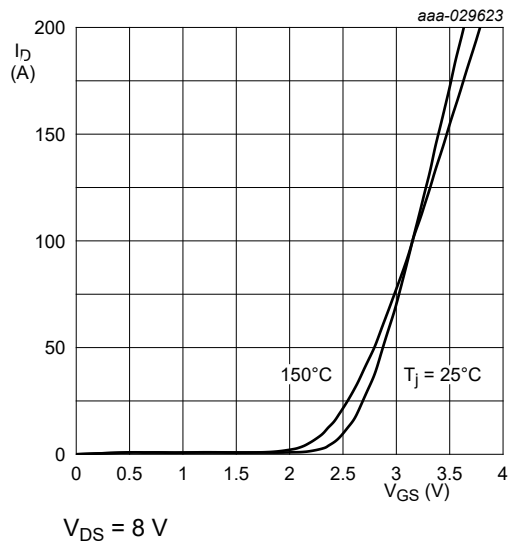


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

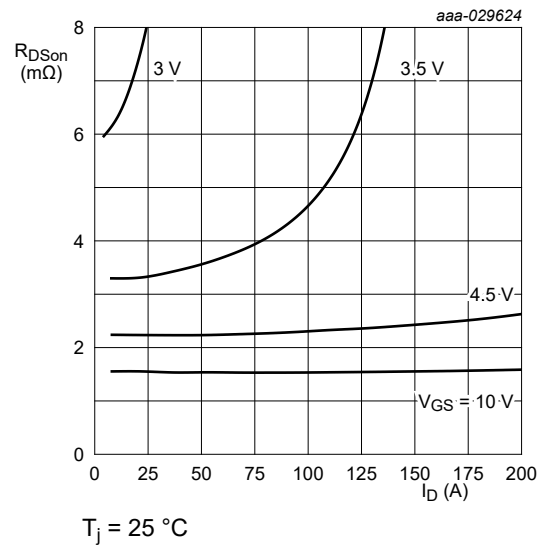


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

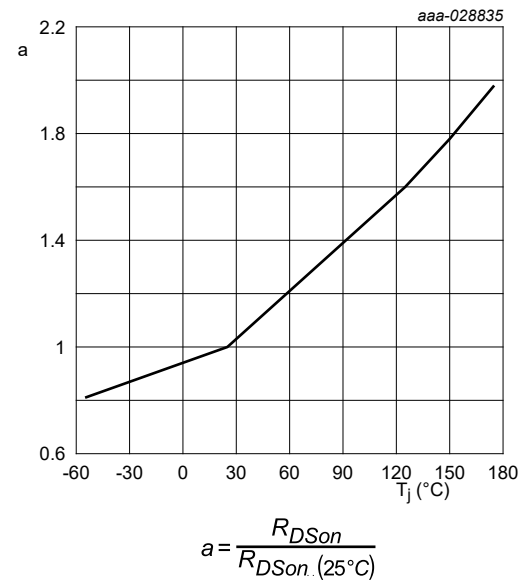


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

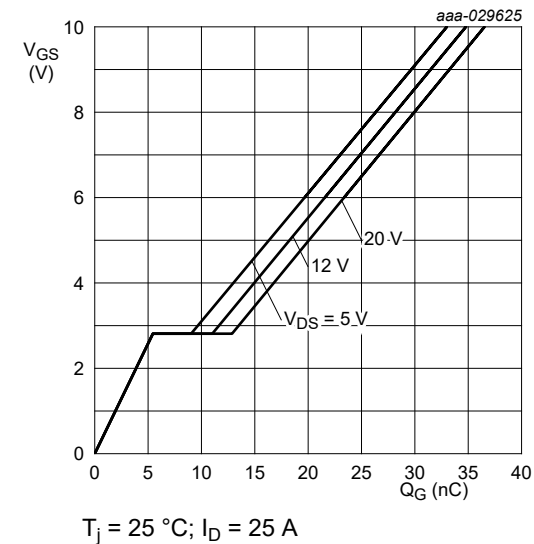


Fig. 12. Gate-source voltage as a function of gate charge; typical values

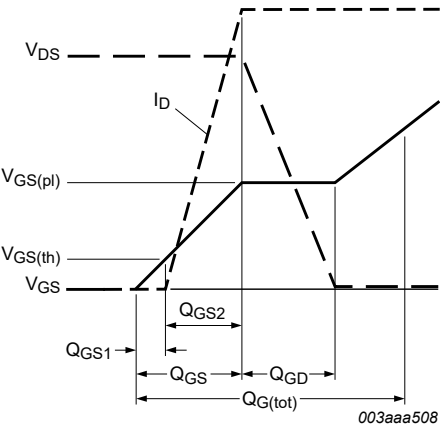
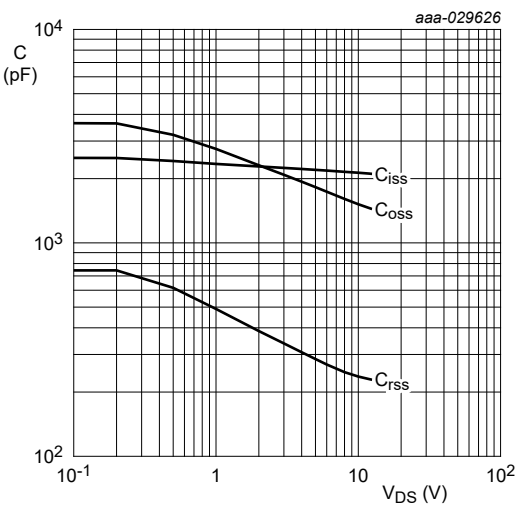
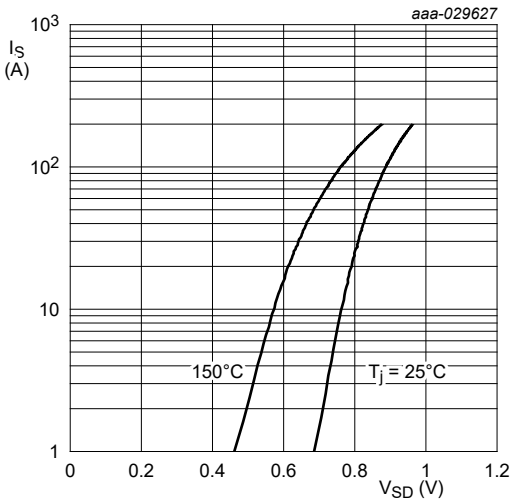


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

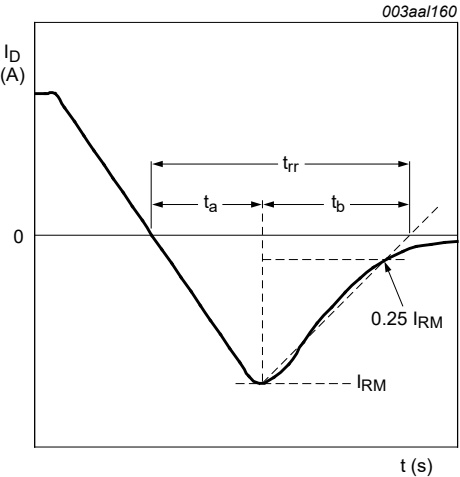


Fig. 16. Reverse recovery timing definition

11. Package outline



Fig. 17. Package outline LPAK33 (SOT1210)

12. Soldering

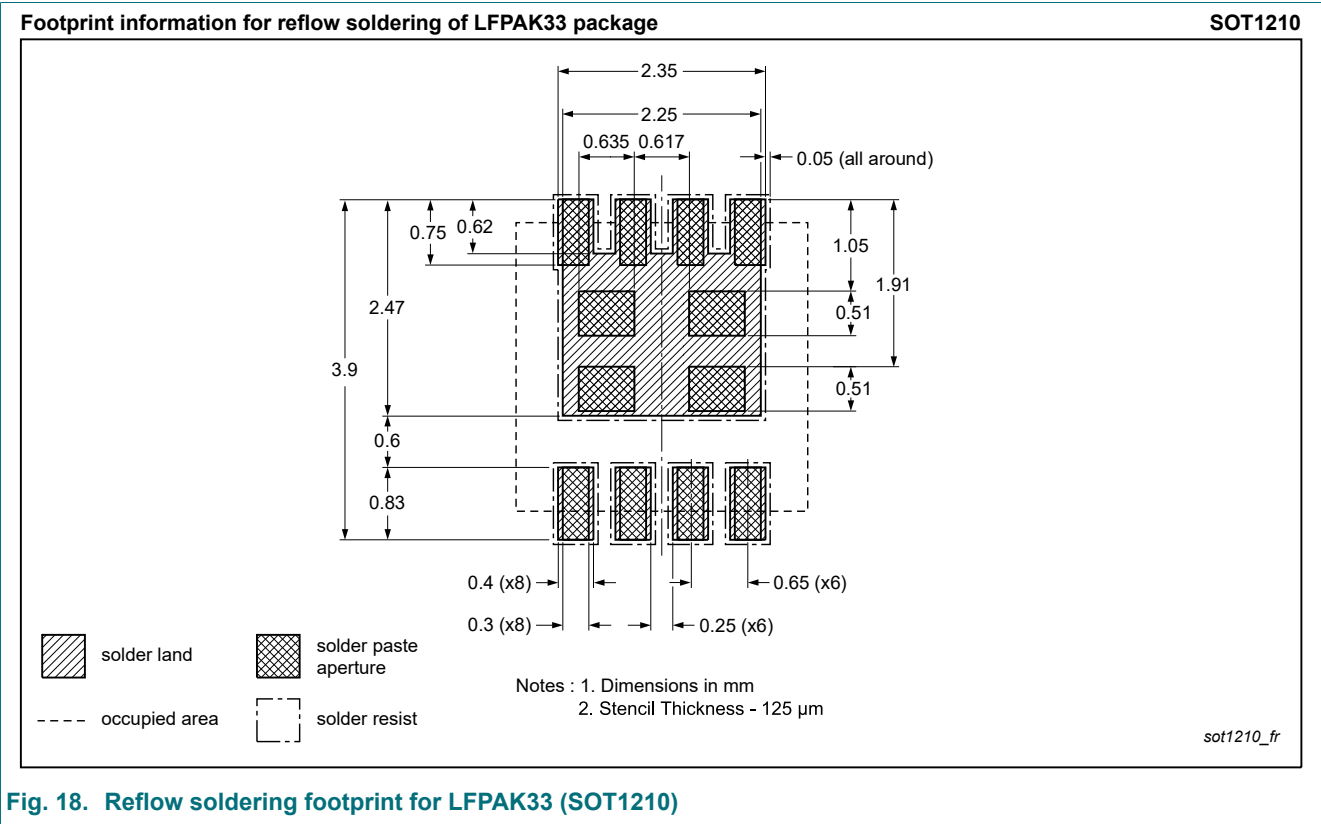


Fig. 18. Reflow soldering footprint for LPAK33 (SOT1210)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 30 September 2019

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