74LVT14

3.3 V hex inverter Schmitt trigger

Rev. 5 — 25 January 2024 Product data sheet

1. General description

The 74LVT14 is a hex inverter with Schmitt-trigger inputs. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Different positive and negative going input threshold voltages
- Tolerant of slow input transitions
- Wide supply voltage range from 2.7 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Output capability: +32 mA/-20 mA
- High noise immunity
- Direct interface with TTL levels
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT14D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT14PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT14BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

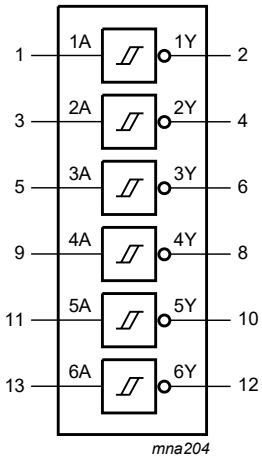


Fig. 1. Logic symbol

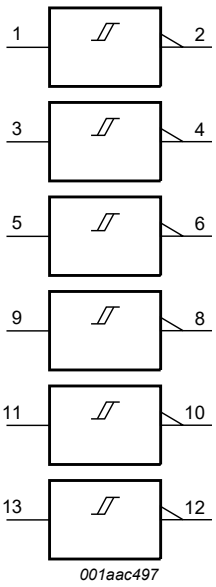


Fig. 2. IEC logic symbol

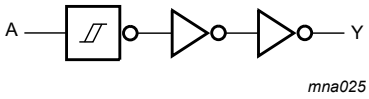
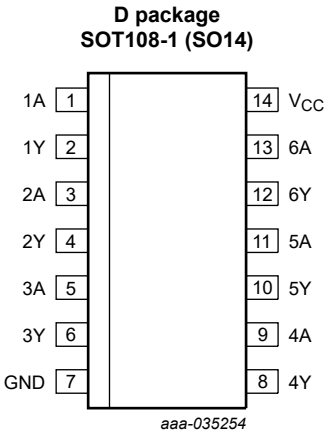
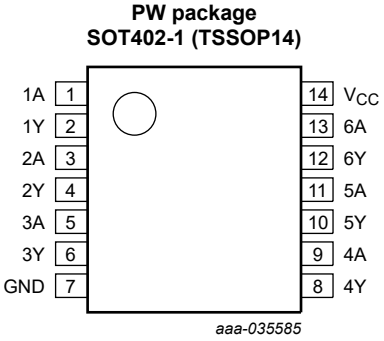


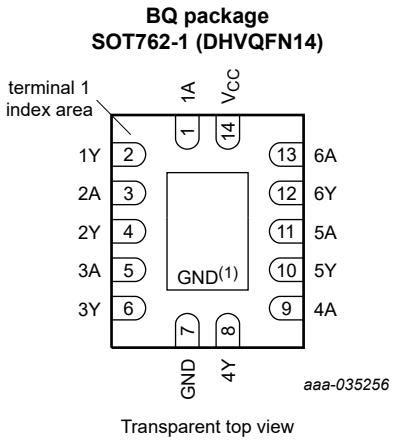
Fig. 3. Logic diagram (one inverter)

5. Pinning information

5.1. Pinning







(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V_{CC}	14	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level.

Inputs	Output
nA	**nY**
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF or HIGH state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
I_{OK}	output clamping current	V_O < 0 V	-50	-	mA
I_O	output current	output in LOW state	-	64	mA
		output in HIGH state	-32	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[2]	-	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C [3]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
[3] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-20	-	-	mA
I_{OL}	LOW-level output current		-	-	32	mA
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	output enabled	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V_{T+}	positive-going threshold voltage	V_{CC} = 3.3 V; see Fig. 4	1.5	1.7	2.0	V
V_{T-}	negative-going threshold voltage	V_{CC} = 3.3 V; see Fig. 4	0.9	1.1	1.3	V
V_H	hysteresis voltage	V_{CC} = 3.3 V; see Fig. 4	0.4	0.6	-	V
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA	-1.2	-	-	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = -100 µA	V_{CC} - 0.2	-	-	V
		V_{CC} = 2.7 V; I_{OH} = -6 mA	2.4	-	-	V
		V_{CC} = 3.0 V; I_{OH} = -20 mA	2.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA	-	-	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA	-	-	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA	-	-	0.5	V
I_I	input leakage current	V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	-	10	µA
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	-	±1	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	-	±100	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		outputs HIGH	-	-	0.02	mA
		outputs LOW	-	1.5	3	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input = V_{CC} - 0.6 V and other inputs at V_{CC} or GND [2]	-	-	0.2	mA
C_I	input capacitance	V_I = 0 V or 3.0 V	-	3	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.
[2] This is the increase in the supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

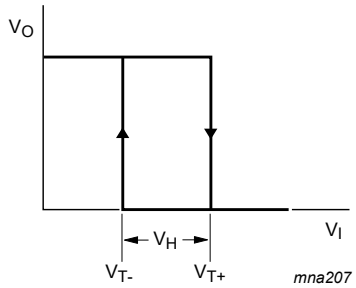
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

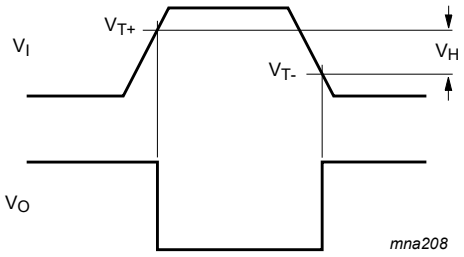
Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t_{PLH}	LOW to HIGH propagation delay	nA to nY; see Fig. 5				
		V_{CC} = 2.7 V	-	-	6.9	ns
		V_{CC} = 3.3 V + 0.3 V	1.0	3.8	5.7	ns
t_{PHL}	HIGH to LOW propagation delay	nA to nY; see Fig. 5				
		V_{CC} = 2.7 V	-	-	4.1	ns
		V_{CC} = 3.3 V + 0.3 V	1.0	3.2	4.5	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

10.1. Waveforms and test circuit

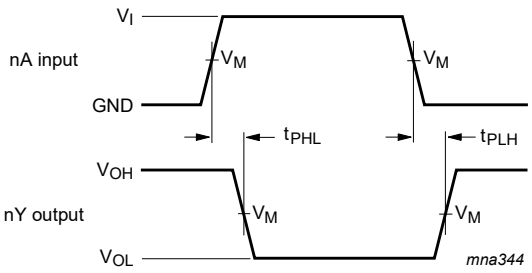


a. Transfer characteristics



b. Voltage levels

Fig. 4. Definition of V_{T+}, V_{T-} and V_H



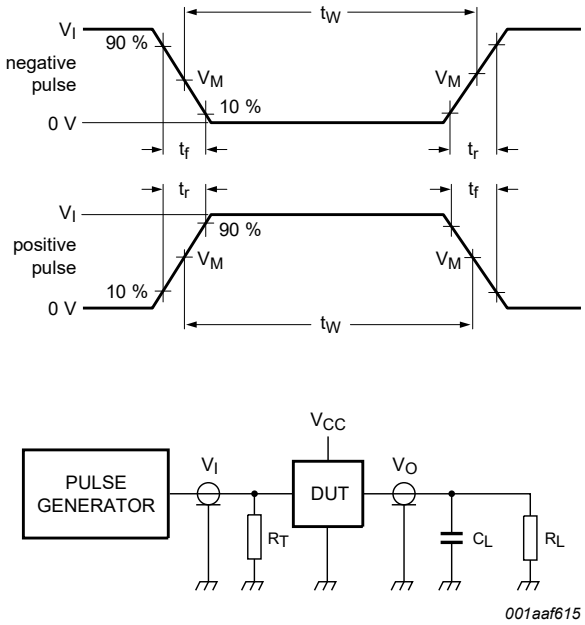
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. nA input to nY output propagation delays

Table 8. Measurement points

V_{CC}	Input	Output
	V_M	V_M
2.7 V to 3.6 V	1.5 V	1.5 V



Test data is given in given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

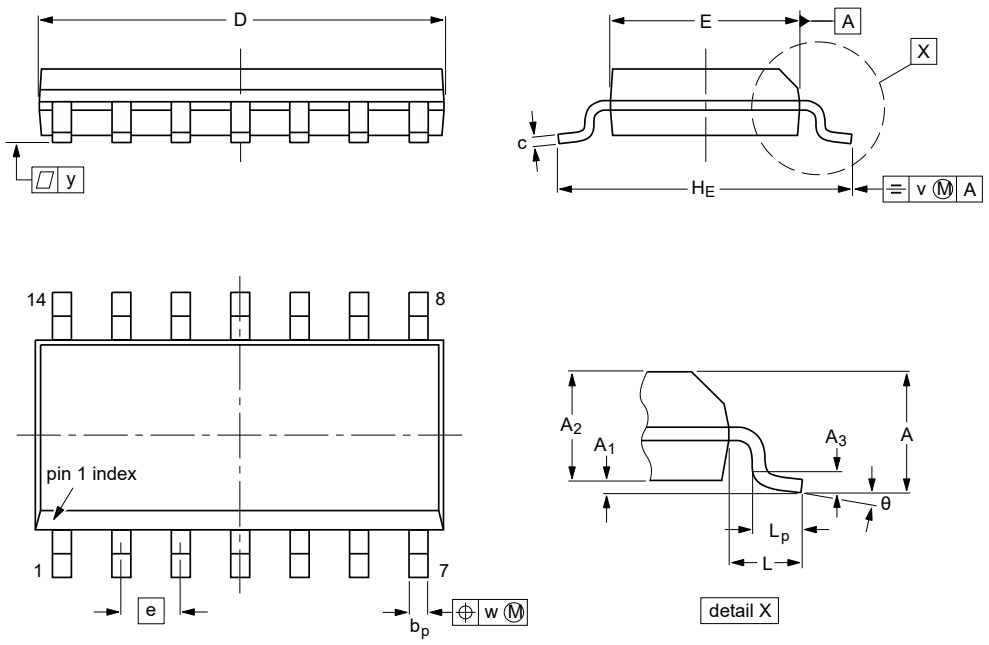
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply	Input				Load	
V_{CC}	V_I	f_i	t_W	t_r, t_f	R_L	C_L
2.7 V to 3.3 V	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

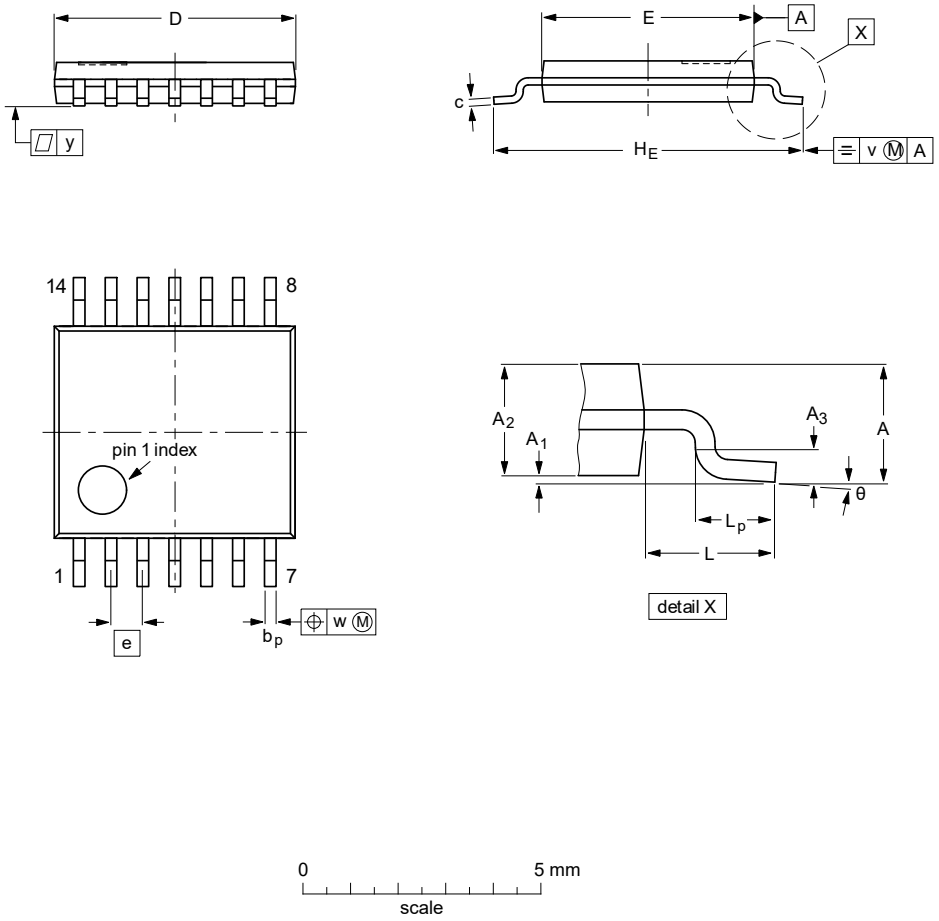
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

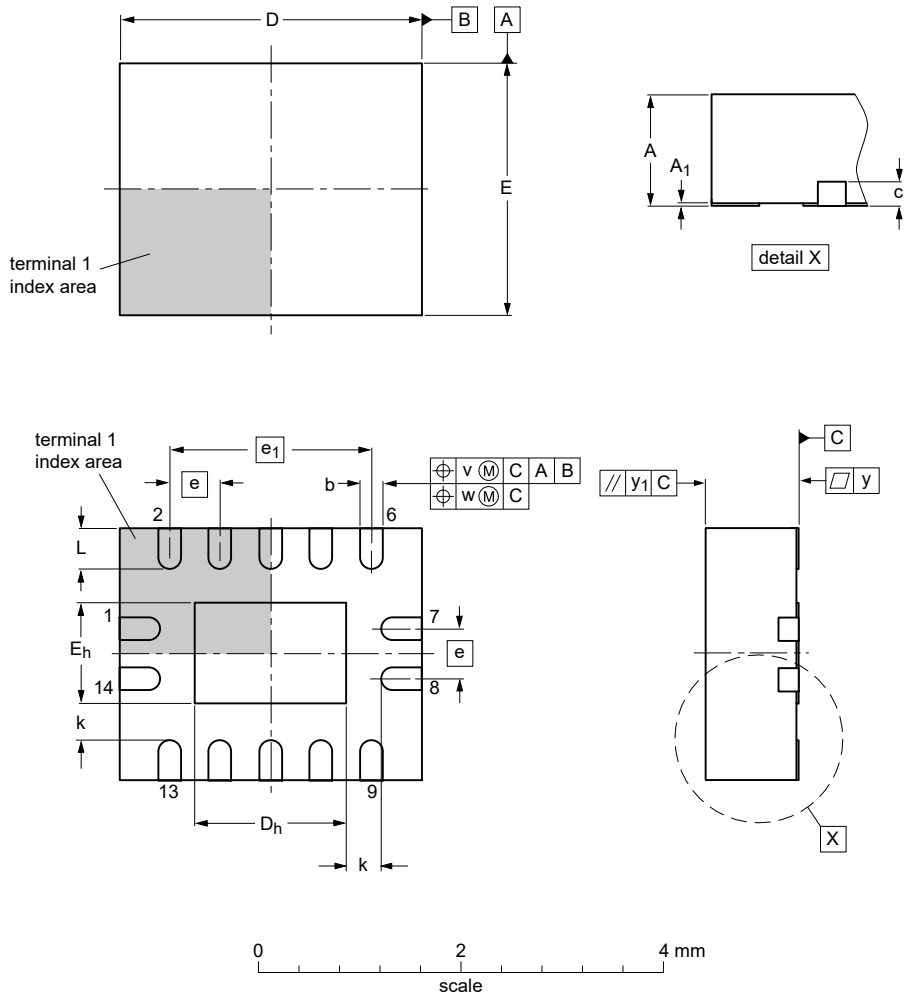
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 9. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT14 v.5	20240125	Product data sheet	-	74LVT14 v.4
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74LVT14 v.4	20210728	Product data sheet	-	74LVT14 v.3
Modifications:	• Type number 74LVT14DB (SOT337-1/SSOP14) removed. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation removed or updated.			
74LVT14 v.3	20180406	Product data sheet	-	74LVT14 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LVT14 v.2	20080425	Product data sheet	-	74LVT14 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Quick reference section removed. • DHVQFN14 package added to Section 3 and Section 11. • Section 12 added.			
74LVT14 v.1	19960828	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 25 January 2024

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