



# 74LVC2G38

Dual 2-input NAND gate; open drain

Rev. 16 — 30 April 2024

Product data sheet

## 1. General description

The 74LVC2G38 is a dual 2-input NAND gate with open-drain outputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- Open-drain outputs
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74LVC2G38DP</a>	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	<a href="#">SOT505-2</a>
<a href="#">74LVC2G38DC</a>	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<a href="#">SOT765-1</a>
<a href="#">74LVC2G38GT</a>	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	<a href="#">SOT833-1</a>
<a href="#">74LVC2G38GN</a>	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	<a href="#">SOT1116</a>
<a href="#">74LVC2G38GS</a>	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	<a href="#">SOT1203</a>
<a href="#">74LVC2G38GX</a>	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 × 0.8 × 0.32 mm	<a href="#">SOT1233-2</a>

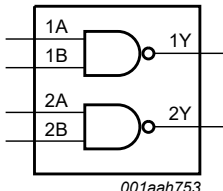
### 4. Marking

Table 2. Marking codes

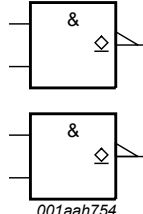
Type number	Marking code <sup>[1]</sup>
74LVC2G38DP	Y38
74LVC2G38DC	Y38
74LVC2G38GT	Y38
74LVC2G38GN	YB
74LVC2G38GS	YB
74LVC2G38GX	YB

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

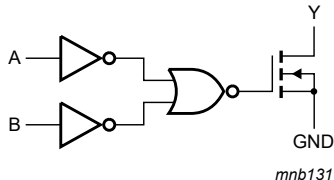
### 5. Functional diagram



**Fig. 1. Logic symbol**



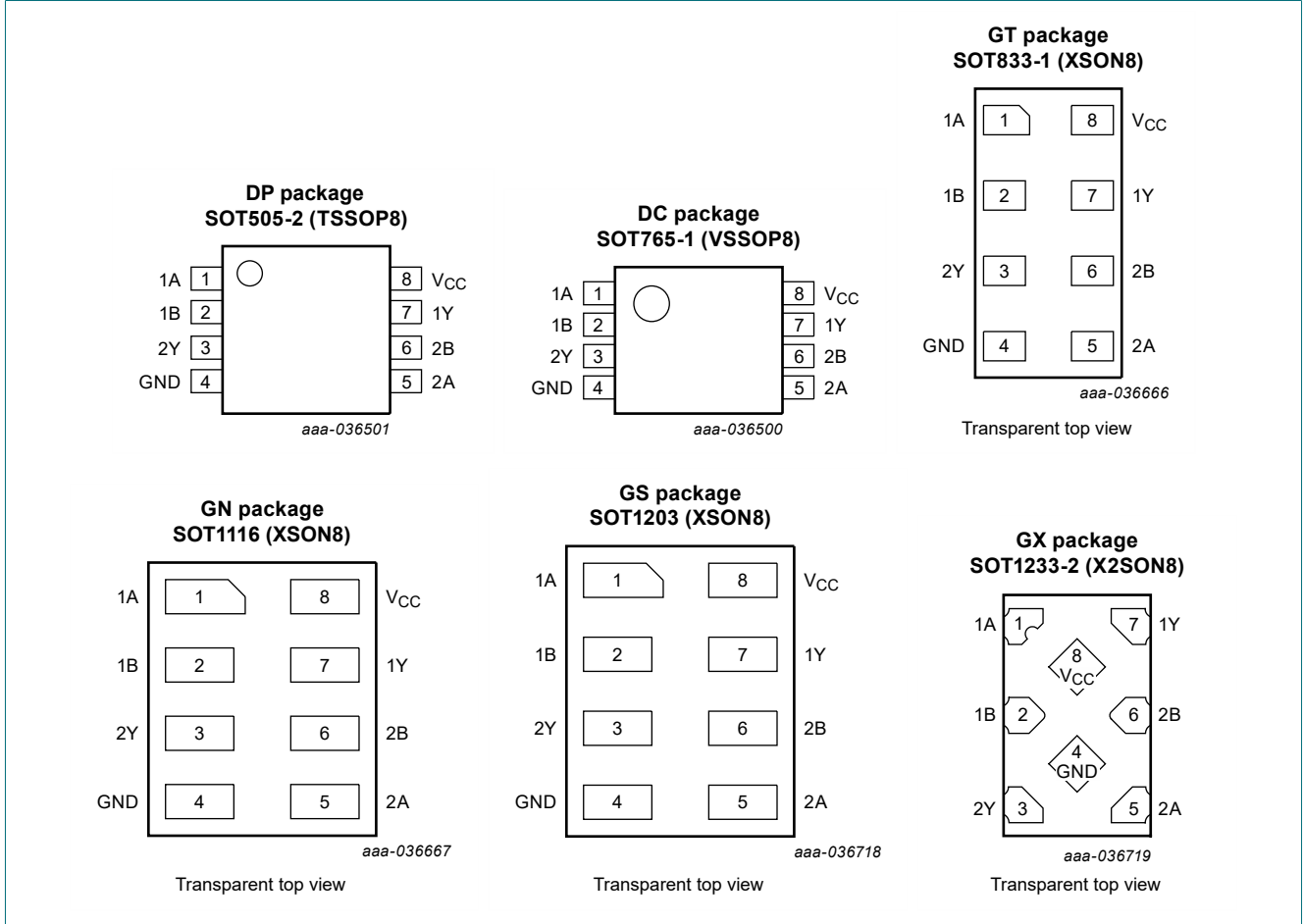
**Fig. 2. IEC logic symbol**



**Fig. 3. Functional diagram (one gate)**

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.*

Input		Output
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$V_I$	input voltage		[1] -0.5	+6.5	V
$V_O$	output voltage	Active mode	[1] -0.5	$V_{CC} + 0.5$	V
		Power-down mode; $V_{CC} = 0$ V	[1] -0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V or $V_O > V_{CC}$	-	$\pm 50$	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		SOT505-2 (TSSOP8) SOT765-1 (VSSOP8) SOT833-1 (XSON8) SOT1116 (XSON8) SOT1203 (XSON8)	[2] -	250	mW
		SOT1233-2 (X2SON8)	[3] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package:  $P_{tot}$  derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99 °C.

For SOT833-1 (XSON8) package:  $P_{tot}$  derates linearly with 3.1 mW/K above 68 °C.

For SOT1116 (XSON8) package:  $P_{tot}$  derates linearly with 4.2 mW/K above 90 °C.

For SOT1203 (XSON8) package:  $P_{tot}$  derates linearly with 3.6 mW/K above 81 °C.

[3] For SOT1233-2 (X2SON8) package:  $P_{tot}$  derates linearly with 7.7 mW/K above 118 °C.

## 9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		disable mode	0	5.5	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

## 10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3V_{CC}$	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	0.08	0.45	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	0.14	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.19	0.4	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	0.37	0.55	V
		$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	0.43	0.55	V
$I_I$	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	$\pm 0.1$	$\pm 1$	$\mu$ A
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	$\pm 0.1$	$\pm 2$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	$\pm 0.1$	$\pm 2$	$\mu$ A
$I_{CC}$	supply current	$V_I = 5.5$ V or GND; $V_{CC} = 1.65$ V to 5.5 V; $I_O = 0$ A	-	0.1	4	$\mu$ A
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.3$ V to 5.5 V; $I_O = 0$ A	-	5	500	$\mu$ A
$C_I$	input capacitance		-	2.5	-	pF

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.70	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.80	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	-	0.80	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±1	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	±0.1	±2	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	-	±2	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A	-	-	4	μA
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.3 V to 5.5 V; I <sub>O</sub> = 0 A	-	-	500	μA

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nA, nB to nY; see Fig. 4						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.2	3.0	8.6	1.2	10.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	1.8	4.8	0.7	6.0	ns
		V <sub>CC</sub> = 2.7 V	0.7	2.5	4.4	0.7	5.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.7	2.1	4.1	0.7	5.2	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nA, nB to nY; see Fig. 4						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.2	3.0	8.6	1.2	10.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	1.8	4.8	0.7	6.0	ns
		V <sub>CC</sub> = 2.7 V	0.7	2.5	4.4	0.7	5.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.7	2.1	4.1	0.7	5.2	ns
C <sub>PD</sub>	power dissipation capacitance	per gate; V <sub>I</sub> = GND to V <sub>CC</sub> [2]	-	5	-	-	-	pF

[1] Typical values are measured at nominal V<sub>CC</sub> and at T<sub>amb</sub> = 25 °C.

[2] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

∑(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

### 11.1. Waveforms and test circuit

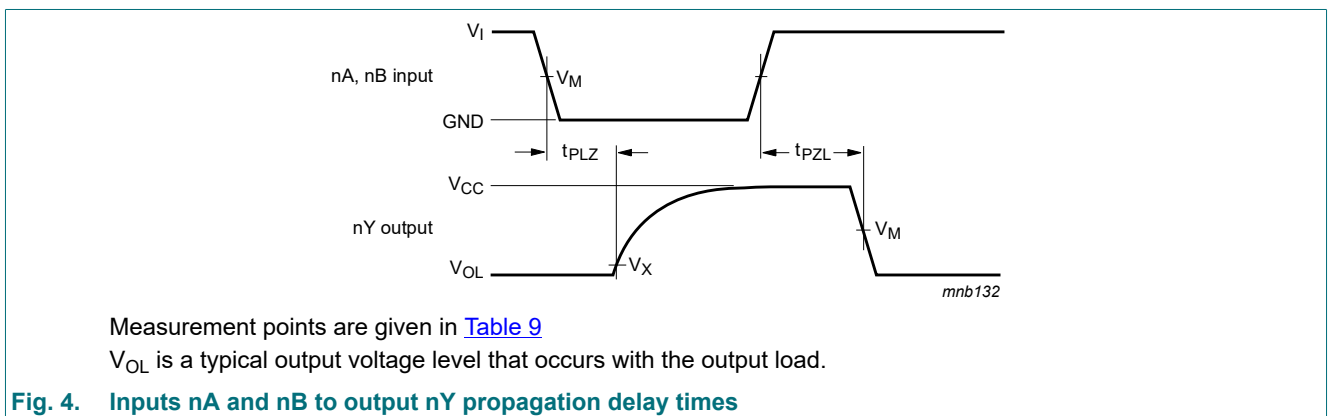


Table 9. Measurement points

Supply voltage	Input	Output	
$V_{CC}$	$V_M$	$V_X$	$V_M$
1.65 V to 1.95 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$0.5V_{CC}$
2.7 V	1.5 V	$V_{OL} + 0.3 V$	1.5 V
3.0 V to 3.6 V	1.5 V	$V_{OL} + 0.3 V$	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$0.5V_{CC}$

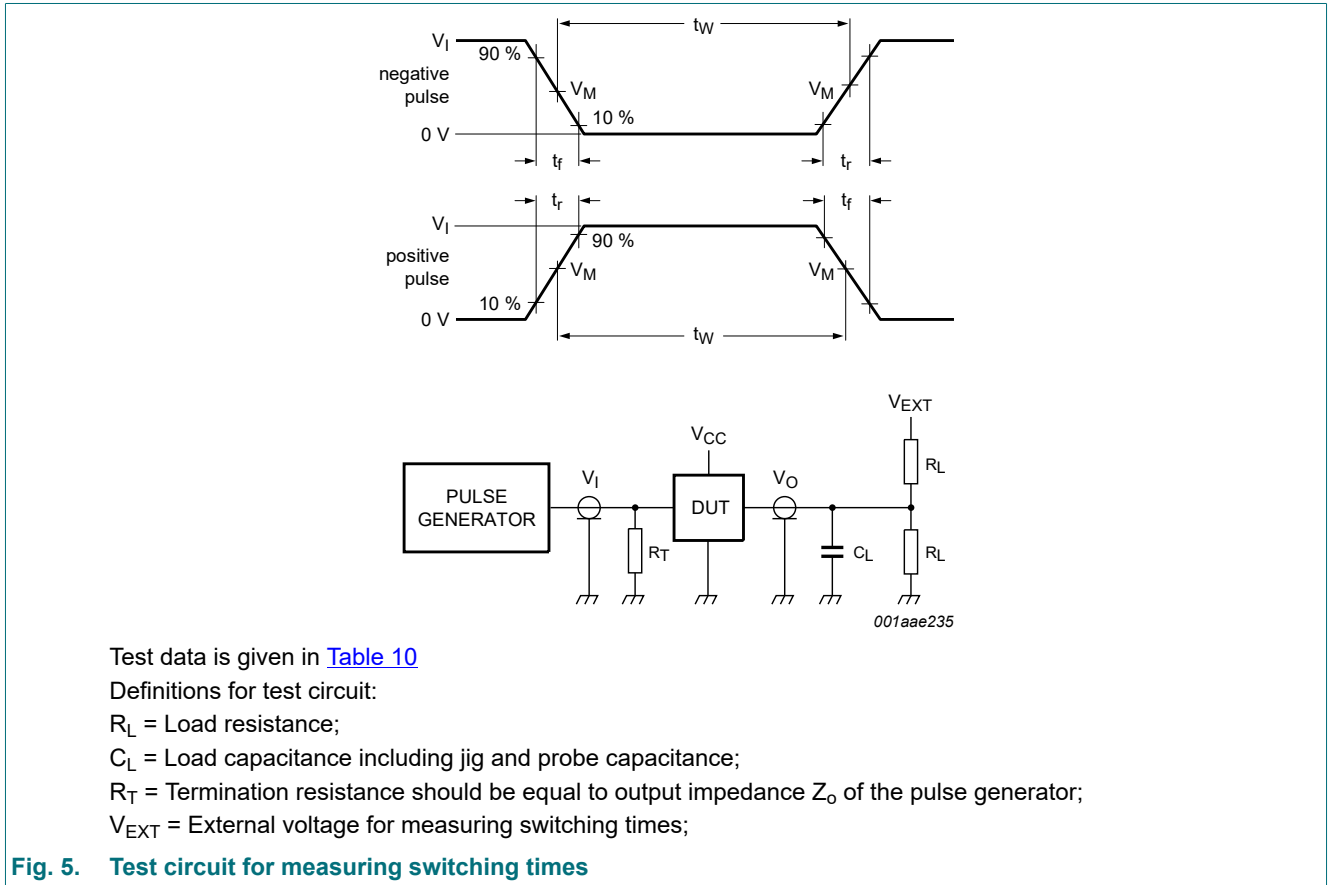


Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		$V_{EXT}$
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLZ}, t_{PZL}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0 \text{ ns}$	30 pF	1 k $\Omega$	$2V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0 \text{ ns}$	30 pF	500 $\Omega$	$2V_{CC}$
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	6 V
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	6 V
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	$2V_{CC}$



## 12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

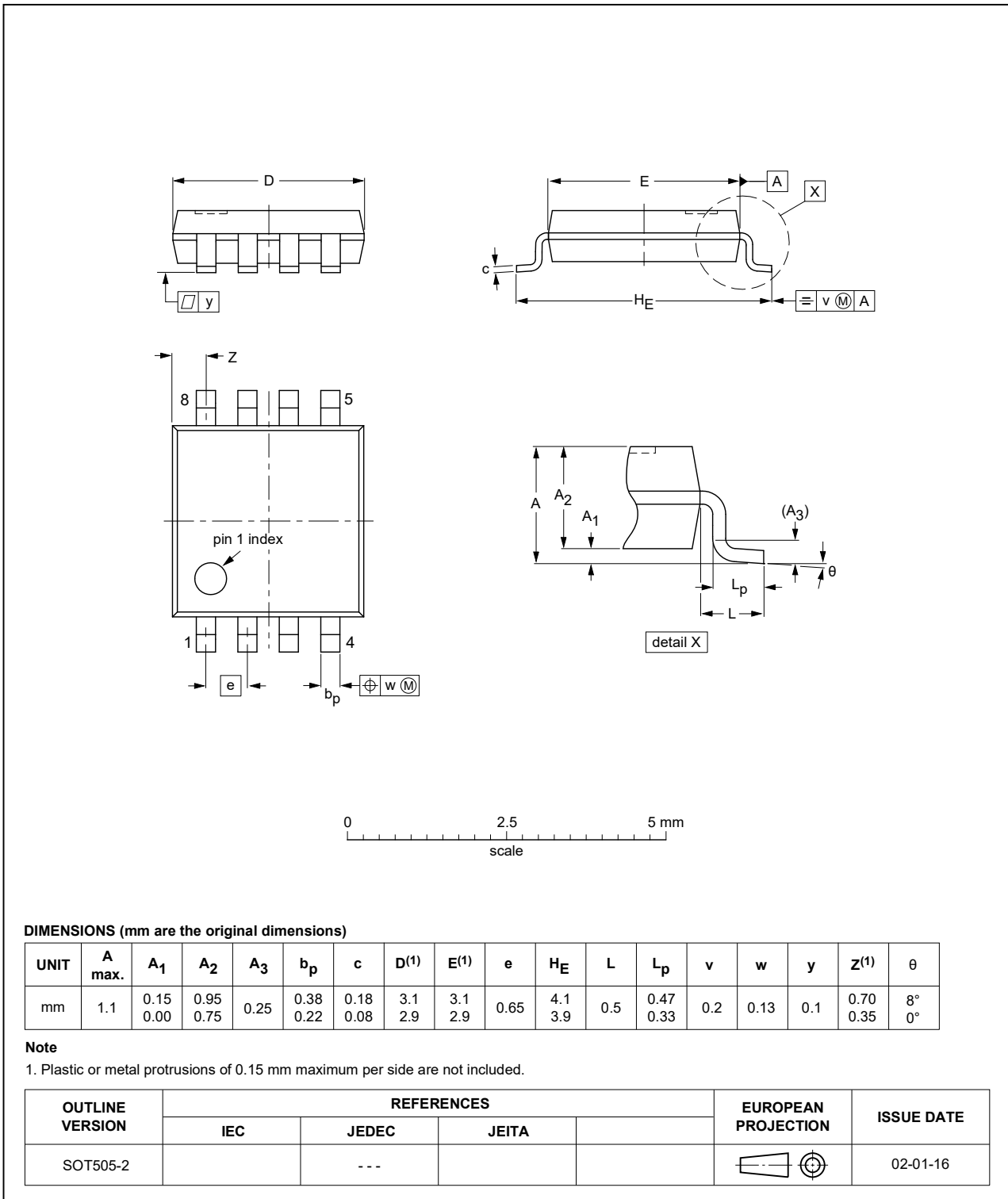


Fig. 6. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

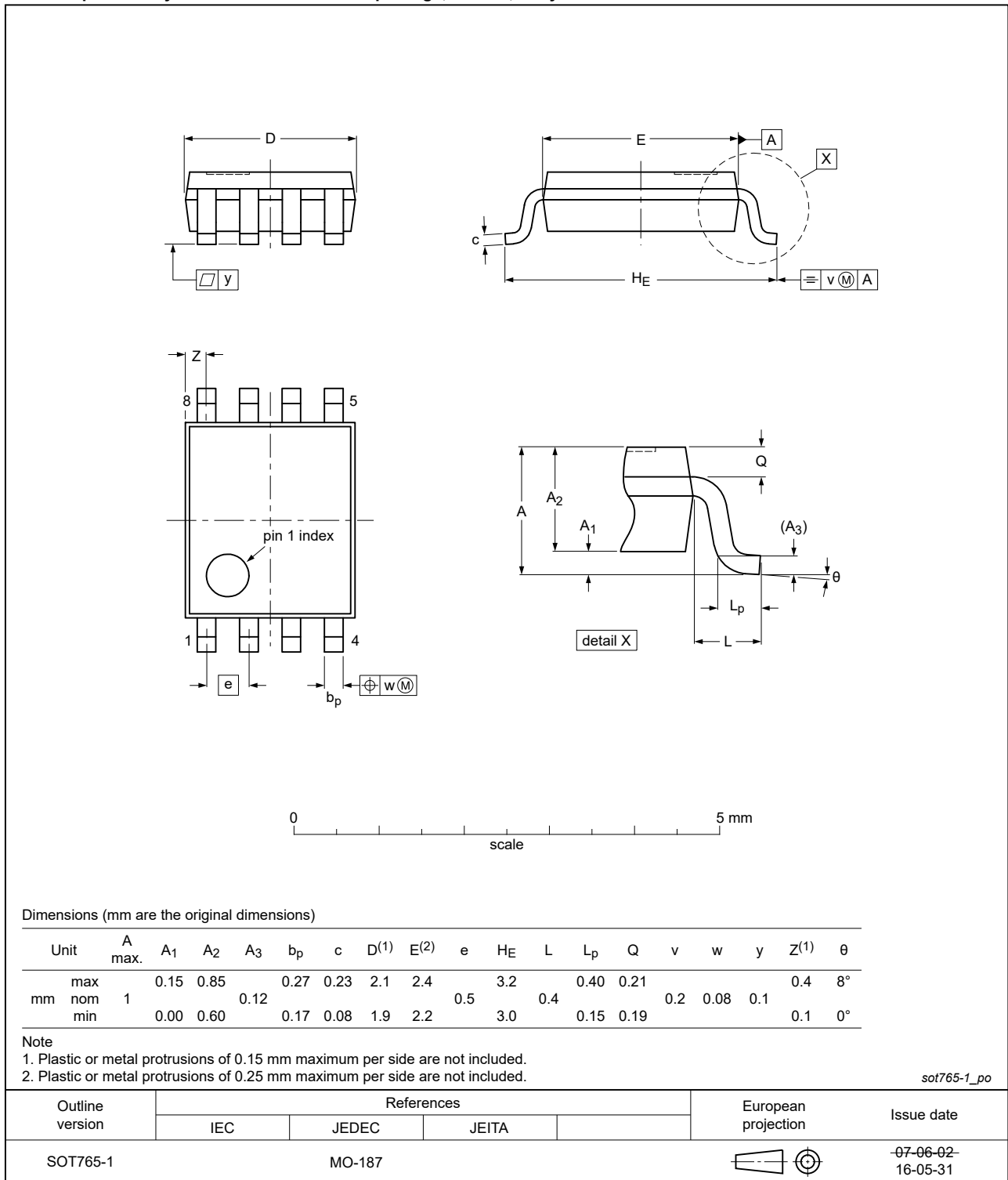


Fig. 7. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

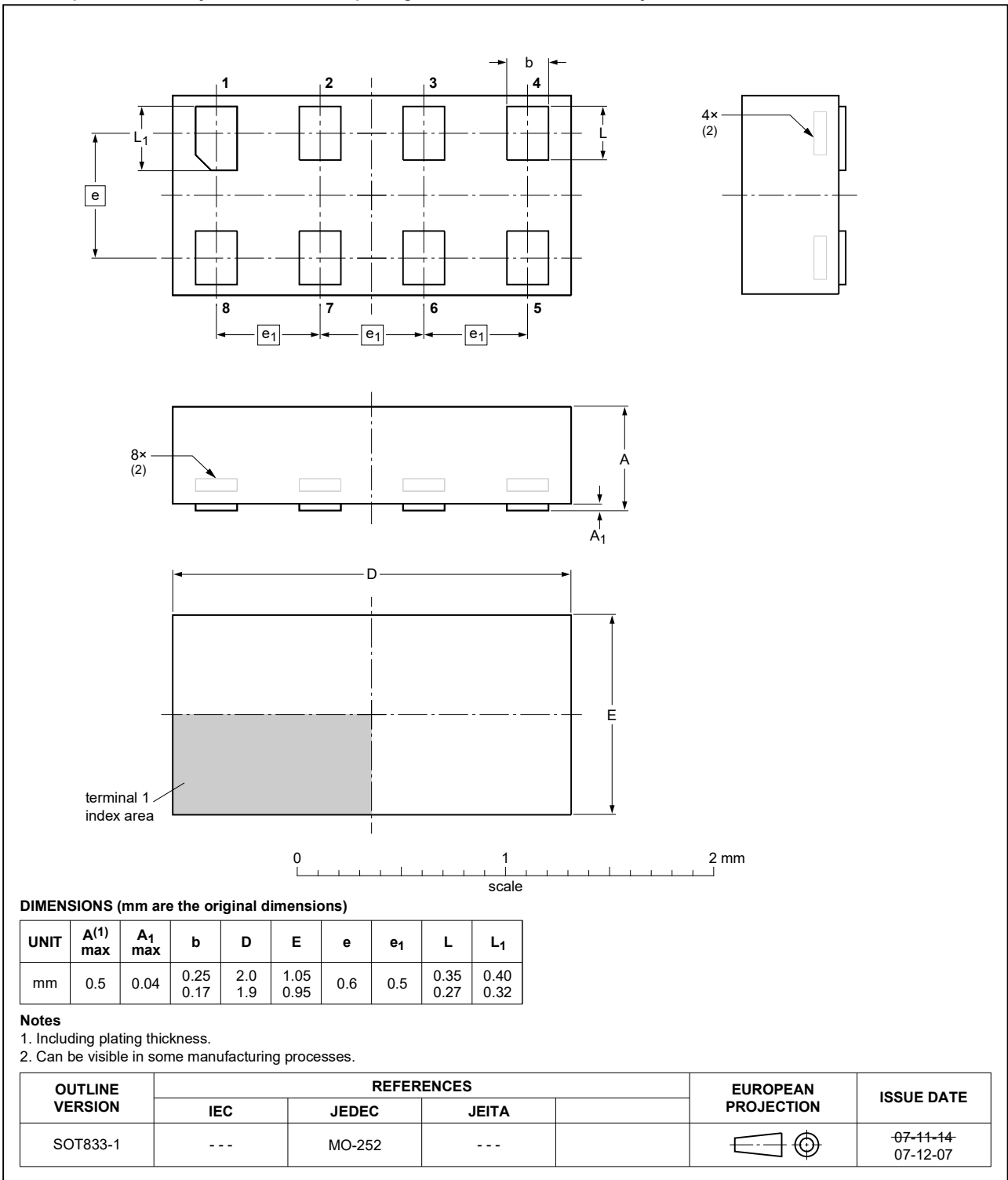


Fig. 8. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

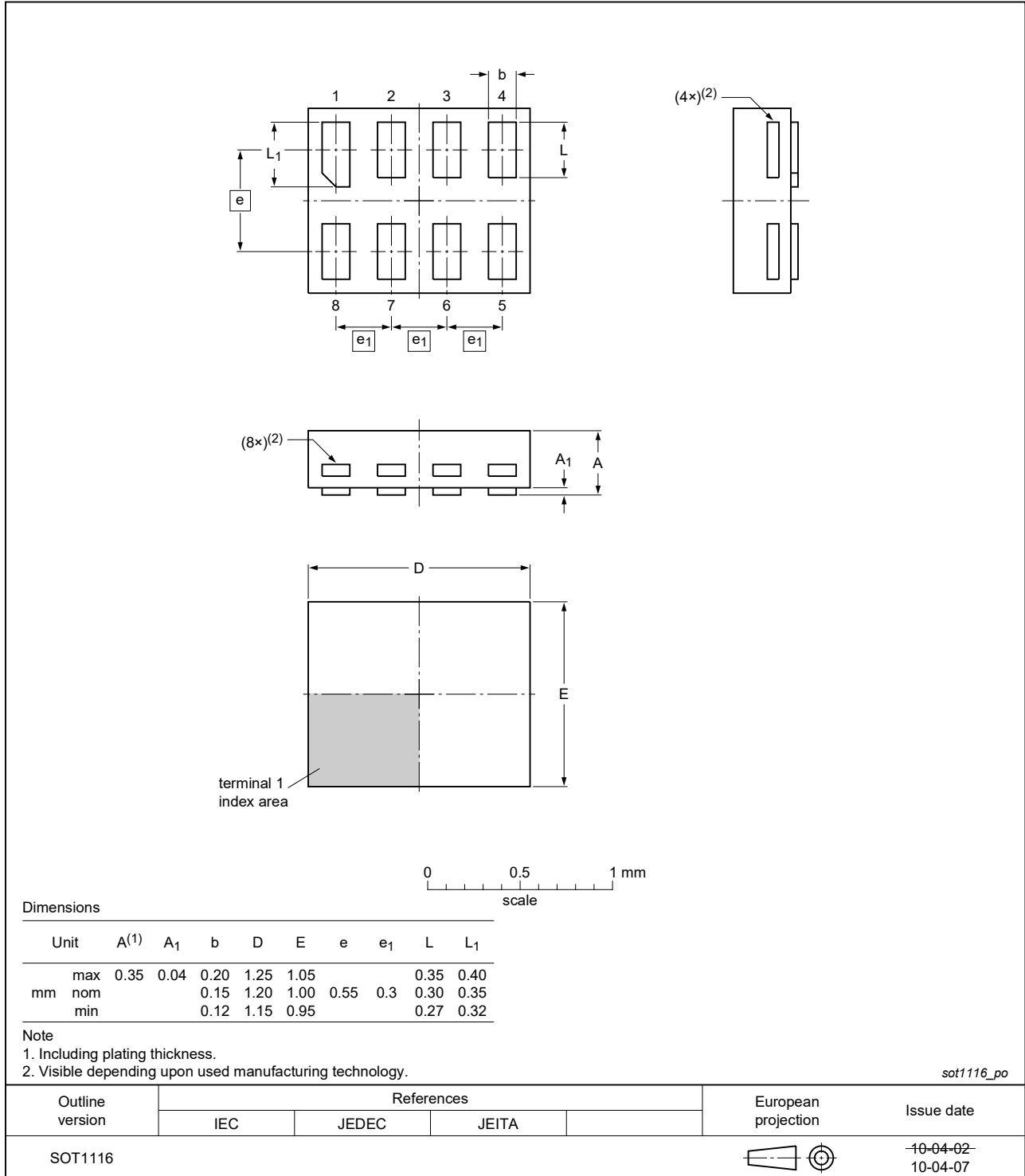


Fig. 9. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

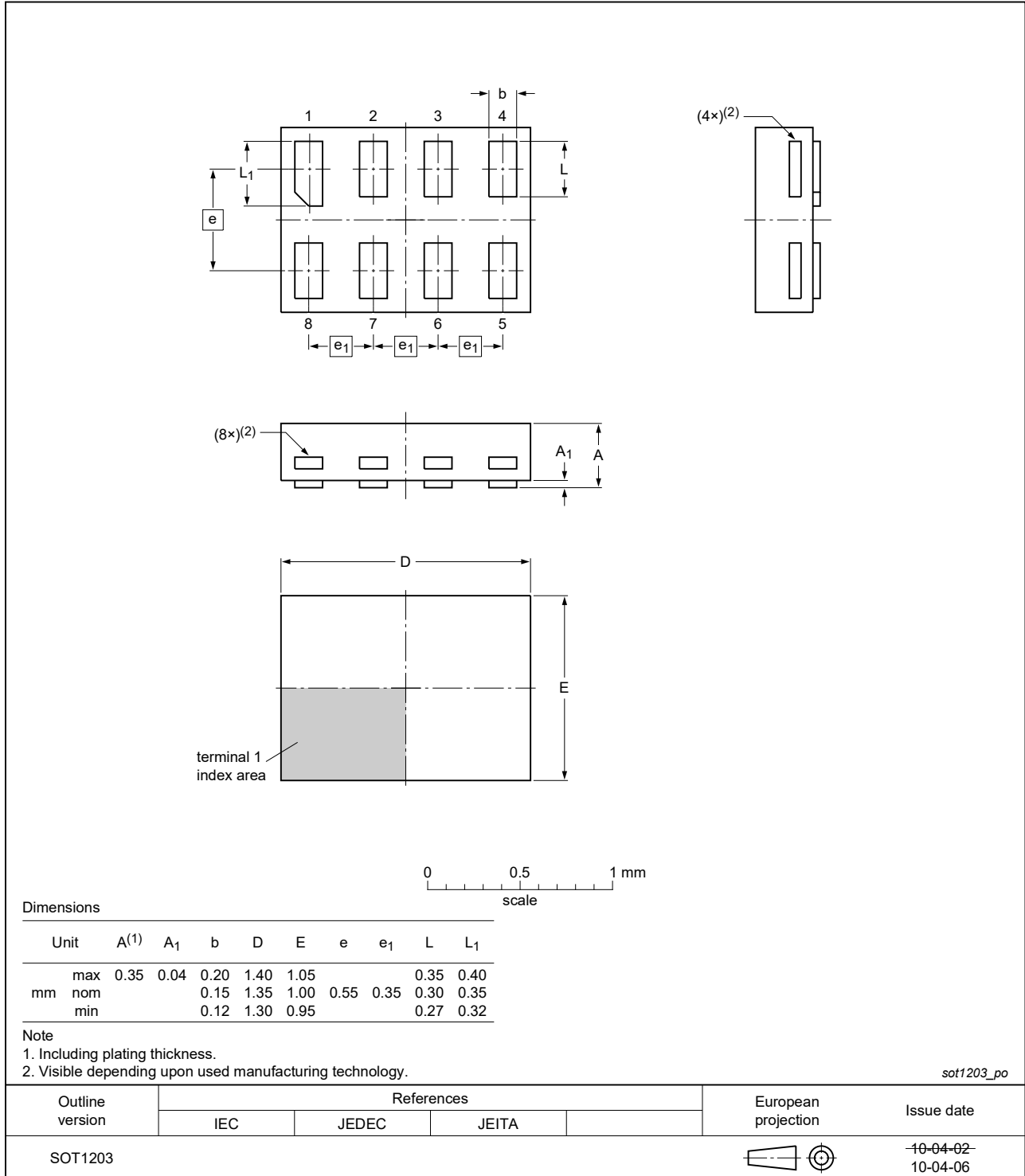


Fig. 10. Package outline SOT1203 (XSON8)

X2SON8: plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.32 mm

SOT1233-2

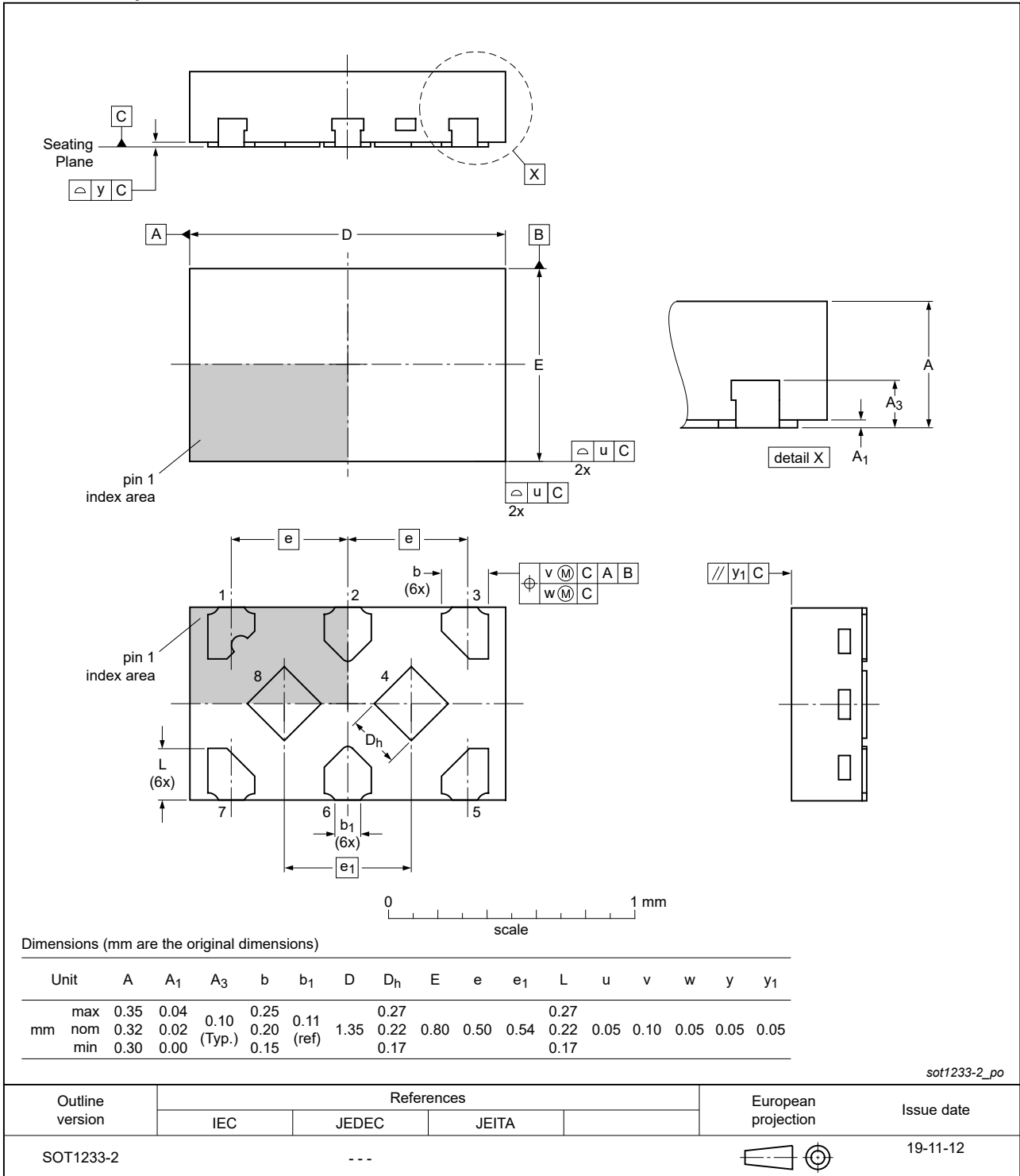


Fig. 11. Package outline SOT1233-2 (X2SON8)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G38 v.16	20240430	Product data sheet	-	74LVC2G38 v.15
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVC2G38GF (SOT1089/XSON8) removed.</li> </ul>			
74LVC2G38 v.15	20230828	Product data sheet	-	74LVC2G38 v.14
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li>Type number 74LVC2G38GM (SOT902-2/XQFN8) removed.</li> </ul>			
74LVC2G38 v.14	20220621	Product data sheet	-	74LVC2G38 v.13
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>SOT1233 (X2SON8) package changed to SOT1233-2 (X2SON8) package.</li> <li><a href="#">Table 5</a>: <math>P_{tot}</math> total power dissipation and derating values have been updated.</li> </ul>			
74LVC2G38 v.13	20170703	Product data sheet	-	74LVC2G38 v.12
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Added type number 74LVC2G38GX (SOT1233 / X2SON8).</li> <li>Type number 74LVC2G38GD removed.</li> </ul>			
74LVC2G38 v.12	20161215	Product data sheet	-	74LVC2G38 v.11
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC2G38 v.11	20130408	Product data sheet	-	74LVC2G38 v.10
Modifications:	<ul style="list-style-type: none"> <li>For type number 74LVC2G38GD XSON8U has changed to XSON8.</li> </ul>			
74LVC2G38 v.10	20120628	Product data sheet	-	74LVC2G38 v.9
Modifications:	<ul style="list-style-type: none"> <li>For type number 74LVC2G38GM the SOT code has changed to SOT902-2.</li> </ul>			
74LVC2G38 v.9	20111128	Product data sheet	-	74LVC2G38 v.8
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74LVC2G38 v.8	20101104	Product data sheet	-	74LVC2G38 v.7
74LVC2G38 v.7	20090320	Product data sheet	-	74LVC2G38 v.6
74LVC2G38 v.6	20080219	Product data sheet	-	74LVC2G38 v.5
74LVC2G38 v.5	20070904	Product data sheet	-	74LVC2G38 v.4
74LVC2G38 v.4	20060516	Product data sheet	-	74LVC2G38 v.3
74LVC2G38 v.3	20050201	Product specification	-	74LVC2G38 v.2
74LVC2G38 v.2	20041018	Product specification	-	74LVC2G38 v.1

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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