

PEMH15 $NPN/NPN \text{ resistor-equipped double transistor; R1 = 4.7 k}\Omega, R2 = 4.7 k}\Omega$

Product data sheet

1. General description

NPN/NPN Resistor-Equipped Transistor (RET) in a SOT666 ultra small and flat lead Surface Mounted Device (SMD) plastic package.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- · Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
Per transistor	er transistor							
V _{CEO}	collector-emitter voltage	open base		-	-	50	V	
Io	output current			-	-	100	mA	
R1	bias resistor 1 (input)	T _{amb} = 25 °C	[1]	3.3	4.7	6.1	kΩ	
R2/R1	bias resistor ratio		[1]	0.8	1	1.2		

[1] See "Section 11: Test information" for resistor calculation and test conditions.



NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		O1 I2 GND2
2	I1	input (base) TR1	6 5 4	
3	O2	output (collector) TR2		R1 R2
4	GND2	GND (emitter) TR2		TR2
5	12	input (base) TR2		TR1 R2 R1
6	01	output (collector) TR1	1 2 3	
			SOT666	
				GND1 I1 O2 sym063

6. Ordering information

Table 3. Ordering information

Type number	Package						
	Name	Description	Version				
PEMH15		plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	<u>SOT666</u>				

7. Marking

Table 4. Marking codes

Type number	Marking code
PEMH15	5F

NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

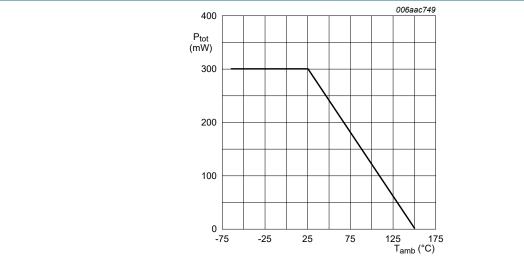
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transisto	or			'		
V _{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage	positive		-	30	V
		negative		-	-10	V
Io	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] [2]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} = 25 °C	[1] [2]	-	300	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.
- [2] Reflow soldering is the only recommended soldering method.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

Fig. 1. Per device: Power derating curve

NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	625	K/W
Per device	Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	417	K/W

- [1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.
- [2] Reflow soldering is the only recommended soldering method.

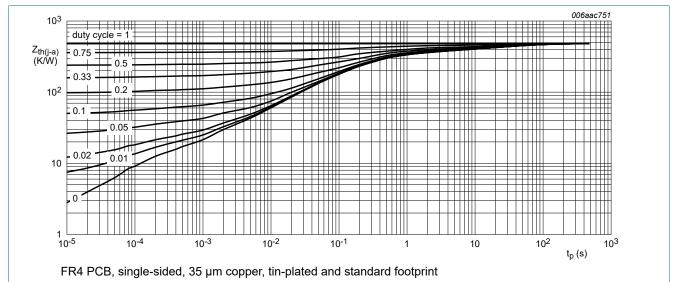


Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transist	or						
V _{(BR)CBO}	collector-base breakdown voltage	I _C = 100 μA; I _E = 0 A; T _{amb} = 25 °C		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		50	-	-	V
I _{CBO}	collector-base cut-off current	$V_{CB} = 50 \text{ V}; I_{E} = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		-	-	100	nA
I _{CEO}	collector-emitter cut-off	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C		-	-	1	μΑ
	current	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 150 °C		-	-	5	μΑ
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A		-	-	900	μA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 10 mA; T _{amb} = 25 °C		30	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		-	-	150	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C		-	1.1	0.5	V
V _{I(on)}	on-state input voltage	V _{CE} = 0.3 V; I _C = 20 mA; T _{amb} = 25 °C		2.5	1.9	-	V
R1	bias resistor 1 (input)	T _{amb} = 25 °C	[1]	3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C _c	collector capacitance	V_{CB} = 10 V; I_{E} = 0 A; i_{e} = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF
f _T	transition frequency	V _{CE} = 5 V; I _C = 10 mA; f = 100 MHz; T _{amb} = 25 °C	[2]	-	230	-	MHz

- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor

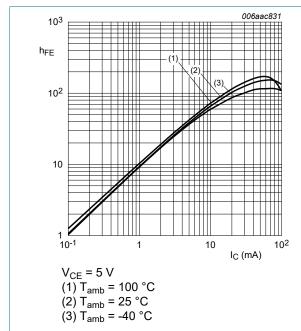


Fig. 3. DC current gain as a function of collector current; typical values

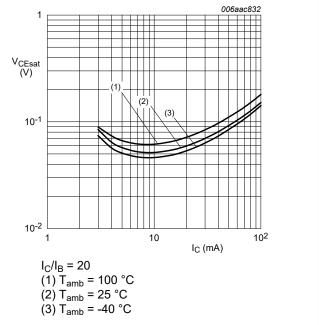
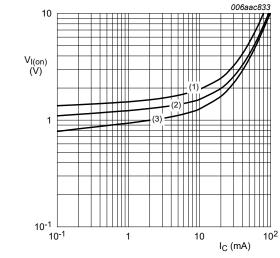


Fig. 4. Collector-emitter saturation voltage as a function of collector current; typical values

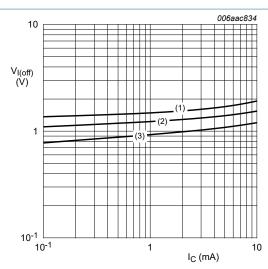
NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω



 $V_{CE} = 0.3 V$

(1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C





V_{CE} = 5 V (1) T_{amb} = -40 °C (2) T_{amb} = 25 °C

(3) $T_{amb} = 100 \, ^{\circ}C$

Off-state input voltage as a function of collector current; typical values

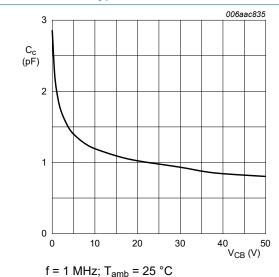
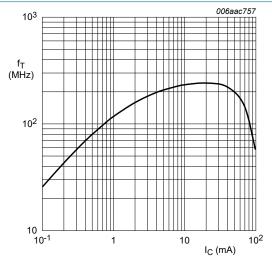


Fig. 7. Collector capacitance as a function of collector- Fig. 8. base voltage; typical values



 V_{CE} = 5 V; T_{amb} = 25 °C

Transition frequency as a function of collector current; typical values of built-in transistor

NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

11. Test information

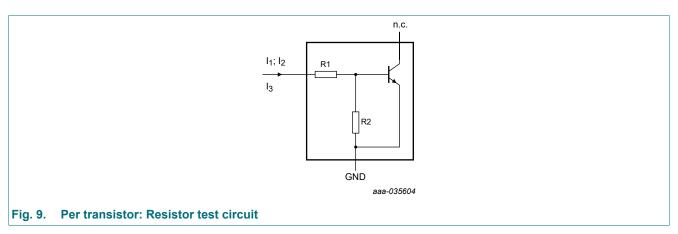
Resistor calculation

· Calculation of bias resistor 1 (R1)

$$R_{I} = \frac{V(I_{2}) - V(I_{1})}{I_{2} - I_{1}}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I3)}{R1 \cdot I3} - 1$$

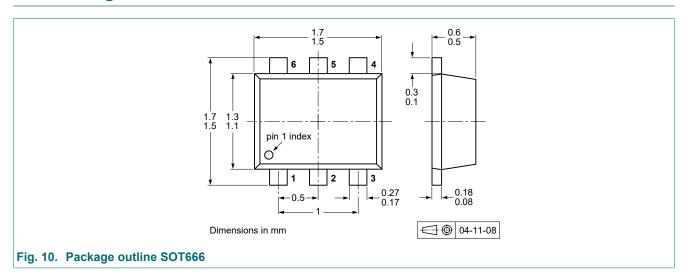


Resistor test conditions

Table 8. Resistor test conditions

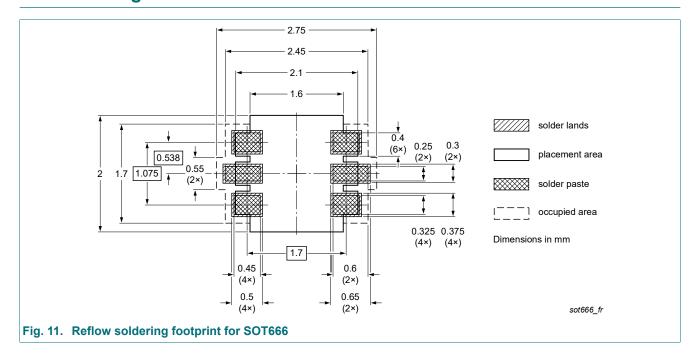
Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	l ₂	l ₃	
PEMH15	4.7	4.7	750 μΑ	950 μΑ	-850 μΑ	

12. Package outline



NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

13. Soldering



NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

14. Revision history

Table 9. Revision history

Table 5. Revision history							
Data sheet ID	Release date		Change notice	Supersedes			
PEMH15 v.7	20221229	Product data sheet	-	PEMH15 v.6			
Modifications:	 Product chan 	ged to non-automotive	qualification				
PEMH15 v.6	20220511	Product data sheet	-	PEMH15_PUMH15 v.5			
PEMH15_PUMH15 v.5	20111220	Product data sheet	-	PEMH15_PUMH15 v.4			
PEMH15_PUMH15 v.4	20031020	Product data sheet	-	PEMH15_PUMH15 v.3			
PEMH15_PUMH15 v.3	20011022	Product data sheet	-	PUMH15 v.2			
PUMH15 v.2	20000801	Product specification	-	PUMH15 v.1			
PUMH15 v.1	20031009	Product specification	-	-			

NPN/NPN resistor-equipped double transistor; R1 = 4.7 k Ω , R2 = 4.7 k Ω

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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