

74ALVC245

Octal bus transceiver; 3-state

Rev. 4 — 10 July 2023

Product data sheet

1. General description

The 74ALVC245 is an 8-bit transceiver with 3-state outputs. The device features an output enable ($\overline{OE}$) and send/receive (DIR) for direction control. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

Schmitt trigger action on all inputs makes the device tolerant of slow rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

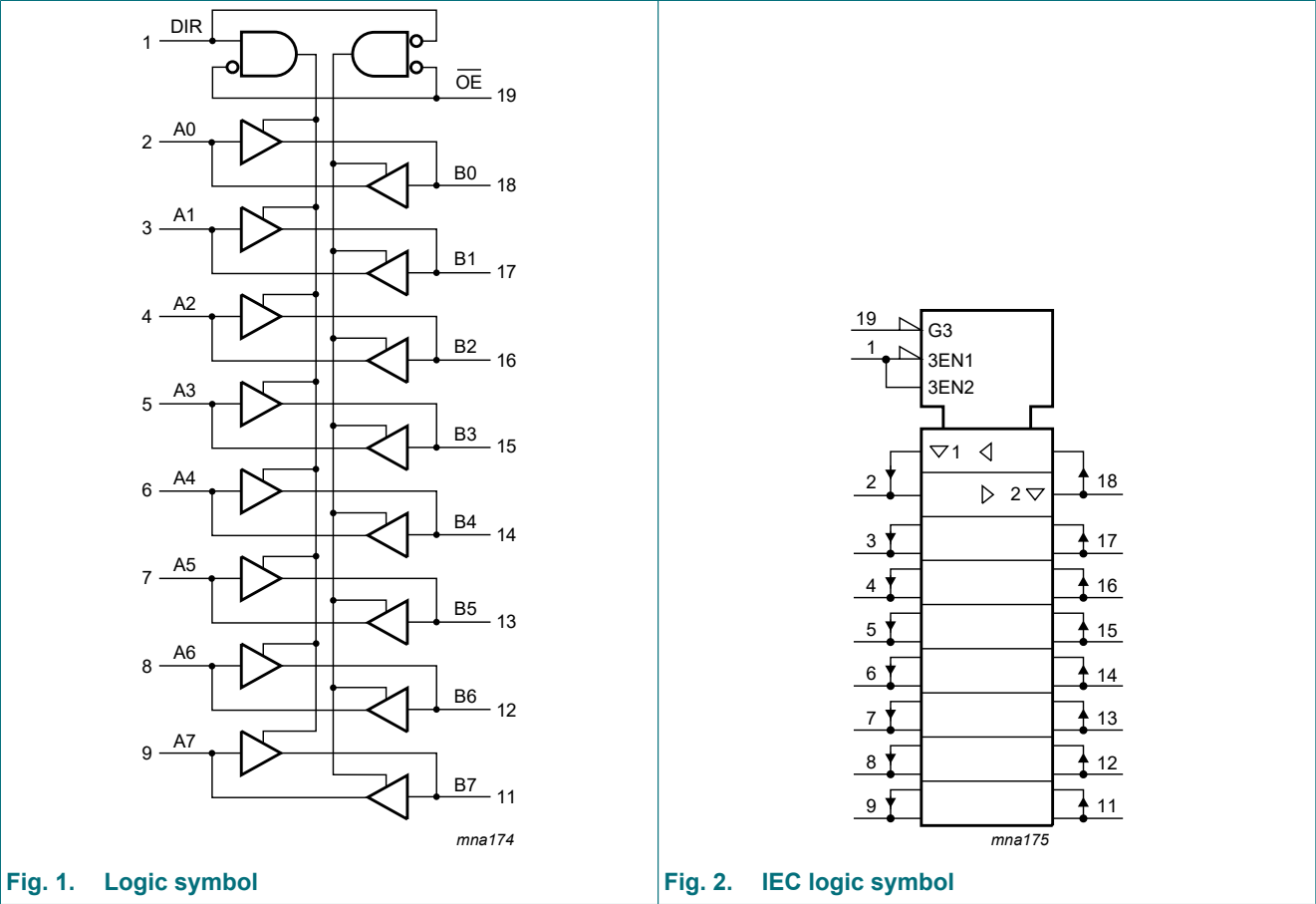
- Wide supply voltage range from 1.65 V to 3.6 V
- CMOS low power dissipation
- Overvoltage tolerant inputs to 3.6 V
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD78 Class II.A
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.5 V)
 - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

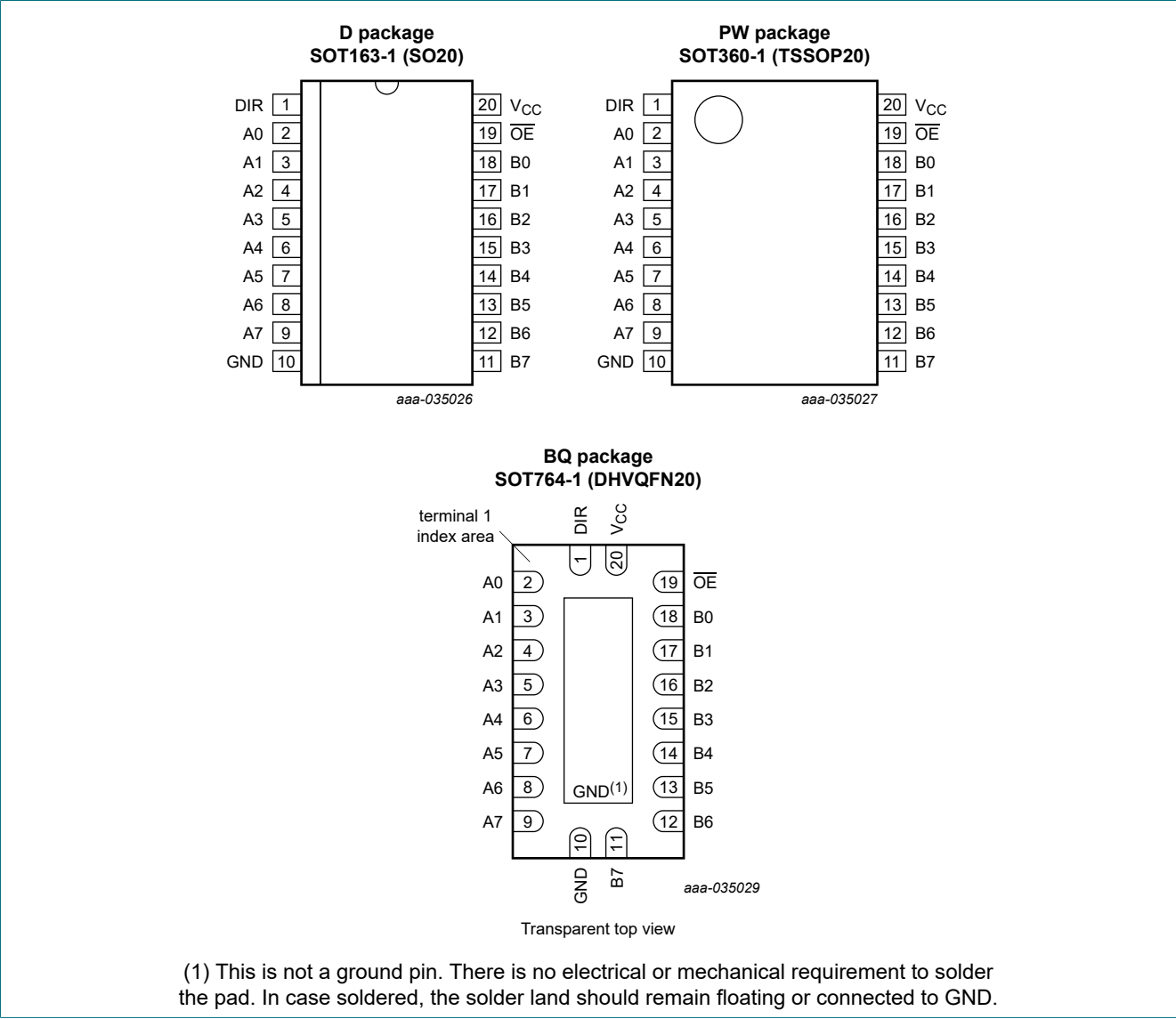
Type number	Package			
	Temperature range	Name	Description	Version
74ALVC245D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC245PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC245BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
GND	10	ground (0 V)
OE	19	output enable input (active LOW)
VCC	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Input/output	
OE	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		[1] -0.5	+4.6	V
V _O	output voltage	output HIGH or LOW state	[1] -0.5	V _{CC} + 0.5	V
		output 3-state	[1] -0.5	+4.6	V
		power-down mode; V _{CC} = 0 V	-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.65	3.6	V
V _I	input voltage		0	3.6	V
V _O	output voltage	output HIGH or LOW state	0	V _{CC}	V
		output 3-state	0	3.6	V
		power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature	in free air	-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.2	-	V
		I _O = -6 mA; V _{CC} = 1.65 V	1.25	-	-	1.25	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	1.8	-	-	1.8	-	V
		I _O = -18 mA; V _{CC} = 2.3 V	1.7	-	-	1.7	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.2	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.4	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.2	V
		I _O = 6 mA; V _{CC} = 1.65 V	-	-	0.3	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	-	0.4	-	0.4	V
		I _O = 18 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.6	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.4	V
		I _O = 18 mA; V _{CC} = 3.0 V	-	-	0.4	-	0.45	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.55	V
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 1.65 V to 3.6 V; V _O = 3.6 V or GND [2]	-	±0.1	±10.0	-	±80	µA
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 3.6 V	-	±0.1	±5.0	-	±20	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	±0.1	±10.0	-	±80	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V	-	0.2	10	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	750	-	750	µA
C _I	input capacitance		-	3.5	-	-	-	pF
C _{I/O}	input/output capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] For transceivers, the parameter I_{OZ} includes the input leakage current.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	An to Bn; Bn to An; see Fig. 3 [2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	2.7	6.0	1.0	6.9	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.1	3.5	1.0	4.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.0	3.6	1.0	4.1	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.3	3.4	1.0	3.9	ns
t_{en}	enable time	$\overline{OE}$ to An; $\overline{OE}$ to Bn; see Fig. 4 [2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	4.0	8.6	1.0	9.9	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.0	6.0	1.0	6.9	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.6	6.3	1.0	7.2	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.9	5.5	1.0	6.3	ns
t_{dis}	disable time	$\overline{OE}$ to An; $\overline{OE}$ to Bn; see Fig. 4 [2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	4.4	8.0	1.0	9.2	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.3	4.8	1.0	5.5	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.3	5.3	1.0	6.1	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	3.2	5.5	1.0	6.3	ns
C_{PD}	power dissipation capacitance	per buffer; $V_I = \text{GND to } V_{CC}$; $V_{CC} = 3.3 \text{ V}$ [3]						
		outputs HIGH or LOW state	-	25	-	-	-	pF
		outputs 3-state	-	1	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25 \text{ °C}$ and $V_{CC} = 1.8 \text{ V}, 2.5 \text{ V}, 2.7 \text{ V}$ and 3.3 V .

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit

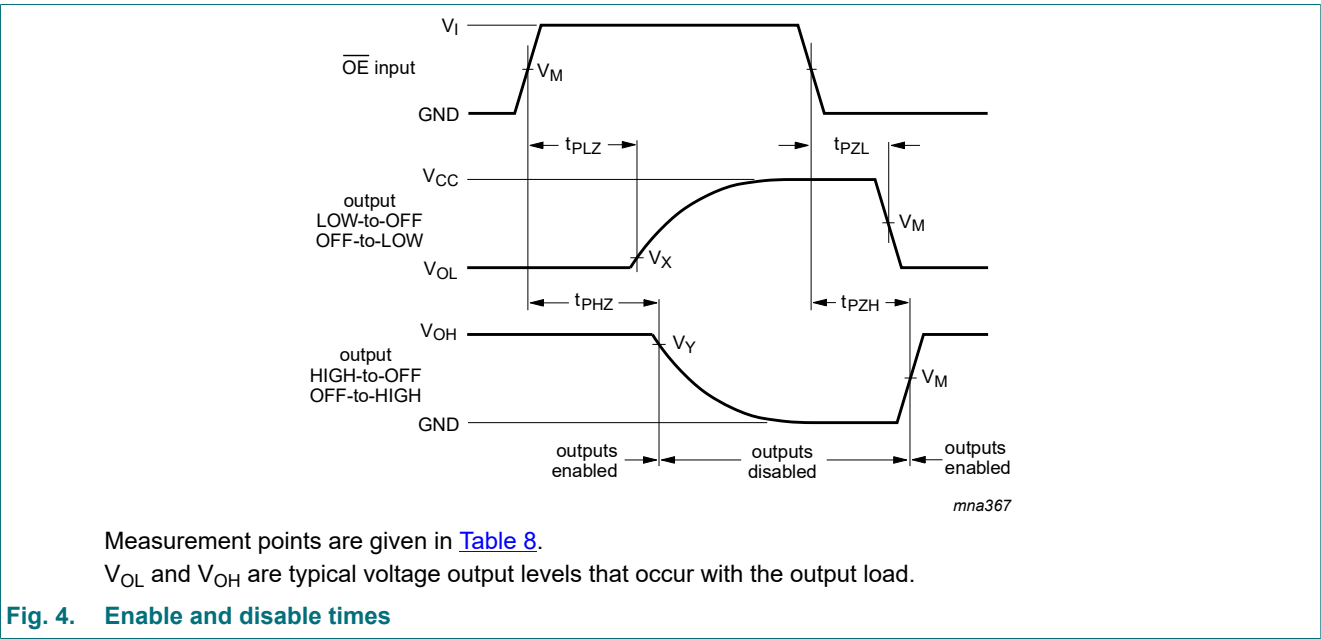
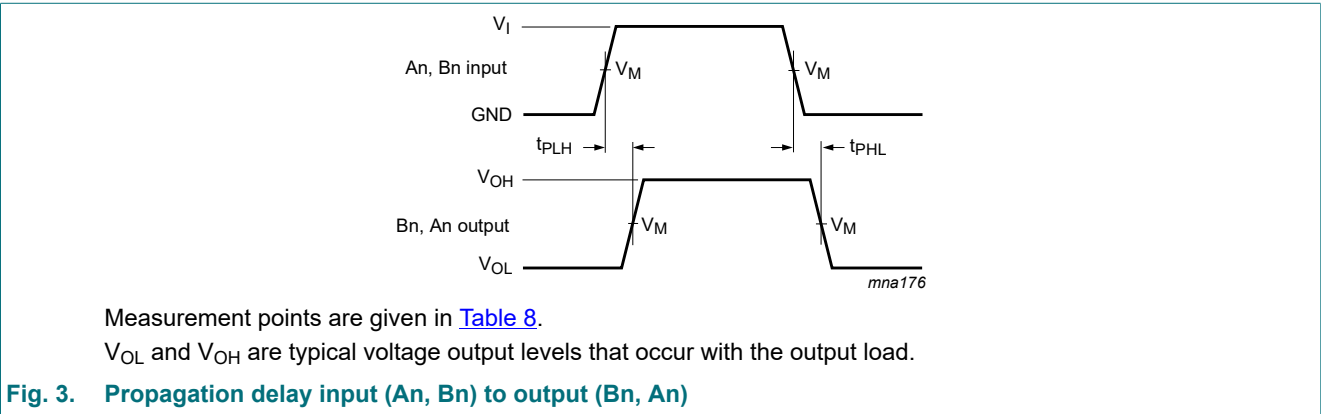
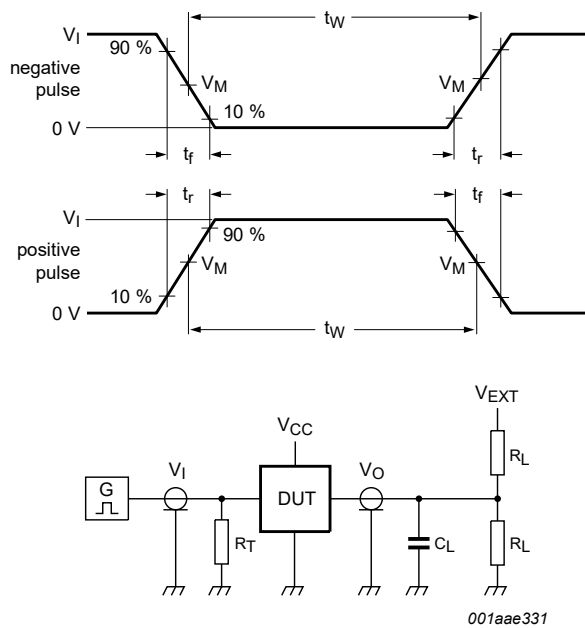


Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;
 C_L = Load capacitance including jig and probe capacitance;
 R_L = Load resistor.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 6. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig. 7. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

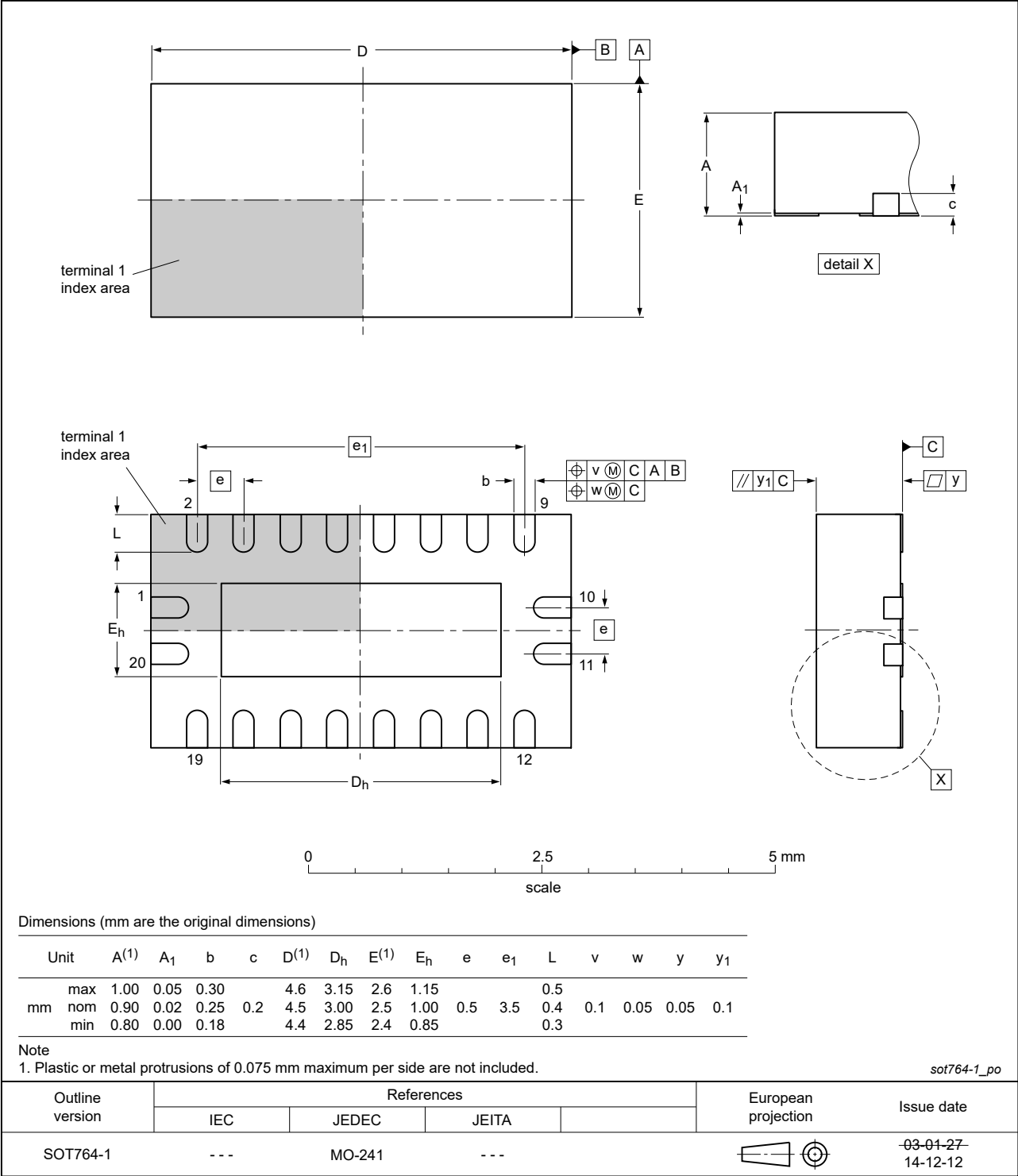


Fig. 8. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC245 v.4	20230710	Product data sheet	-	74ALVC245 v.3
Modifications:	- Specifications for -40 °C to +125 °C added. Section 1 updated. Section 2: ESD specification updated according to the latest JEDEC standard. Table 6: errata.			
74ALVC245 v.3	20210430	Product data sheet	-	74ALVC245 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. Section 2: Reference to JESD36 removed. Section 7: Derating values for P_{tot} total power dissipation removed (errata). - Package outline drawing SOT764-1 (DHVQFN20) updated.			
74ALVC245 v.2	20080107	Product data sheet		74ALVC245 v.1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Section 3: DHVQFN20 package added. Section 7: derating values added for DHVQFN20 package. Section 11: outline drawing added for DHVQFN20 package.			
74ALVC245 v.1	20030710	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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