

HEF4014B-Q100

8-bit static shift register

Rev. 4 — 8 August 2024

Product data sheet

1. General description

The HEF4014B-Q100 is an 8-bit shift register with synchronous parallel enable. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 - Specified from -40 °C to +85 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Applications

- Parallel-to-serial converter
- Serial data queueing
- General-purpose register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4014BT-Q100	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

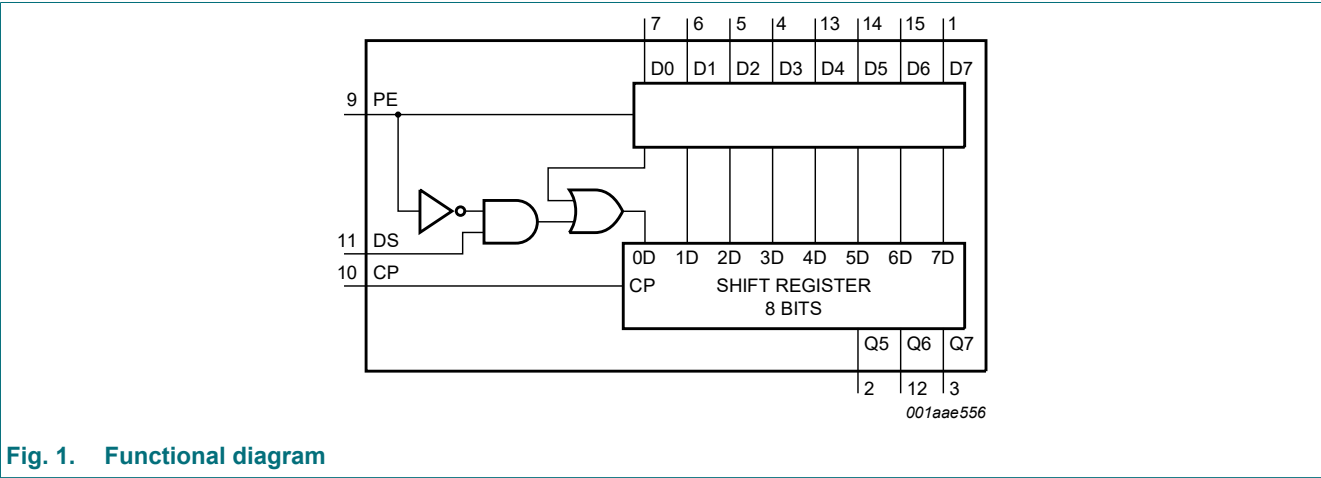


Fig. 1. Functional diagram

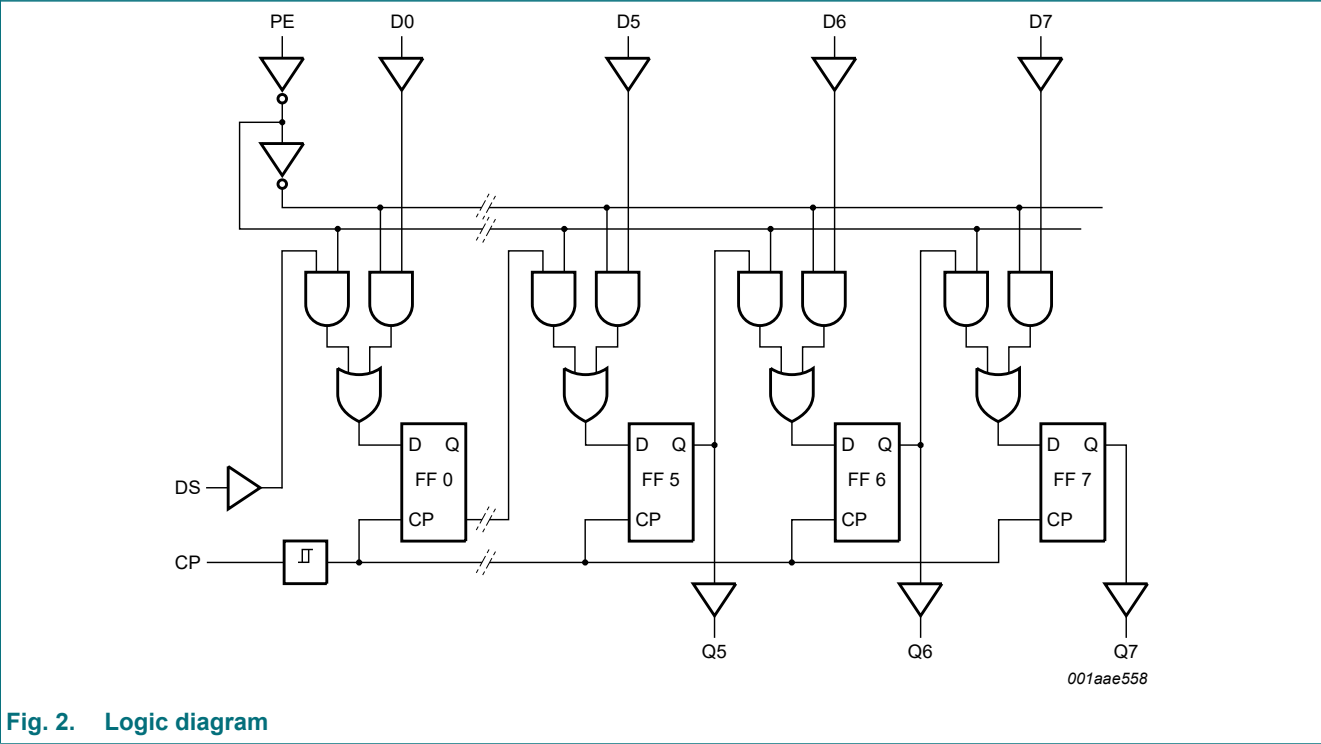
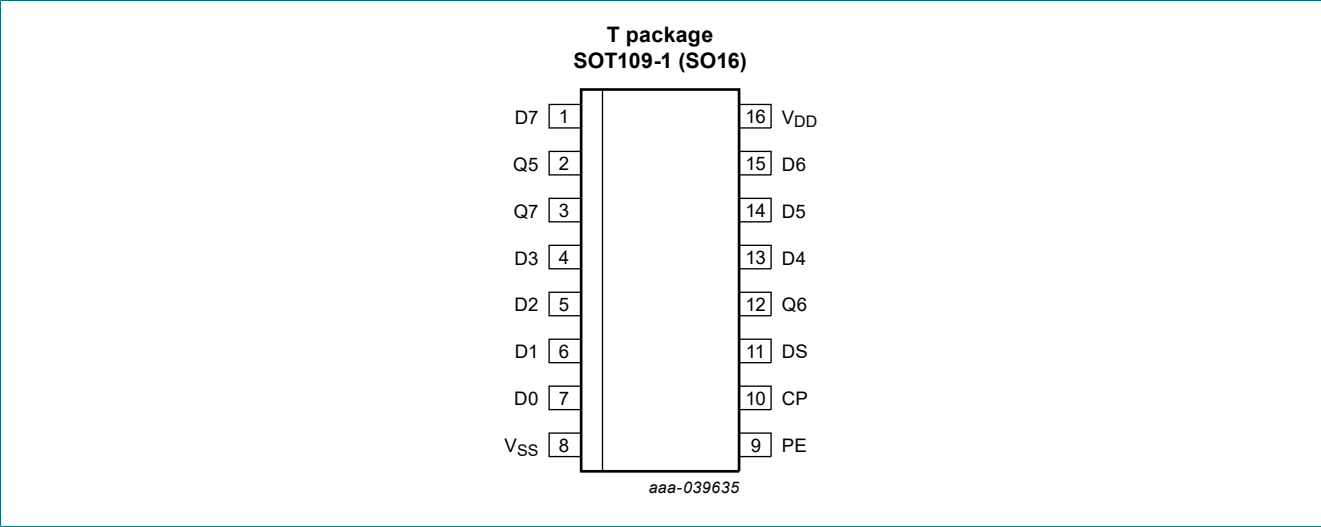


Fig. 2. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q5 to Q7	2, 12, 3	output
D0 to D7	7, 6, 5, 4, 13, 14, 15, 1	parallel data input
V _{SS}	8	ground supply voltage
PE	9	parallel enable input
CP	10	clock input (LOW-to-HIGH edge-triggered)
DS	11	serial data input
V _{DD}	16	supply voltage

7. Functional description

Table 3. Function table
H = HIGH voltage level; L = LOW voltage level; X = don't care; nD = HIGH or LOW;
↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Number of clock transitions	Inputs			Outputs		
	CP	DS	PE	Q5	Q6	Q7
Serial operation						
1	↑	1D	L	X	X	X
2	↑	2D	L	X	X	X
3	↑	3D	L	X	X	X
6	↑	X	L	1D	X	X
7	↑	X	L	2D	1D	X
8	↑	X	L	3D	2D	1D
	↓	X	X	no change	no change	no change
Parallel operation						
1	↑	X	H	D5	D6	D7
	↓	X	X	no change	no change	no change

8. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	supply voltage		3	-	15	V
V _I	input voltage		0	-	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		T _{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I _O < 1 µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I _{DD}	supply current	I _O = 0 A	5 V	-	20	-	20	-	150	µA
			10 V	-	40	-	40	-	300	µA
			15 V	-	80	-	80	-	600	µA
C _I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 25 °C; V_{SS} = 0 V.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	CP to Qn; see Fig. 3	5 V	103 ns + (0.55 ns/pF)C _L	-	130	260	ns
			10 V	44 ns + (0.23 ns/pF)C _L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
t _{PLH}	LOW to HIGH propagation delay	CP to Qn; see Fig. 3	5 V	88 ns + (0.55 ns/pF)C _L	-	115	230	ns
			10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
t _t	transition time	Qn output; see Fig. 3	5 V [2]	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _W	pulse width	CP input; minimum width; see Fig. 4	5 V		70	35	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
t _{su}	set-up time	PE to CP; see Fig. 4	5 V		40	10	-	ns
			10 V		25	5	-	ns
			15 V		15	0	-	ns
		DS to CP; see Fig. 4	5 V		+35	-5	-	ns
			10 V		+25	-5	-	ns
			15 V		25	0	-	ns
		Dn to CP; see Fig. 4	5 V		+35	-5	-	ns
			10 V		+25	-5	-	ns
			15 V		25	0	-	ns
t _h	hold time	PE to CP; see Fig. 4	5 V		+25	-5	-	ns
			10 V		20	0	-	ns
			15 V		15	0	-	ns
		DS to CP; see Fig. 4	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		15	7	-	ns
		Dn to CP; see Fig. 4	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		15	7	-	ns
f _{clk(max)}	maximum clock frequency	see Fig. 4	5 V		6	13	-	MHz
			10 V		15	30	-	MHz
			15 V		20	40	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
[2] t_t is the same as t_{THL} and t_{TLH}.

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	Where:
P_D	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\sum(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 4300 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 12000 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	

11.1. Waveforms and test circuit

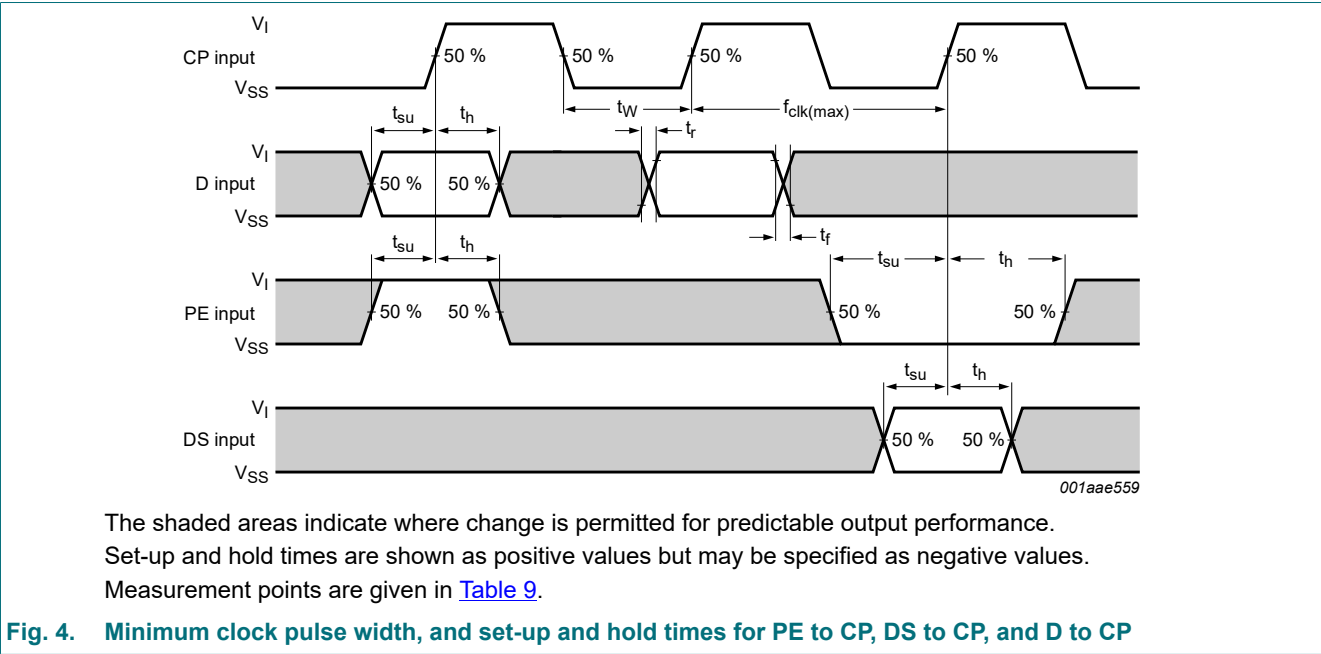
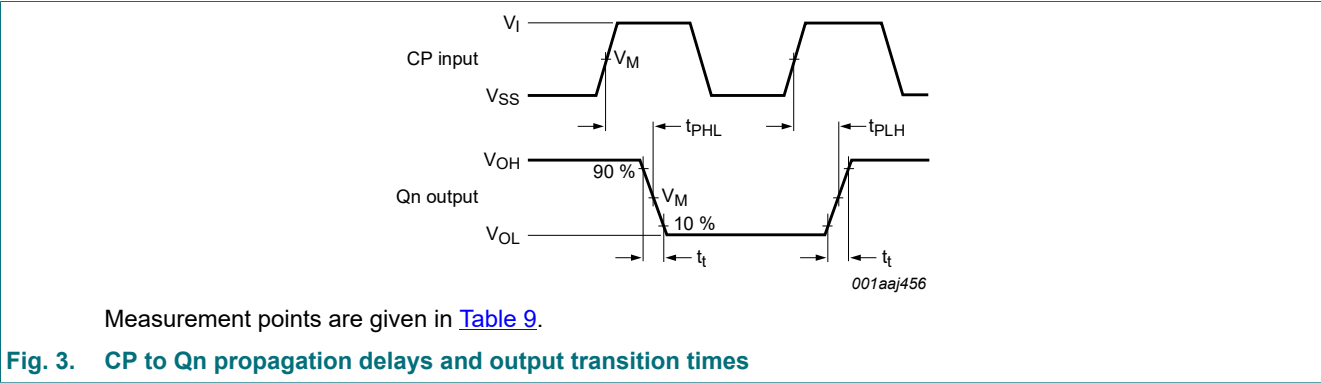
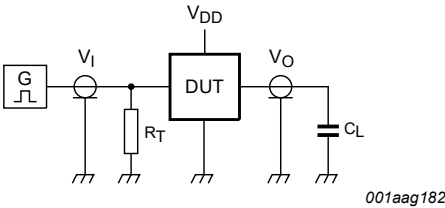


Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).
Definitions test circuit:
 C_L = load capacitance including jig and probe capacitance;
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

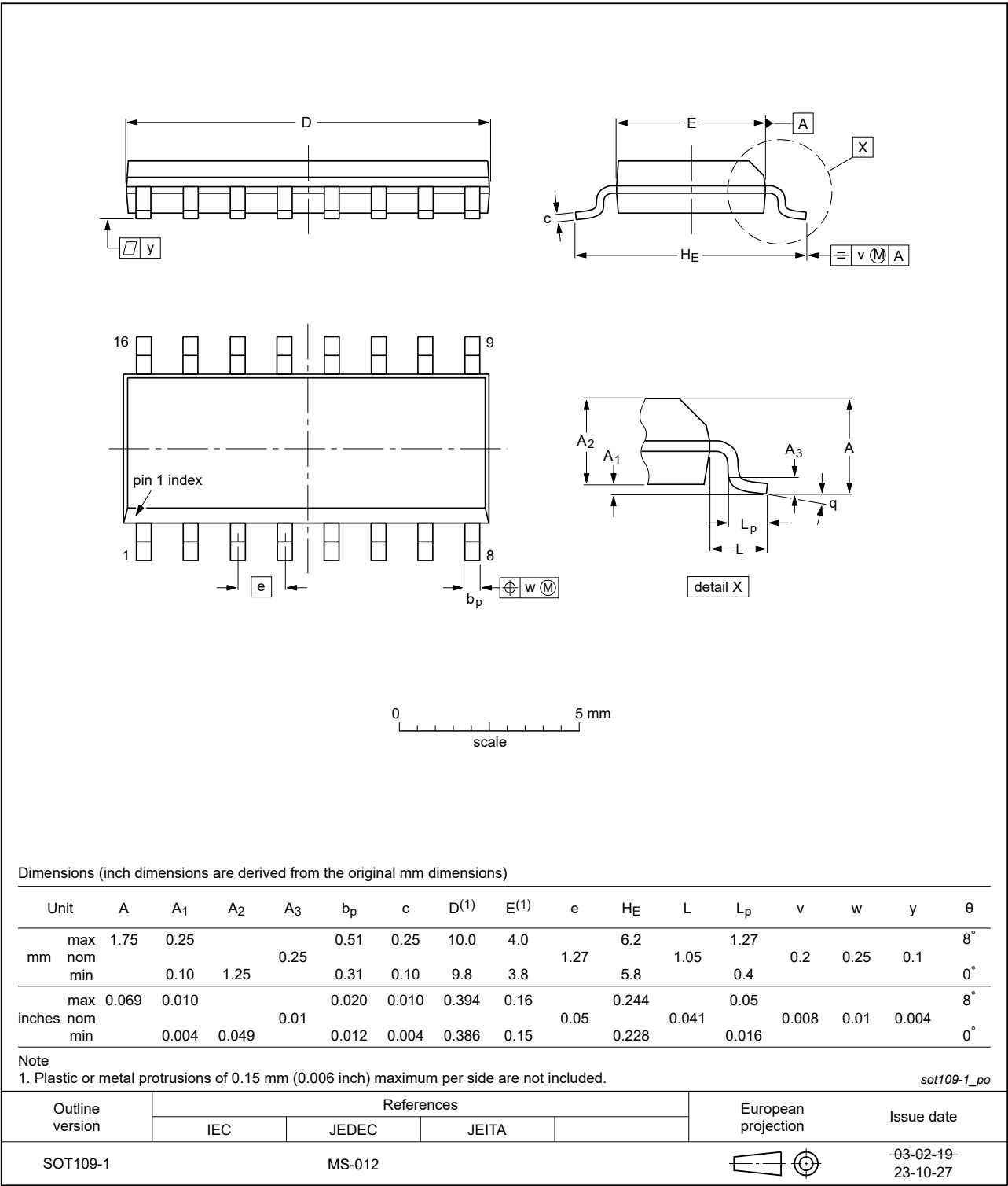


Fig. 6. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4014B_Q100 v.4	20240808	Product data sheet	-	HEF4014B_Q100 v.3
Modifications:	<ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard.Fig. 6: Aligned SO package outline drawing to JEDEC MS-012			
HEF4014B_Q100 v.3	20211124	Product data sheet	-	HEF4014B_Q100 v.2
Modifications:	<ul style="list-style-type: none">Section 1 and Section 2 updated.			
HEF4014B_Q100 v.2	20181017	Product data sheet	-	HEF4014B_Q100 v.1
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.			
HEF4014B_Q100 v.1	20130227	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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