



PNX6R2-25QL

25 V, N-channel Trench MOSFET

31 July 2023

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- Ultra low Q_G and Q_{GD} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery
- Low spiking and ringing for low EMI designs
- MLPAK33 package (3.3 x 3.3 mm footprint)

3. Applications

- DC to DC conversion
- Battery management
- Low-side load switch
- Switching circuits

4. Quick reference data

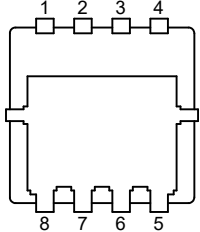
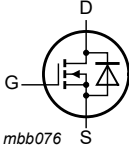
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	25	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	22.3	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 13.1\text{ A}; T_j = 25\text{ °C}$	-	5.3	6.2	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 11.2\text{ A}; T_j = 25\text{ °C}$	-	6.8	8.5	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 12.5\text{ V}; I_D = 11.2\text{ A}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ °C}$	-	8.1	12.2	nC

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>MLPAK33 (SOT8002-1)</p>	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN6R2-25QL	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN6R2-25QL	9AG

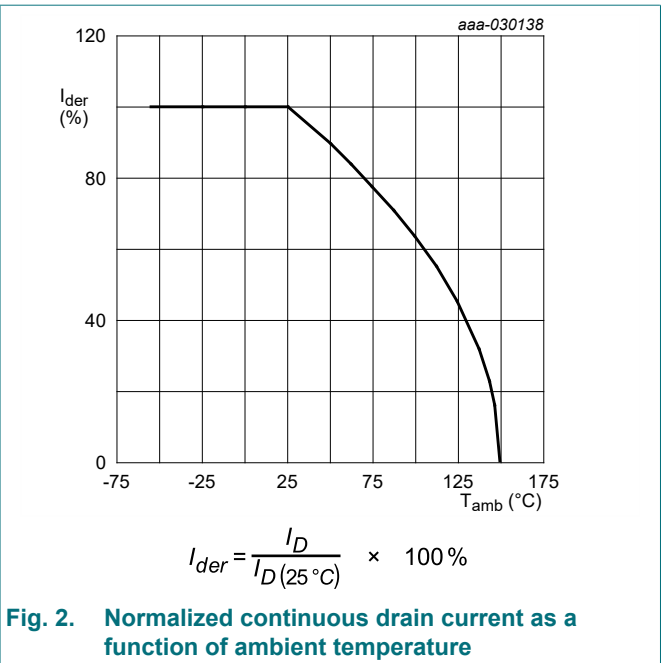
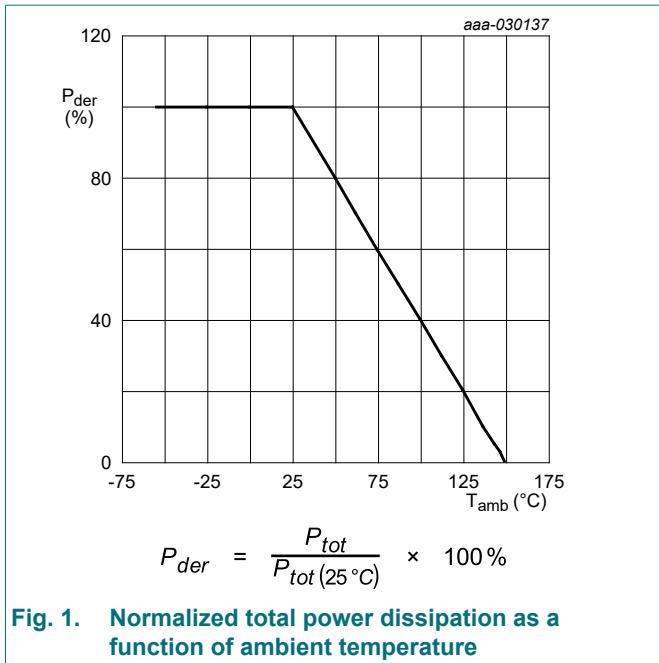
8. Limiting values

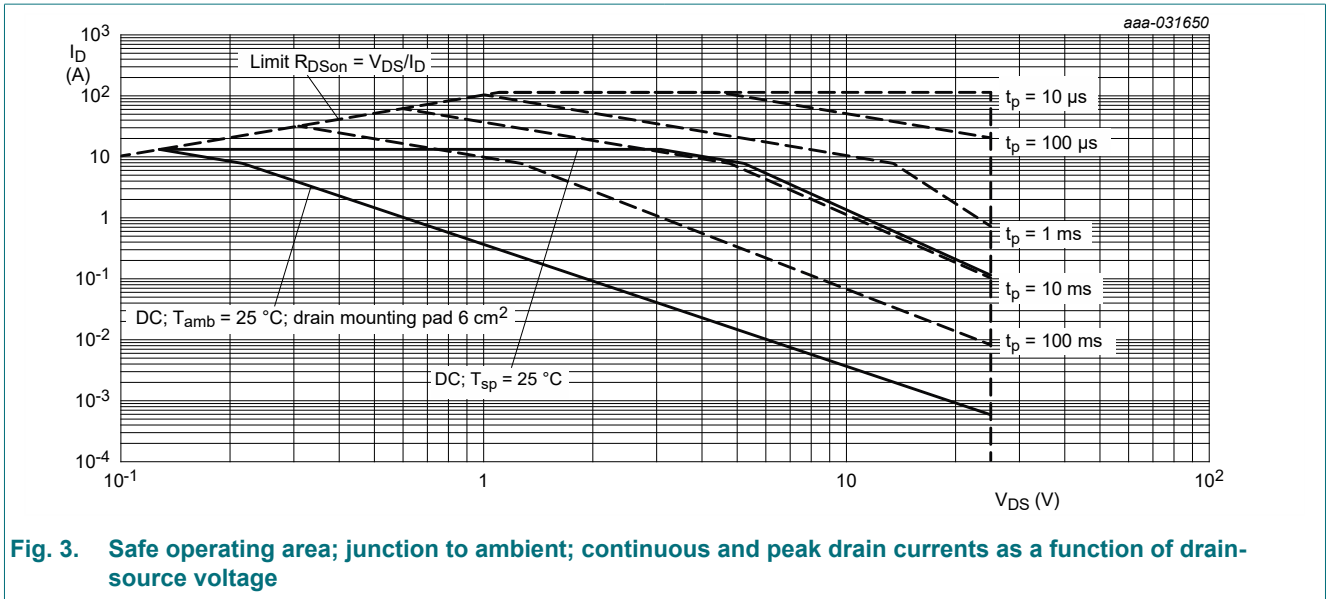
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	25	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	22.3	A
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	13.1	A
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	8.3	A
		V _{GS} = 10 V; T _{sp} = 25 °C		-	65	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	90	A
P _{tot}	total power dissipation	T _{amb} = 25 °C; t ≤ 5 s	[1]	-	4.8	W
		T _{amb} = 25 °C	[1]	-	1.7	W
		T _{sp} = 25 °C		-	40.3	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.5	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(initial)} = 25 °C; I _D = 2.4 A; DUT in avalanche (unclamped)		-	30	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	150	190	K/W
			[2]	-	60	75	K/W
		in free air; $t \leq 5$ s	[2]	-	21	26	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	2.1	3.1	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

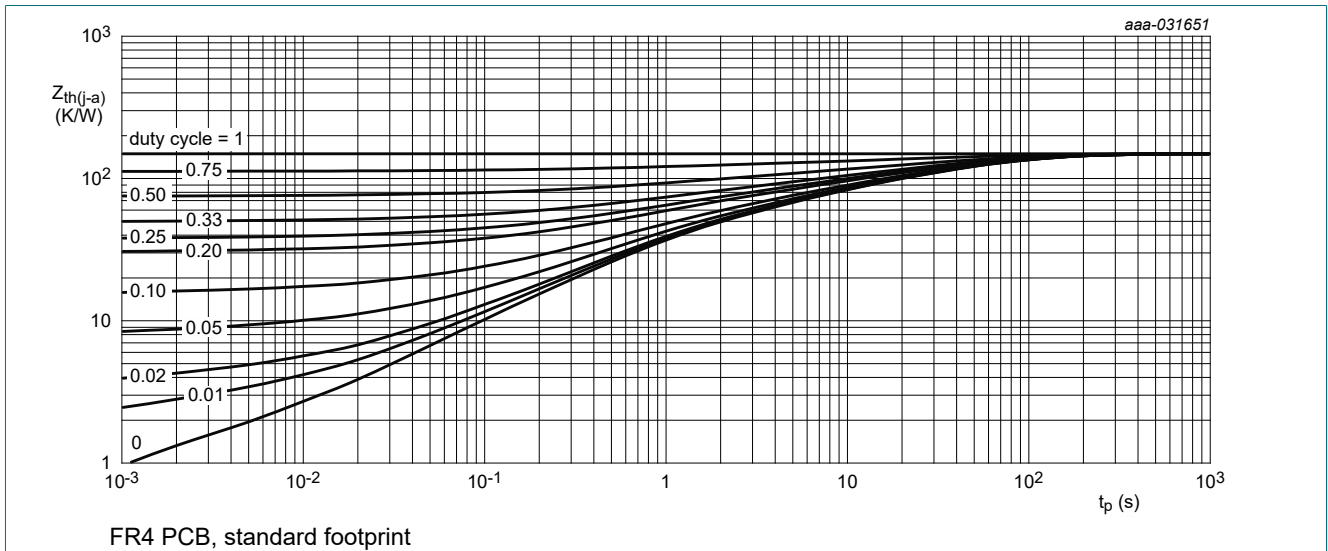


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

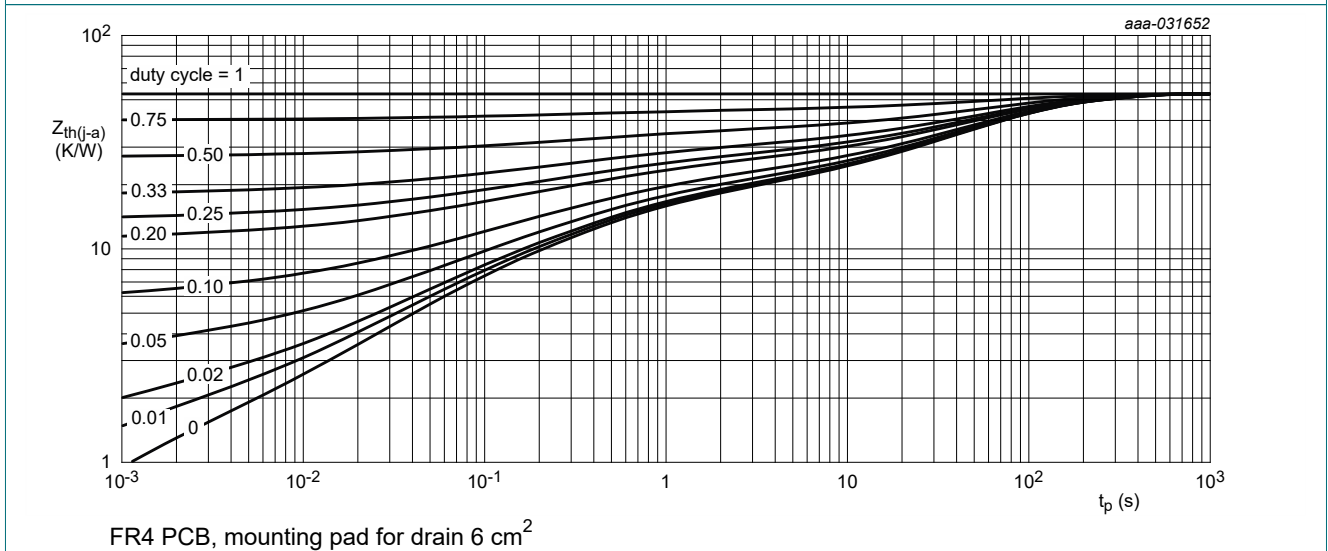


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	25	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$	1.2	1.7	2.2	V
I_{DSS}	drain leakage current	$V_{DS} = 25 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 13.1 A$; $T_j = 25 \text{ }^\circ C$	-	5.3	6.2	m Ω
		$V_{GS} = 10 V$; $I_D = 13.1 A$; $T_j = 150 \text{ }^\circ C$	-	8.2	9.7	m Ω
		$V_{GS} = 4.5 V$; $I_D = 11.2 A$; $T_j = 25 \text{ }^\circ C$	-	6.8	8.5	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V$; $I_D = 13.1 A$; $T_j = 25 \text{ }^\circ C$	-	32	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$	-	11.5	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 12.5 V$; $I_D = 13.1 A$; $V_{GS} = 10 V$; $T_j = 25 \text{ }^\circ C$	-	17	25.5	nC
		$V_{DS} = 12.5 V$; $I_D = 11.2 A$; $V_{GS} = 4.5 V$; $T_j = 25 \text{ }^\circ C$	-	8.1	12.2	nC
Q_{GS}	gate-source charge	$T_j = 25 \text{ }^\circ C$	-	3.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.2	-	nC
Q_{GD}	gate-drain charge		-	2.2	-	nC
V_{GSpl}	gate-source plateau voltage	$V_{DS} = 12.5 V$; $I_D = 11.2 A$; $T_j = 25 \text{ }^\circ C$	-	2.8	-	V
C_{iss}	input capacitance	$V_{DS} = 12.5 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	1200	-	pF
C_{oss}	output capacitance		-	430	-	pF
C_{rss}	reverse transfer capacitance		-	76	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12.5 V$; $I_D = 11.2 A$; $V_{GS} = 4.5 V$; $R_{G(ext)} = 5 \Omega$; $T_j = 25 \text{ }^\circ C$	-	5	-	ns
t_r	rise time		-	8	-	ns
$t_{d(off)}$	turn-off delay time		-	6	-	ns
t_f	fall time		-	3	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.5 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	0.7	1.2	V
t_{rr}	reverse recovery time	$I_S = 1.5 A$; $di_S/dt = -100 A/\mu s$; $V_{GS} = 4.5 V$; $V_{DS} = 12.5 V$; $T_j = 25 \text{ }^\circ C$	-	15	-	ns
Q_r	recovered charge		-	6	-	nC
t_a	reverse recovery rise time		-	8	-	ns
t_b	reverse recovery fall time		-	7	-	ns

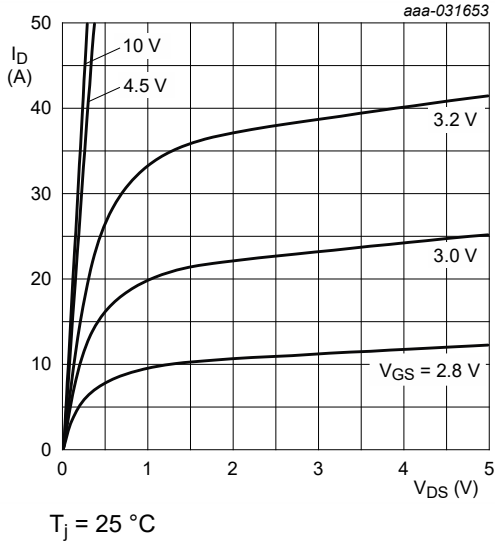


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

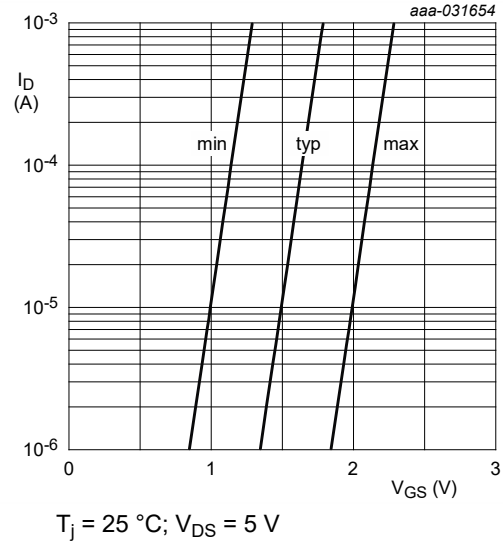


Fig. 7. Subthreshold drain current as a function of gate-source voltage

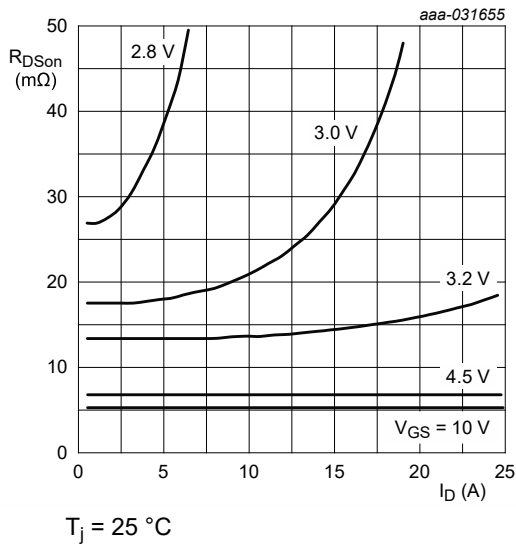


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

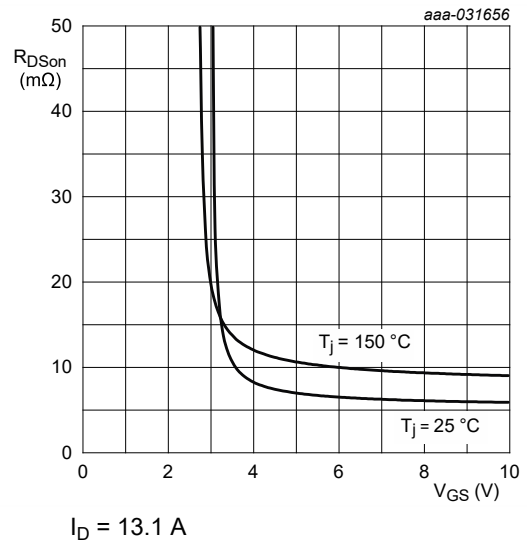


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

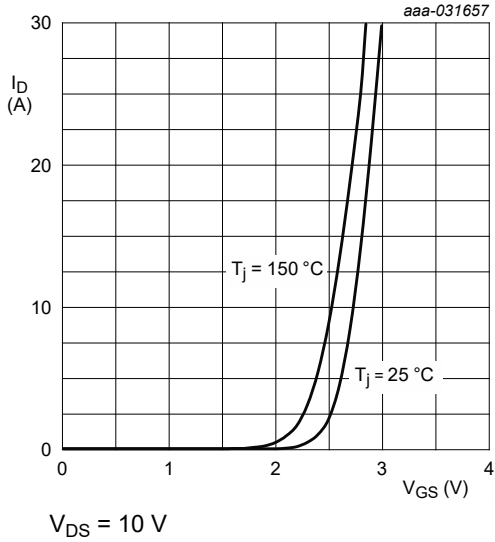
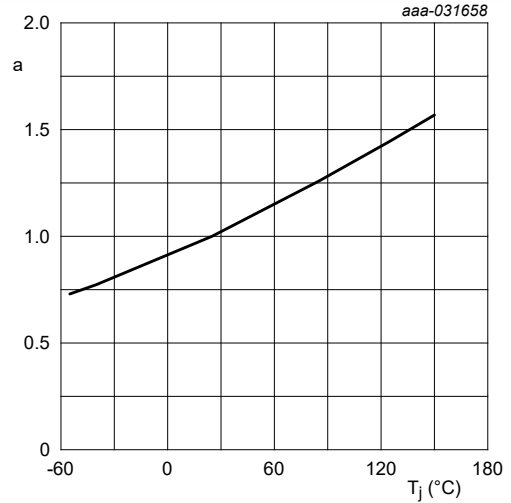


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

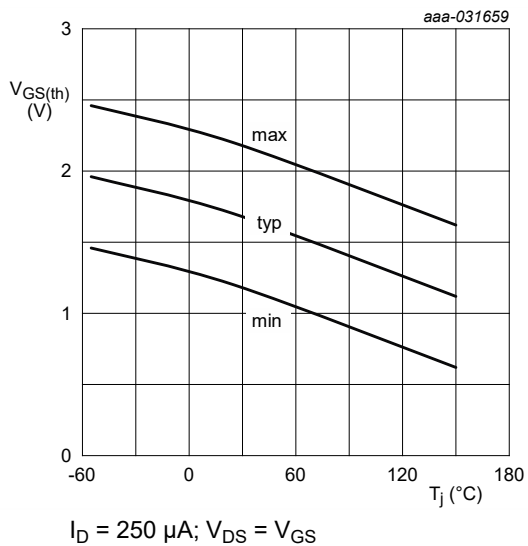


Fig. 12. Gate-source threshold voltage as a function of junction temperature

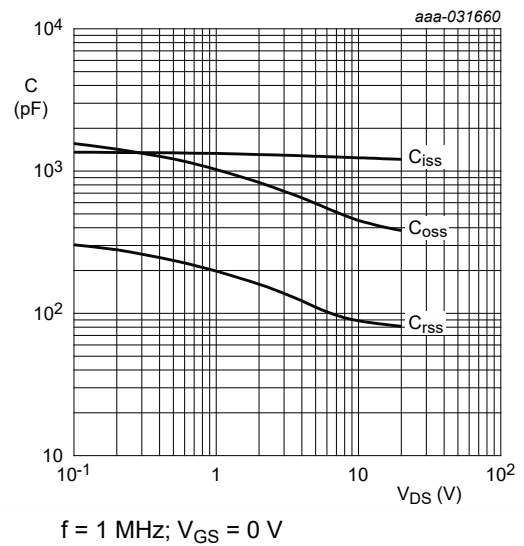


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

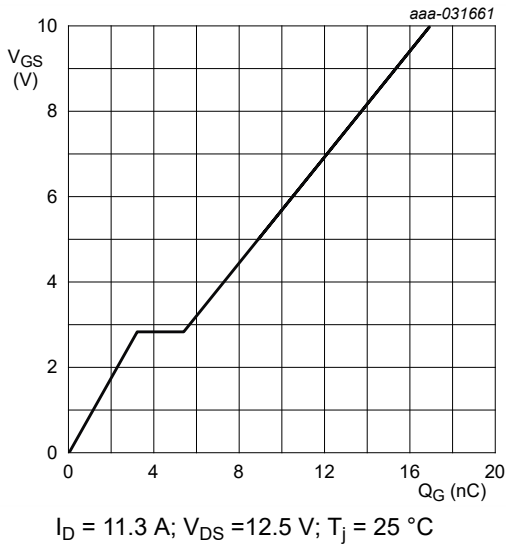


Fig. 14. Gate-source voltage as a function of gate charge; typical values

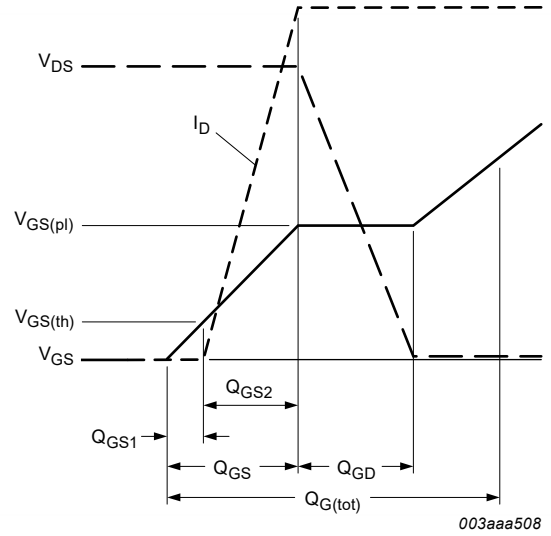


Fig. 15. Gate charge waveform definitions

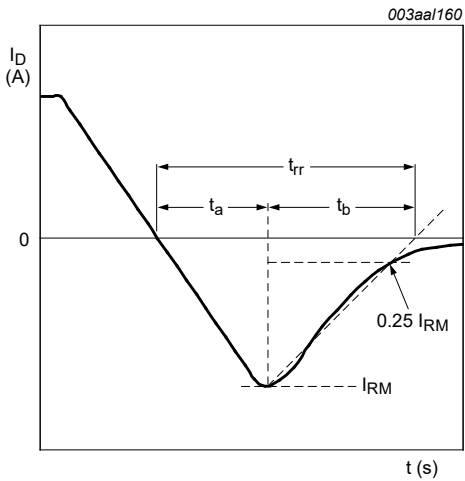


Fig. 16. Reverse recovery timing definition

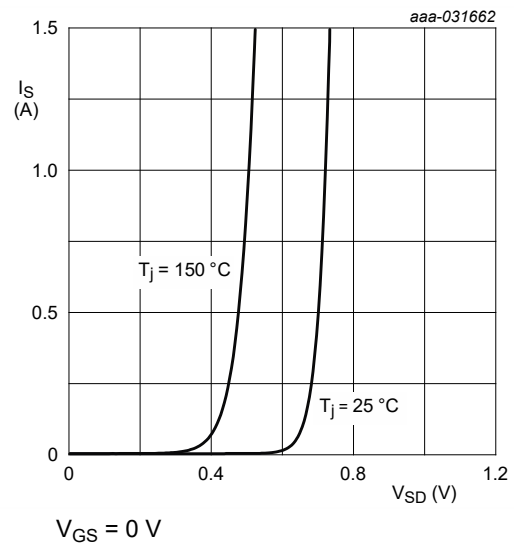


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

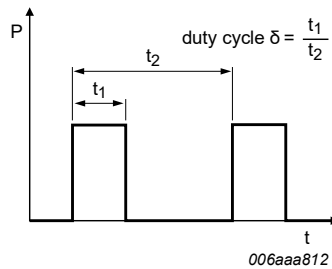
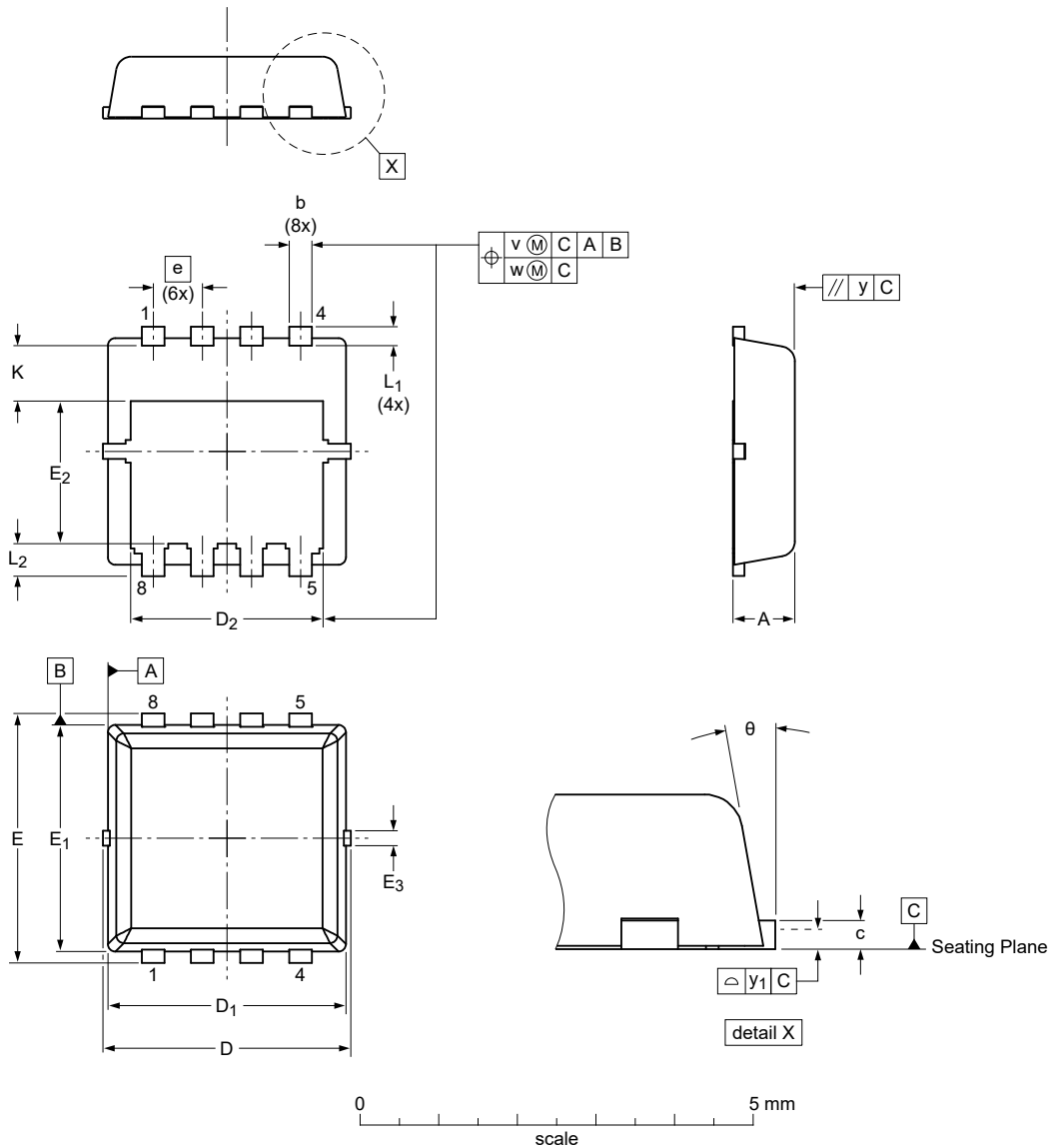


Fig. 18. Duty cycle definition

12. Package outline

MLPAK33: plastic thermal enhanced surface mounted package; mini leads; 8 terminals;
pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body

SOT8002-1



Dimensions (mm are the original dimensions)

Unit	A	b	c	D	D ₁	D ₂	e	E	E ₁	E ₂	E ₃	K	L ₁	L ₂	θ	y	y ₁	v	w
max	0.90	0.35	0.18	3.50	3.25	2.65		3.50	3.10	1.99	0.25		0.40	0.58	12°				
mm nom	0.80	0.30	0.15	3.30	3.15	2.55	0.65	3.30	3.00	1.89	0.20	0.65 (ref)	0.25	0.43	10°	0.05	0.05	0.1	0.05
min	0.70	0.25	0.12	3.10	3.05	2.45		3.10	2.90	1.79	0.15		0.10	0.28	8°				

sot8002-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT8002-1						20-01-19 23-05-17

Fig. 19. Package outline MLPAK33 (SOT8002-1)

13. Soldering

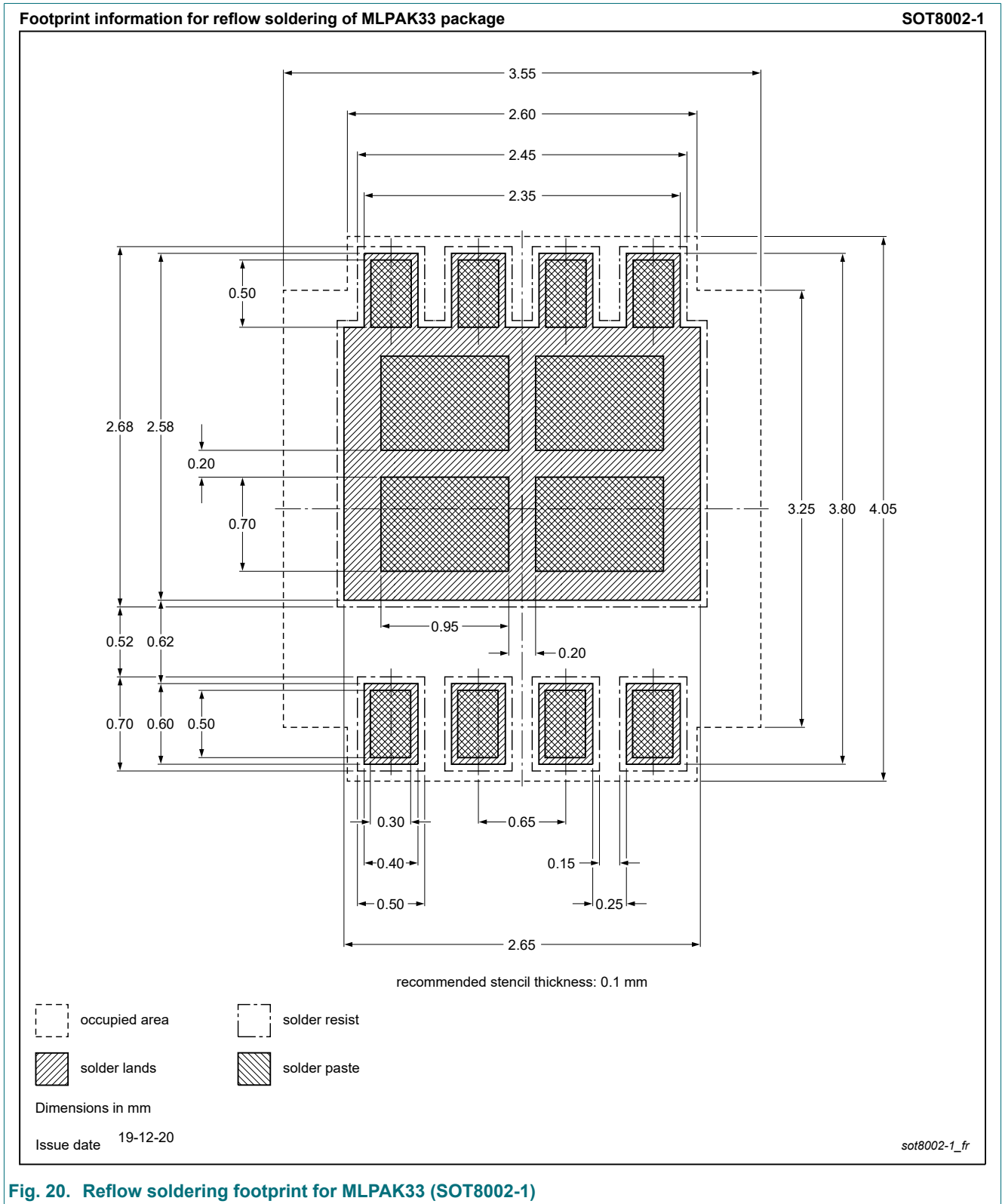


Fig. 20. Reflow soldering footprint for MLPAK33 (SOT8002-1)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PXN6R2-25QL v.2	20230731	Product data sheet	-	PXN6R2-25QL v.1
Modifications:	• Chapter "Package outline": drawing update			
PXN6R2-25QL v.1	20201102	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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