

# 74LVC244A; 74LVCH244A

Octal buffer/line driver; 3-state

Rev. 14 — 29 November 2024

Product data sheet

## 1. General description

The 74LVC244A; 74LVCH244A are 8-bit buffer/line drivers with 3-state outputs. The devices can be used as two 4-bit buffers or one 8-bit buffer. Both devices features two output enables ( $1\overline{OE}$  and  $2\overline{OE}$ ), each controlling four of the 3-state outputs. A HIGH on  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Bus hold on all data inputs (74LVCH244A only)
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74LVC244AD</a> <a href="#">74LVCH244AD</a>	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	<a href="#">SOT163-1</a>
<a href="#">74LVC244APW</a> <a href="#">74LVCH244APW</a>	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	<a href="#">SOT360-1</a>
<a href="#">74LVC244ABQ</a> <a href="#">74LVCH244ABQ</a>	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	<a href="#">SOT764-1</a>
<a href="#">74LVC244ABZ</a>	-40 °C to +125 °C	DHXQFN20	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 20 terminals; 0.4 mm pitch; body 2 mm × 3.2 mm × 0.48 mm	<a href="#">SOT8020-1</a>

4. Functional diagram

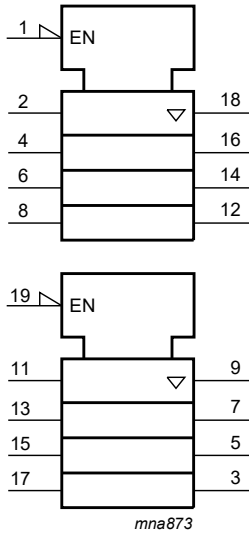


Fig. 1. IEC logic diagram

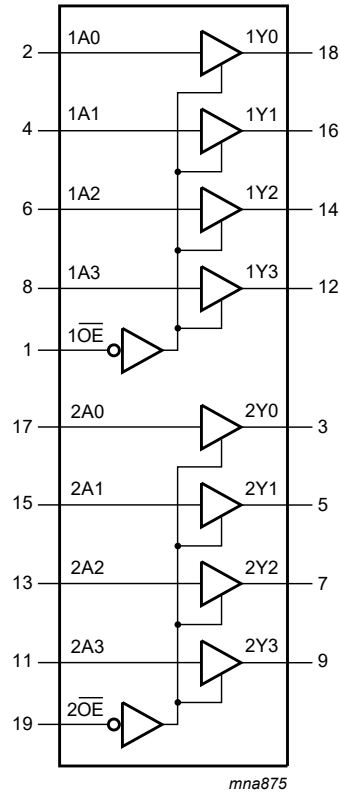


Fig. 2. Functional diagram

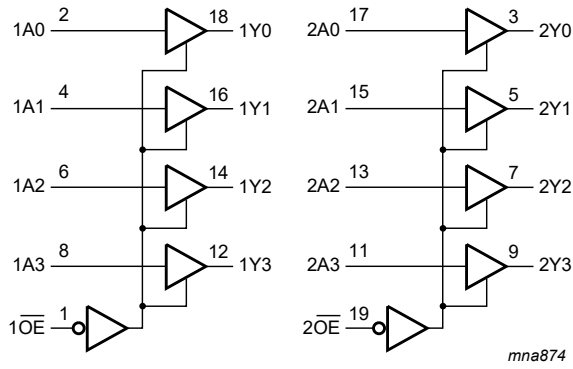
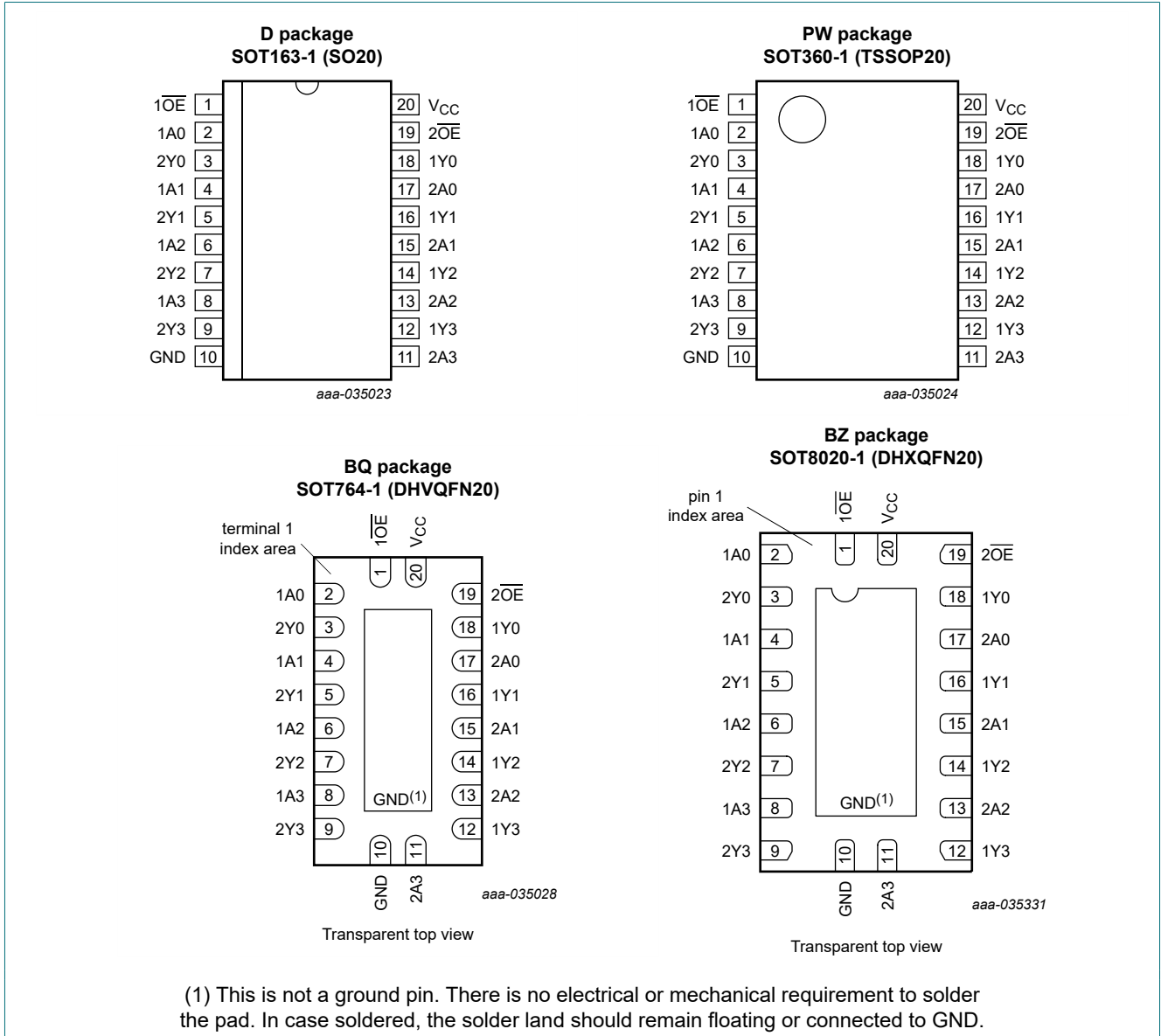


Fig. 3. Logic symbol

## 5. Pinning information

### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3,	18, 16, 14, 12	data output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA	
V <sub>I</sub>	input voltage		[1] -0.5	+6.5	V	
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA	
V <sub>O</sub>	output voltage	output HIGH or LOW	[2] -0.5	V <sub>CC</sub> + 0.5	V	
		output 3-state	[2] -0.5	+6.5	V	
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA	
I <sub>CC</sub>	supply current		-	100	mA	
I <sub>GND</sub>	ground current		-100	-	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C				
		SOT163-1 (SO20) SOT360-1 (TSSOP20) SOT764-1 (DHVQFN20)	[3]	-	500	mW
		SOT8020-1		-	250	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT163-1 (SO20) package: P<sub>tot</sub> derates linearly with 12.3 mW/K above 109 °C.

For SOT360-1 (TSSOP20) package: P<sub>tot</sub> derates linearly with 10.0 mW/K above 100 °C.

For SOT764-1 (DHVQFN20) package: P<sub>tot</sub> derates linearly with 12.9 mW/K above 111 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.2 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 3.6 \text{ V}$ [2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = 5.5 \text{ V}$ or GND; $V_{CC} = 3.6 \text{ V}$ [2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5 \text{ V}$ ; $V_{CC} = 0.0 \text{ V}$	-	$\pm 0.1$	$\pm 10$	-	$\pm 20$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 3.6 \text{ V}$	-	0.1	10	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$ ; $V_{CC} = 2.7 \text{ V}$ to $3.6 \text{ V}$	-	5	500	-	5000	$\mu\text{A}$
$C_I$	input capacitance		-	4.0	-	-	-	pF
$I_{BHL}$	bus hold LOW current	$V_{CC} = 1.65 \text{ V}$ ; $V_I = 0.58 \text{ V}$ [3][4]	10	-	-	10	-	$\mu\text{A}$
		$V_{CC} = 2.3 \text{ V}$ ; $V_I = 0.7 \text{ V}$	30	-	-	25	-	$\mu\text{A}$
		$V_{CC} = 3.0 \text{ V}$ ; $V_I = 0.8 \text{ V}$	75	-	-	60	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 1.65 \text{ V}$ ; $V_I = 1.07 \text{ V}$ [3][4]	-10	-	-	-10	-	$\mu\text{A}$
		$V_{CC} = 2.3 \text{ V}$ ; $V_I = 1.7 \text{ V}$	-30	-	-	-25	-	$\mu\text{A}$
		$V_{CC} = 3.0 \text{ V}$ ; $V_I = 2.0 \text{ V}$	-75	-	-	-60	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 1.95 \text{ V}$ [3][5]	200	-	-	200	-	$\mu\text{A}$
		$V_{CC} = 2.7 \text{ V}$	300	-	-	300	-	$\mu\text{A}$
		$V_{CC} = 3.6 \text{ V}$	500	-	-	500	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 1.95 \text{ V}$ [3][5]	-200	-	-	-200	-	$\mu\text{A}$
		$V_{CC} = 2.7 \text{ V}$	-300	-	-	-300	-	$\mu\text{A}$
		$V_{CC} = 3.6 \text{ V}$	-500	-	-	-500	-	$\mu\text{A}$

[1] All typical values are measured at  $V_{CC} = 3.3 \text{ V}$  (unless stated otherwise) and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

[2] The bus hold circuit is switched off when  $V_I > V_{CC}$  allowing 5.5 V on the input terminal.

[3] Valid for data inputs of bus hold parts only (74LVCH244A). Note that control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data input holds the input below the specified  $V_I$  level.

[5] The specified overdrive current at the data input forces the data input to the opposite input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{pd}$	propagation delay	nAn to nYn; see Fig. 4 [2]						
		$V_{CC} = 1.2\text{ V}$	-	17.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	6.4	13.7	1.5	15.8	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.4	7.1	1.0	8.2	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.4	6.9	1.5	9.0	ns
$t_{en}$	enable time	nOE to nYn; see Fig. 5 [2]						
		$V_{CC} = 1.2\text{ V}$	-	24.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	7.0	17.3	1.5	20.0	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.5	3.9	9.5	1.5	11.0	ns
		$V_{CC} = 2.7\text{ V}$	1.5	4.1	8.6	1.5	11.0	ns
$t_{dis}$	disable time	nOE to nYn; see Fig. 5 [2]						
		$V_{CC} = 1.2\text{ V}$	-	9.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.2	4.5	9.8	2.2	11.3	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.5	3.6	5.5	0.5	6.4	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.3	6.8	1.5	8.5	ns
$t_{sk(o)}$	output skew time	[3]	-	-	1.0	-	1.5	ns
$C_{PD}$	power dissipation capacitance	per input; $V_I = \text{GND to } V_{CC}$ [4]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	6.4	-	-	-	pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	9.6	-	-	-	pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	12.5	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V},$  and  $3.3\text{ V}$  respectively.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

$t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

$t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

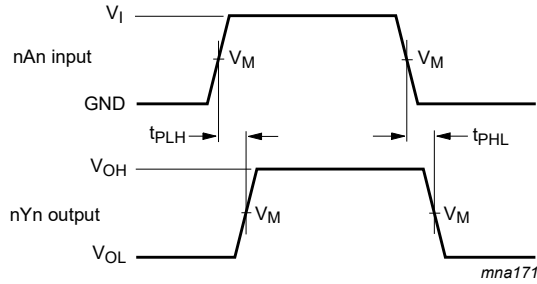
$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in Volts

$N$  = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

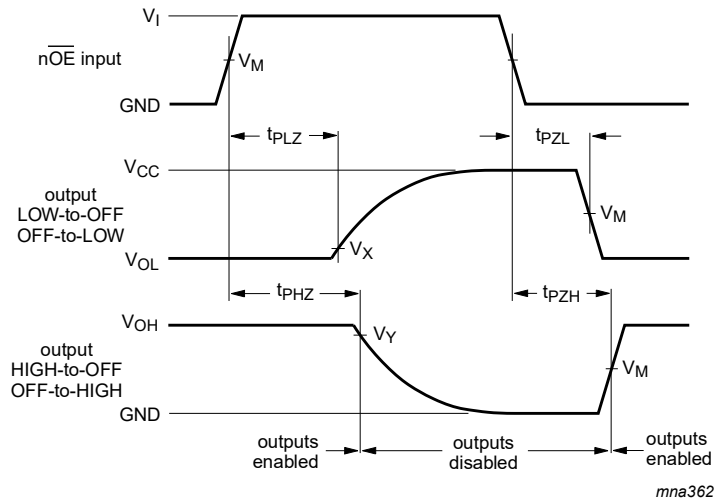
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 4. The input (nAn) to output (nYn) propagation delays



Measurement points are given in [Table 8](#).

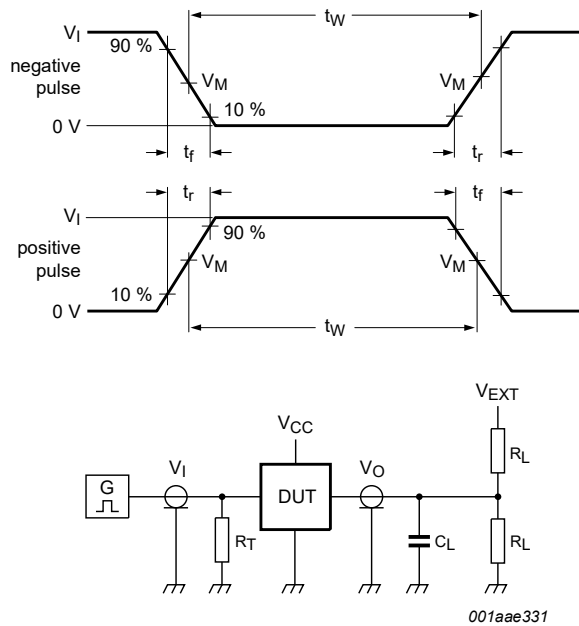
Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 5. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$





Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 6. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

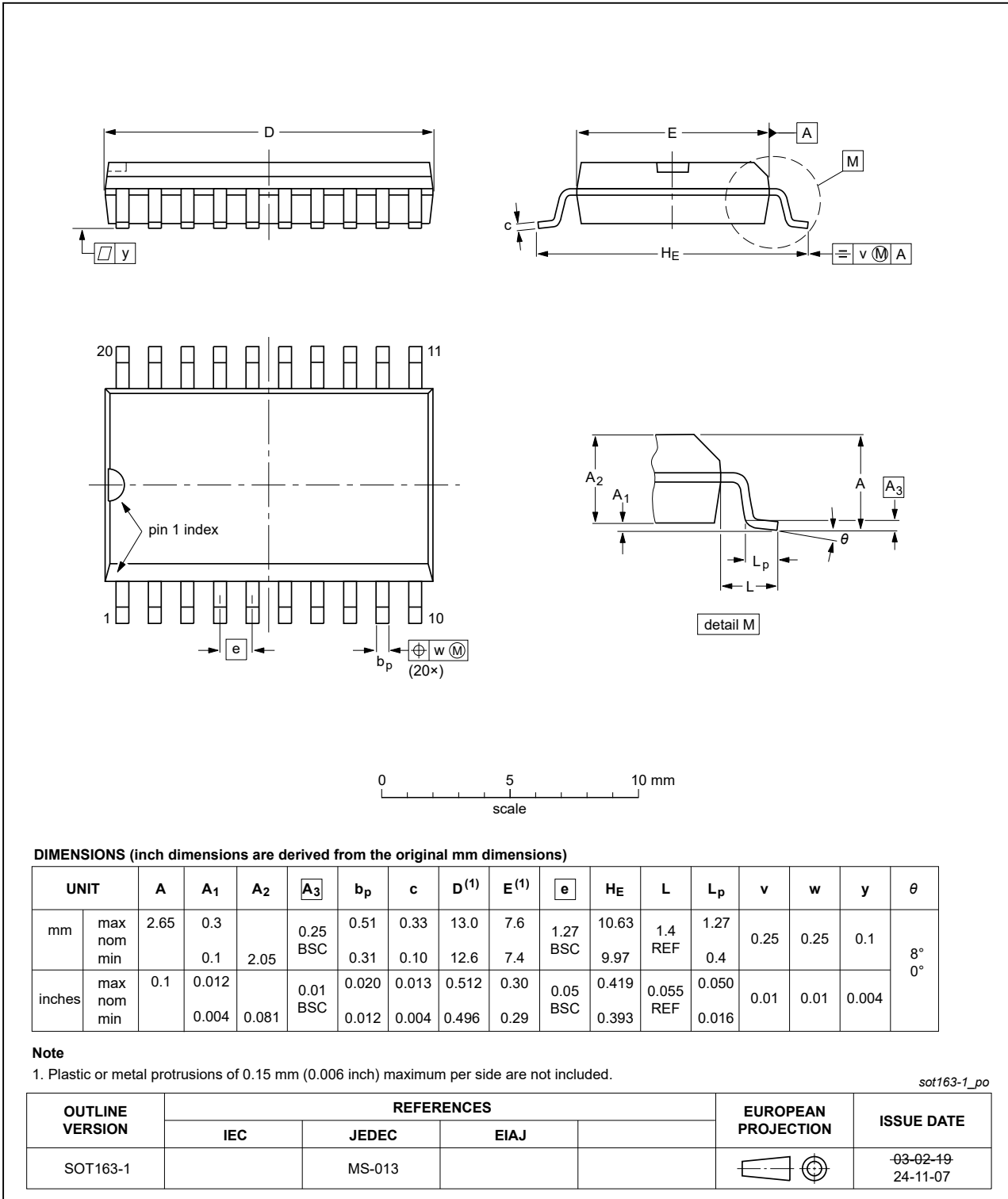


Fig. 7. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

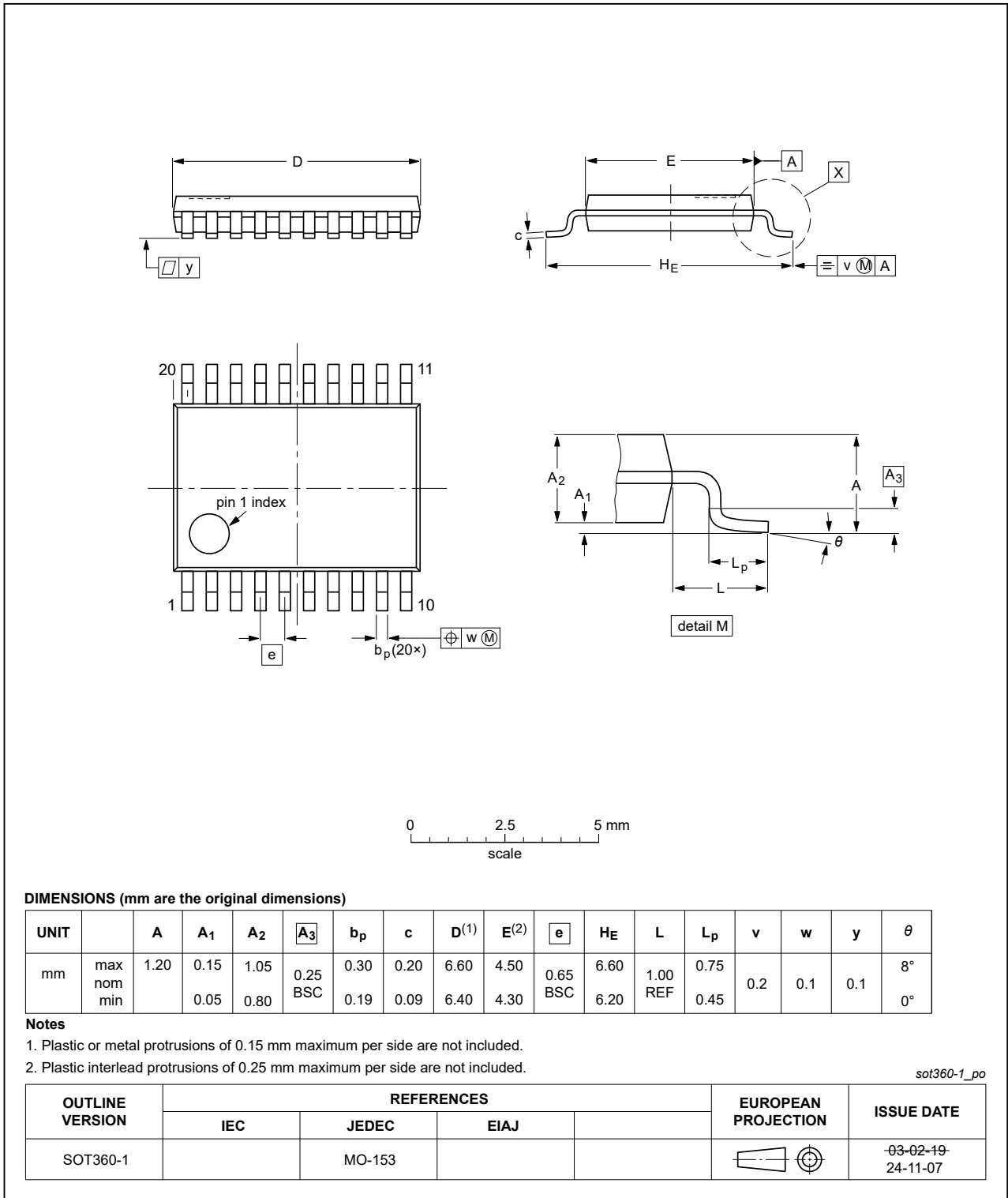


Fig. 8. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig. 9. Package outline SOT764-1 (DHVQFN20)

DHXQFN20: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package;  
no leads; 20 terminals; 0.4 mm pitch; body 2 mm x 3.2 mm x 0.48 mm

SOT8020-1

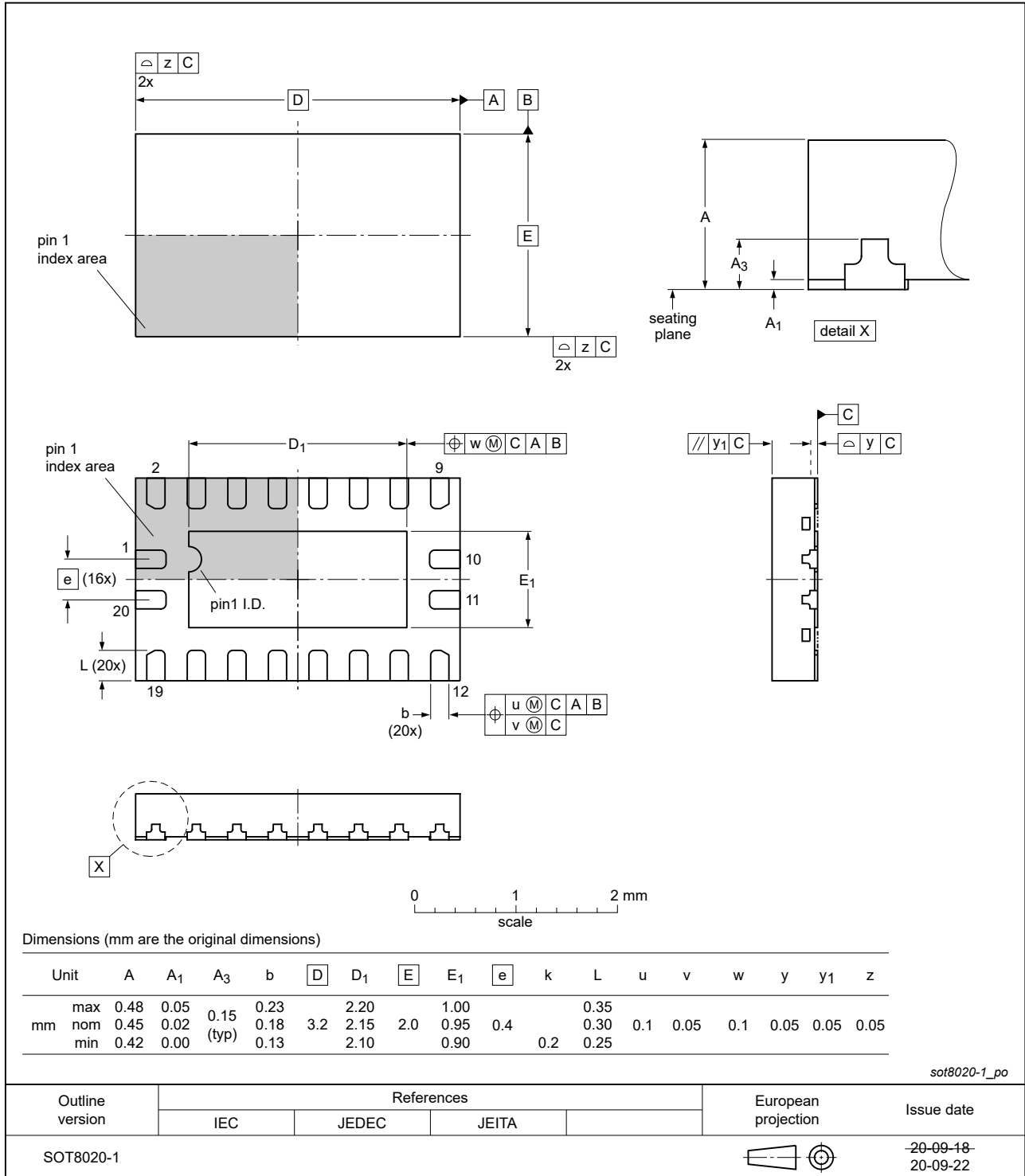


Fig. 10. Package outline SOT8020-1 (DHXQFN20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH244A v.14	20241129	Product data sheet	-	74LVC_LVCH244A v.13
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Fig. 7</a> and <a href="#">Fig. 8</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-013 and MO-153.</li> </ul>			
74LVC_LVCH244A v.13	20230807	Product data sheet	-	74LVC_LVCH244A v.12
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74LVC_LVCH244A v.12	20210916	Product data sheet	-	74LVC_LVCH244A v.11
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVC244ADB (SOT339-1 / SSOP20) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
74LVC_LVCH244A v.11	20210429	Product data sheet	-	74LVC_LVCH244A v.10
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVC244ABZ (SOT8020-1 / DHXQFN20) added.</li> <li>Type number 74LVCH244ADB (SOT339-1 / SSOP20) removed.</li> </ul>			
74LVC_LVCH244A v.10	20200408	Product data sheet	-	74LVC_LVCH244A v.9
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74LVC_LVCH244A v.9	20180813	Product data sheet	-	74LVC_LVCH244A v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74LVC244ABX and 74LVCH244ABX (SOT1045-2) removed.</li> </ul>			
74LVC_LVCH244A v.8	20130626	Product data sheet	-	74LVC_LVCH244A v.7
Modifications:	<ul style="list-style-type: none"> <li>For type numbers 74LVC244ABX and 74LVCH244ABX DHXQFN20U (SOT1045-1) has changed to DHXQFN20 (SOT1045-2).</li> </ul>			
74LVC_LVCH244A v.7	20111122	Product data sheet	-	74LVC_LVCH244A v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC_LVCH244A v.6	20090813	Product data sheet	-	74LVC_LVCH244A v.5
74LVC_LVCH244A v.5	20090709	Product data sheet	-	74LVC_LVCH244A v.4
74LVC_LVCH244A v.4	20031030	Product specification	-	74LVC_LVCH244A v.3
74LVC_LVCH244A v.3	20030520	Product specification	-	74LVC_H244A v.2

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_H244A v.2	19980520	Product specification	-	74LVC244A_74LVCH244A v.1
74LVC244A_74LVCH244A v.1	19960906	Product specification	-	-

## 14. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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