



# PDTA123YM

NPN resistor-equipped transistor; R1 = 2.2 k $\Omega$ , R2 = 10 k $\Omega$

6 December 2024

Product data sheet

## 1. General description

NPN Resistor-Equipped Transistor (RET) in a leadless ultra small SOT883 (SC-101) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA123YM

## 2. Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

## 3. Applications

- General-purpose switching and amplification
- Inverter and interface circuits
- Circuit drivers

## 4. Quick reference data

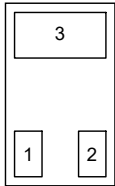
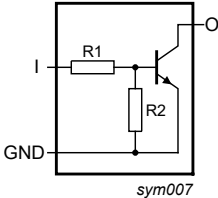
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-	50	V
I <sub>O</sub>	output current			-	-	100	mA
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	k $\Omega$
R2/R1	bias resistor ratio		[1]	3.6	4.5	5.5	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 <p>Transparent top view</p> <p>DFN1006-3 (SOT883)</p>	 <p>sym007</p>
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTC123YM	DFN1006-3	plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PDTC123YM	G7

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	5	V
V <sub>I</sub>	input voltage			-5	12	V
I <sub>O</sub>	output current			-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1] [2]	-	250	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 60 μm copper, tin-plated and standard footprint.  
[2] Reflow soldering is the only recommended soldering method.

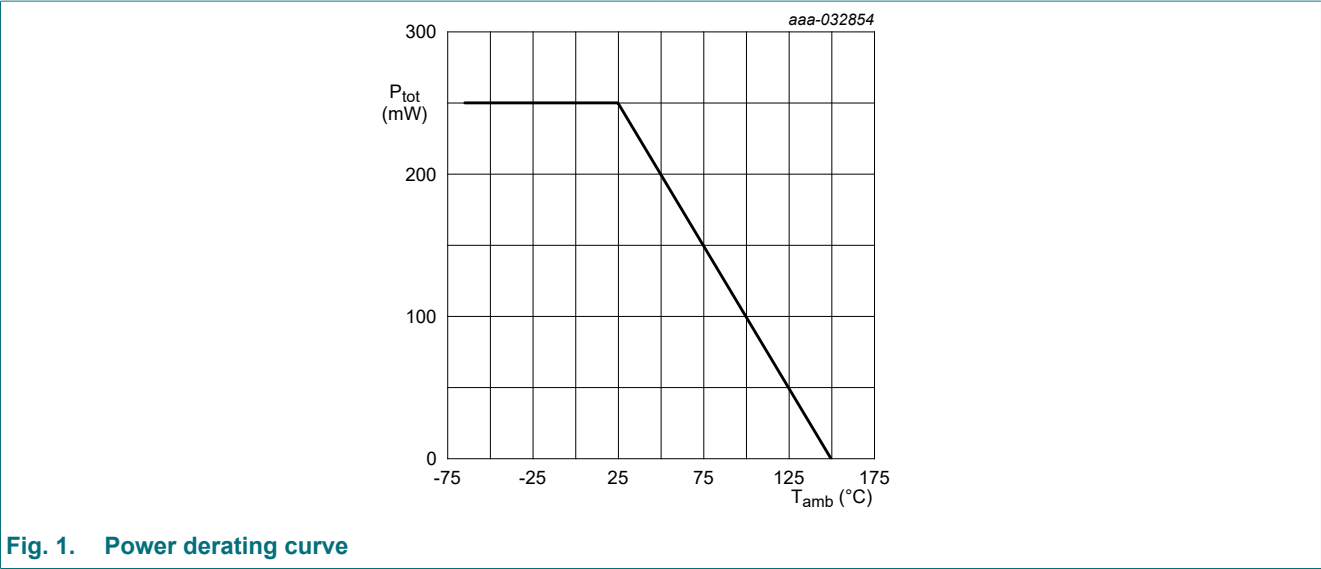


Fig. 1. Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	500	K/W

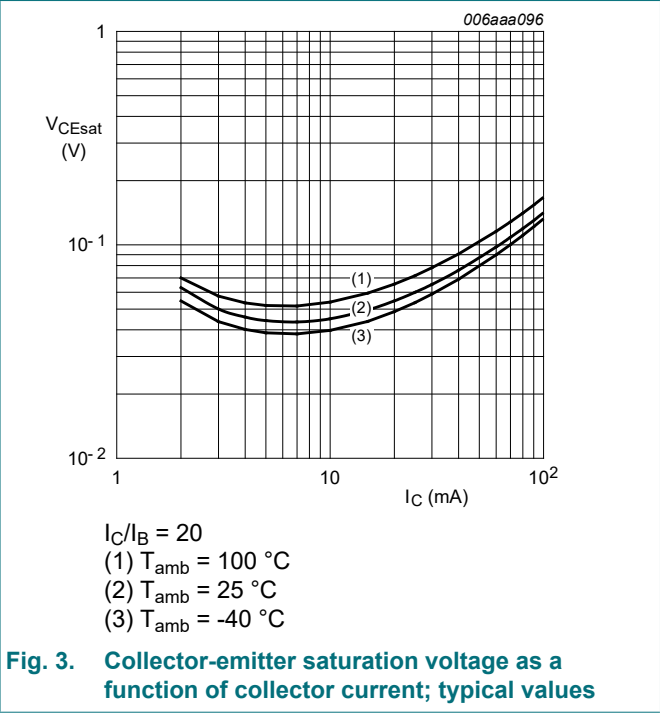
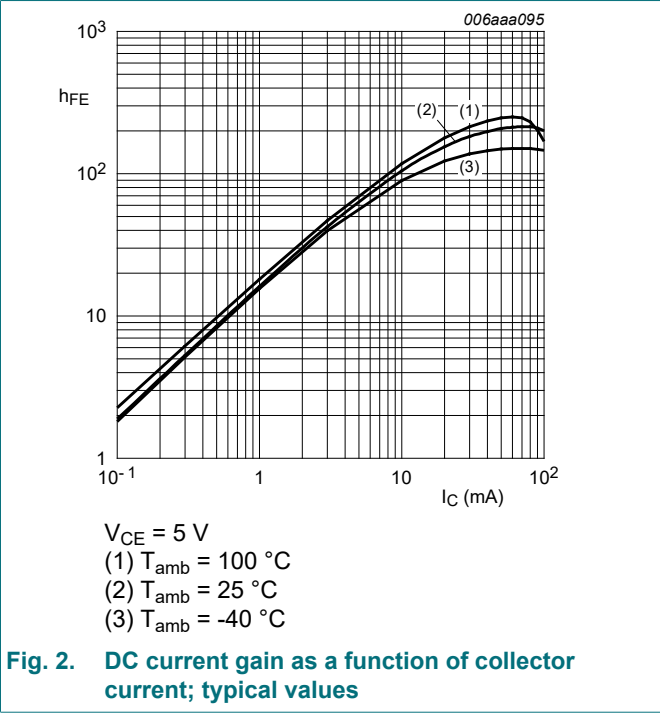
[1] Device mounted on an FR4 PCB, single-sided, 60 μm copper, tin-plated and standard footprint.  
[2] Reflow soldering is the only recommended soldering method.

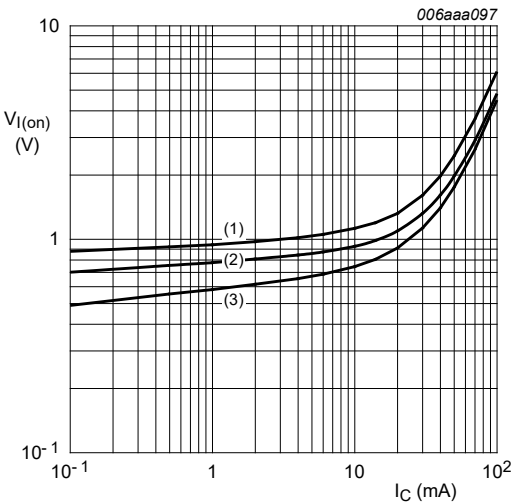
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\text{ }\mu\text{A}$ ; $I_E = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2\text{ mA}$ ; $I_B = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	50	-	-	V
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50\text{ V}$ ; $I_E = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	100	nA
		$V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_j = 150\text{ }^{\circ}\text{C}$	-	-	5	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}$ ; $I_C = 0\text{ A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	700	$\mu\text{A}$
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}$ ; $I_C = 5\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	35	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}$ ; $I_B = 0.5\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$ ; $I_C = 100\text{ }\mu\text{A}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	0.75	0.3	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 300\text{ mV}$ ; $I_C = 20\text{ mA}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	2.5	1.15	-	V
R1	bias resistor 1 (input)	[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio	[1]	3.6	4.5	5.5	
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}$ ; $I_E = 0\text{ A}$ ; $i_e = 0\text{ A}$ ; $f = 1\text{ MHz}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	2	pF

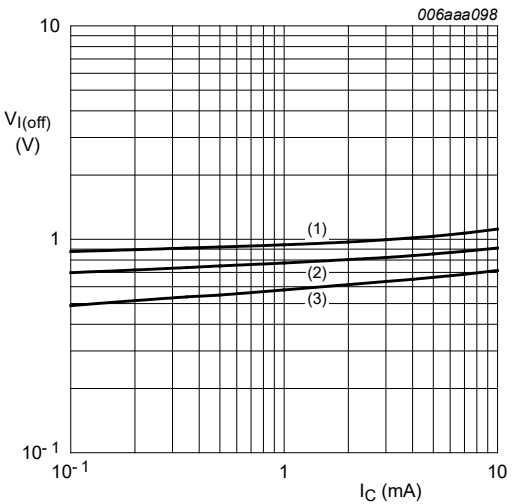
[1] See "Section 11: Test information" for resistor calculation and test conditions.





$V_{CE} = 0.3$  V  
(1)  $T_{amb} = -40$  °C  
(2)  $T_{amb} = 25$  °C  
(3)  $T_{amb} = 100$  °C

Fig. 4. On-state input voltage as a function of collector current; typical values



$V_{CE} = 5$  V  
(1)  $T_{amb} = -40$  °C  
(2)  $T_{amb} = 25$  °C  
(3)  $T_{amb} = 100$  °C

Fig. 5. Off-state input voltage as a function of collector current; typical values

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

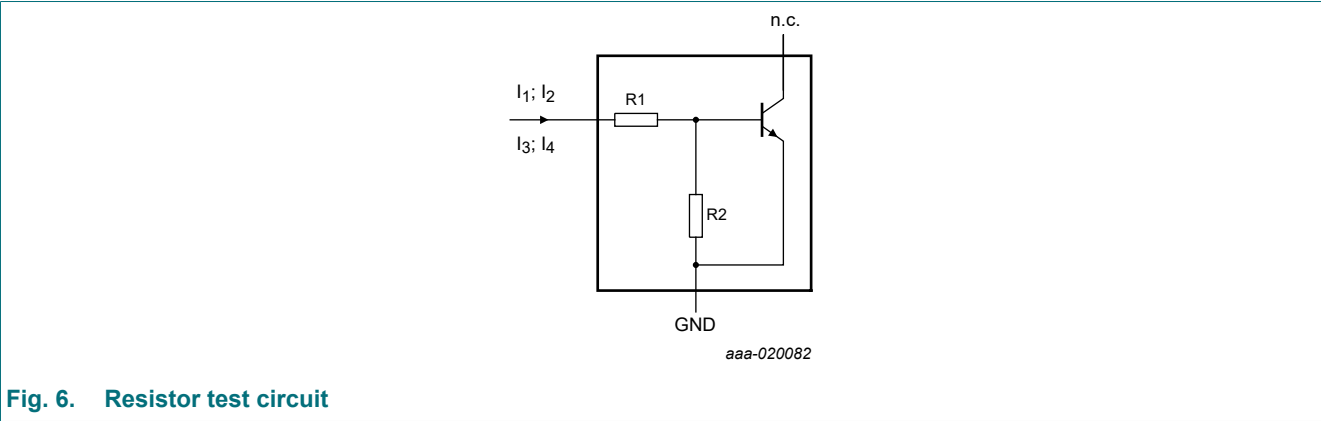


Fig. 6. Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>
PDTC123YM	2.2	10	1300 μA	1500 μA	-350 μA	-450 μA

12. Package outline

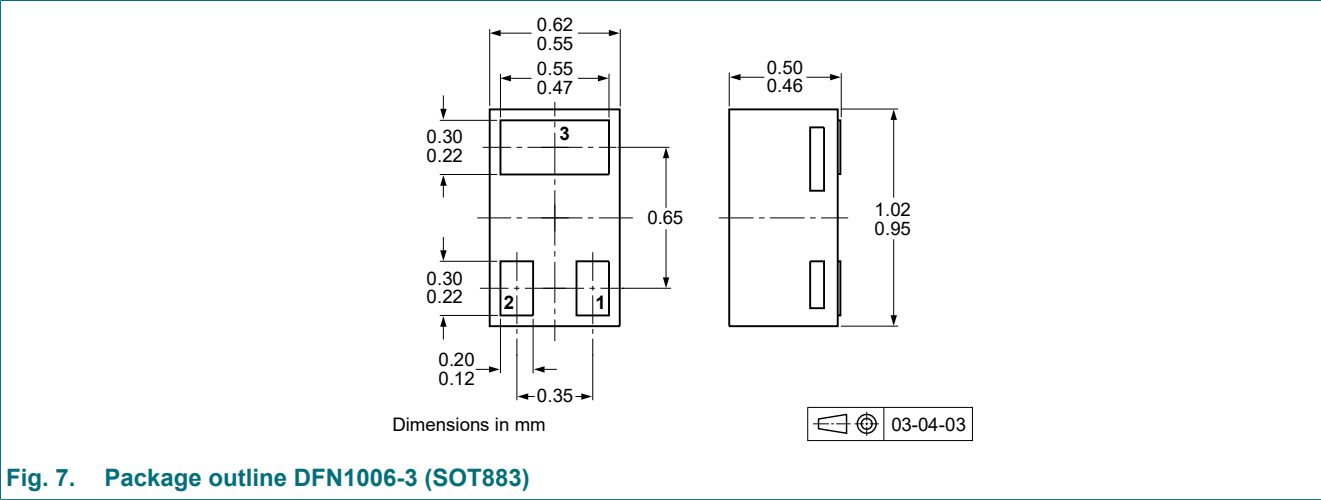


Fig. 7. Package outline DFN1006-3 (SOT883)

13. Soldering

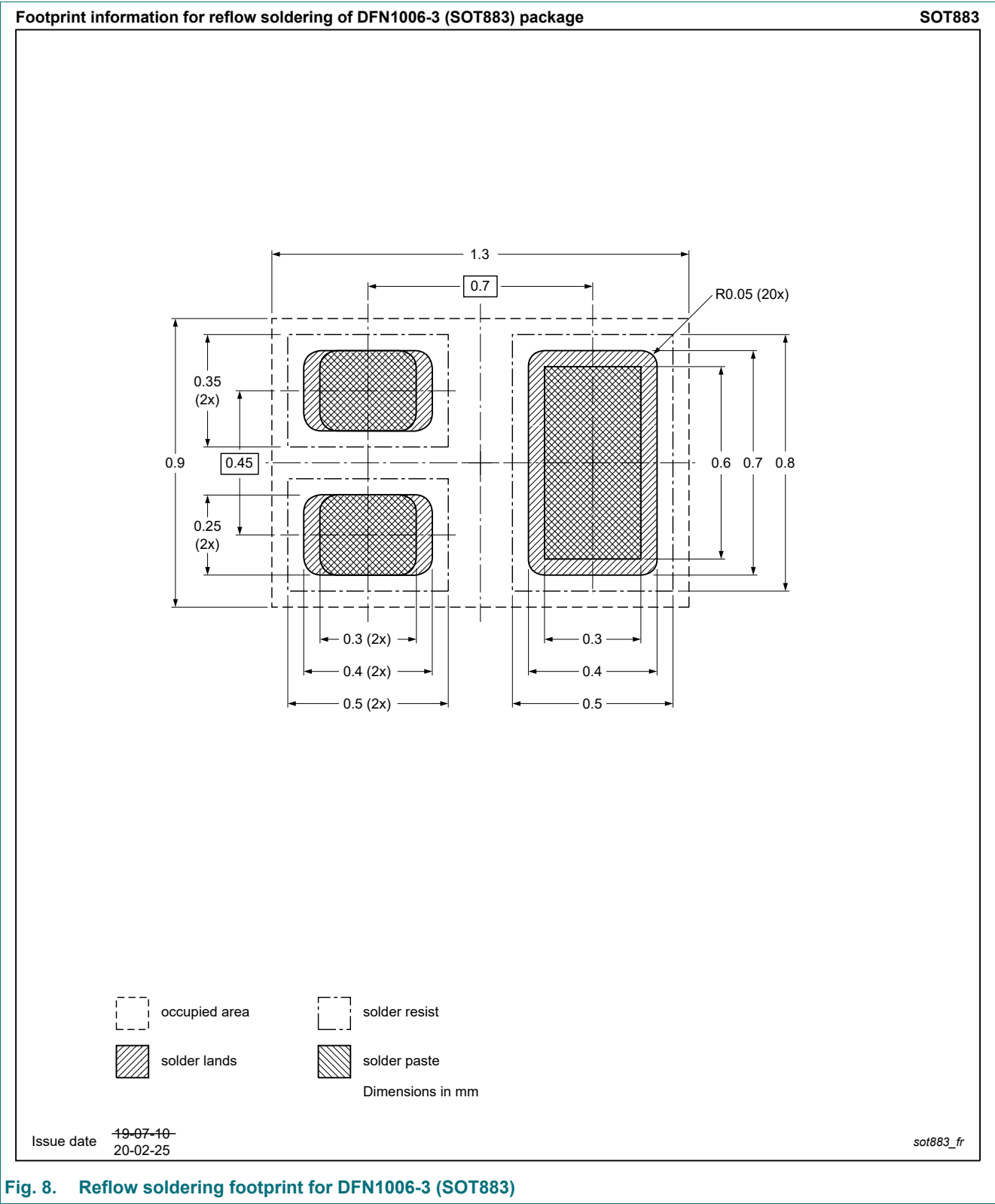


Fig. 8. Reflow soldering footprint for DFN1006-3 (SOT883)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTC123YM v.5	20241206	Product data sheet	-	PDTC123Y_SER_4
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Section "Packing information" removed.</li><li>Family data sheet splitted to single type data sheets.</li></ul>			
PDTC123Y_SER_4	20091116	Product data sheet	-	PDTC123Y_SER_3
PDTC123Y_SER_3	20050324	Product data sheet	-	PDTC123YT_2
PDTC123YT_2	20040510	Objective data sheet	-	PDTC123YT_1
PDTC123YT_1	20040406	Objective data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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