PESD2ETHD-Q

Ultra low capacitance double rail-to-rail ESD protection diode

24 May 2023 **Product data sheet**

1. General description

Ultra low capacitance double rail-to-rail ElectroStatic Discharge (ESD) protection diode in a small SOT457 Surface-Mounted Device (SMD) plastic package. The device is designed to protect two high-speed data lines or high-frequency signal lines from the damage caused by ESD and other transients. The device integrates two ultra low capacitance rail-to-rail diodes and one additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

2. Features and benefits

- ESD protection of two high-speed data lines
- Ultra low capacitance: C_D = 1.3 pF
- ISO 10605 (330 pF, 2 kΩ) up to 15 kV
- ESD protection up to 8 kV
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- 100BASE-T1 / OPEN Allicance BroadR-Reach automotive Ethernet
- Low-Voltage Differential Signaling (LVDS) automotive
- USB 2.0 automotive

4. Quick reference data

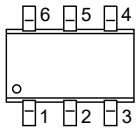
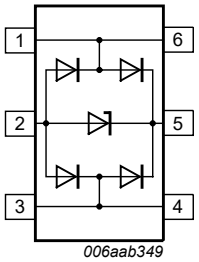
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
Zener diode							
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[1]	-	16	-	pF
Per channel							
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[2]	-	1.3	1.5	pF

[1] Measured from pin 5 to ground.
[2] Measured from pin 4 or 6 to ground.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I/O 1	input/output 1	 TSOP6 (SOT457)	
2	GND	ground		
3	I/O 2	input/output 2		
4	I/O 2	input/output 2		
5	V_{CC}	supply voltage		
6	I/O 1	input/output 1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2ETHD-Q	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD2ETHD-Q	L8

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1]	-	2.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	-	8	kV
		MIL-STD-883; human body model (HBM)		-	10	kV

[1] Measured from pin 1,3,4 or 6 to GND.
[2] According to IEC61000-4-5.
[3] Device stressed with ten non-repetitive ESD pulses.

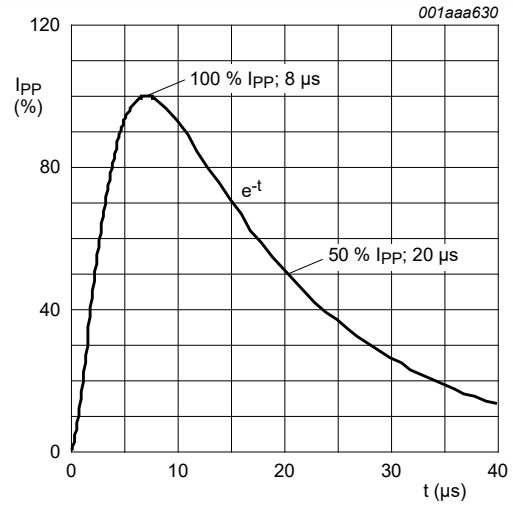


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

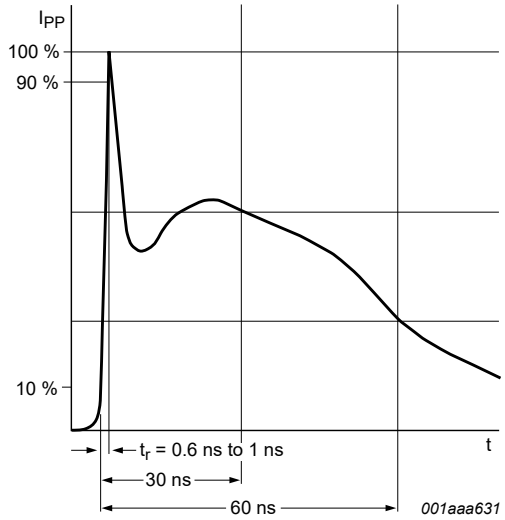


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_F	forward voltage	I_F = 1 mA; T_{amb} = 25 °C		-	0.7	-	V
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
I_{RM}	reverse leakage current	V_R = 5.5 V; T_{amb} = 25 °C	[1]	-	1	100	nA
V_{CL}	clamping voltage	I_{PPM} = 2.5 A; t_p = 8/20 µs; T_{amb} = 25 °C	[1] [2]	-	11.8	-	V
R_{dyn}	dynamic resistance	I_R = 10 A; t_p = 100 ns; T_{amb} = 25 °C	[1] [3]	-	1.1	-	Ω
Zener diode							
V_{BR}	breakdown voltage	I_R = 1 mA; T_{amb} = 25 °C	[4]	6	-	9	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[4]	-	16	-	pF
Per channel							
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[5]	-	1.3	1.5	pF

[1] Measured from pin 1,3,4 or 6 to GND.
[2] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.
[4] Measured from pin 5 to ground.
[5] Measured from pin 4 or 6 to ground.

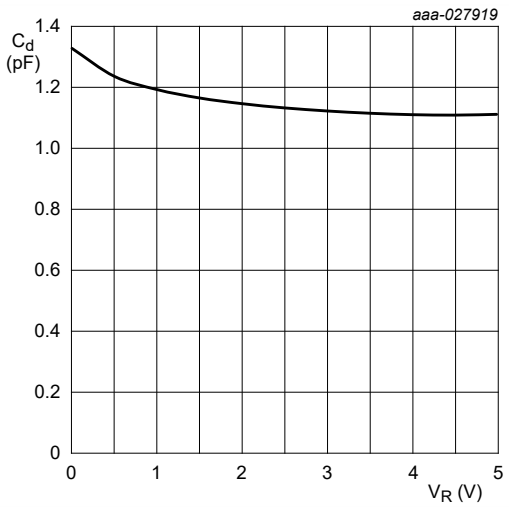


Fig. 3. Input/output to ground capacitance as a function of reverse voltage

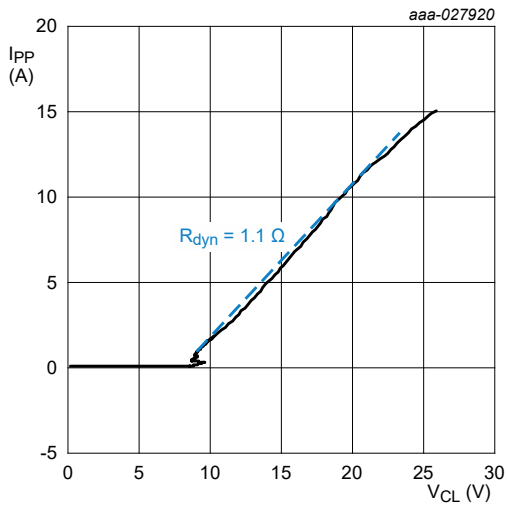


Fig. 4. Dynamic resistance with positive clamping; typical values; Input/output to ground

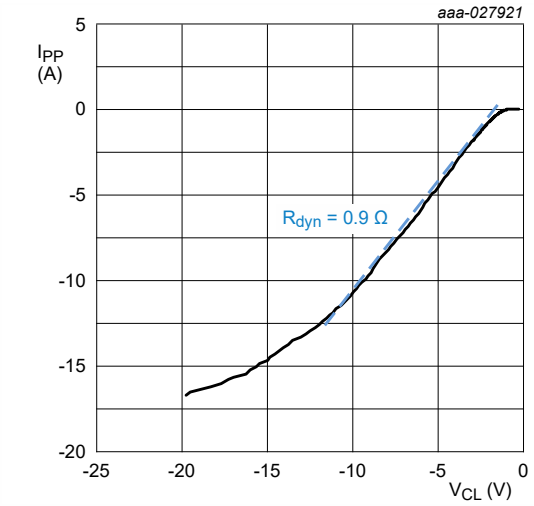


Fig. 5. Dynamic resistance with negative clamping; typical values; Input/output to ground

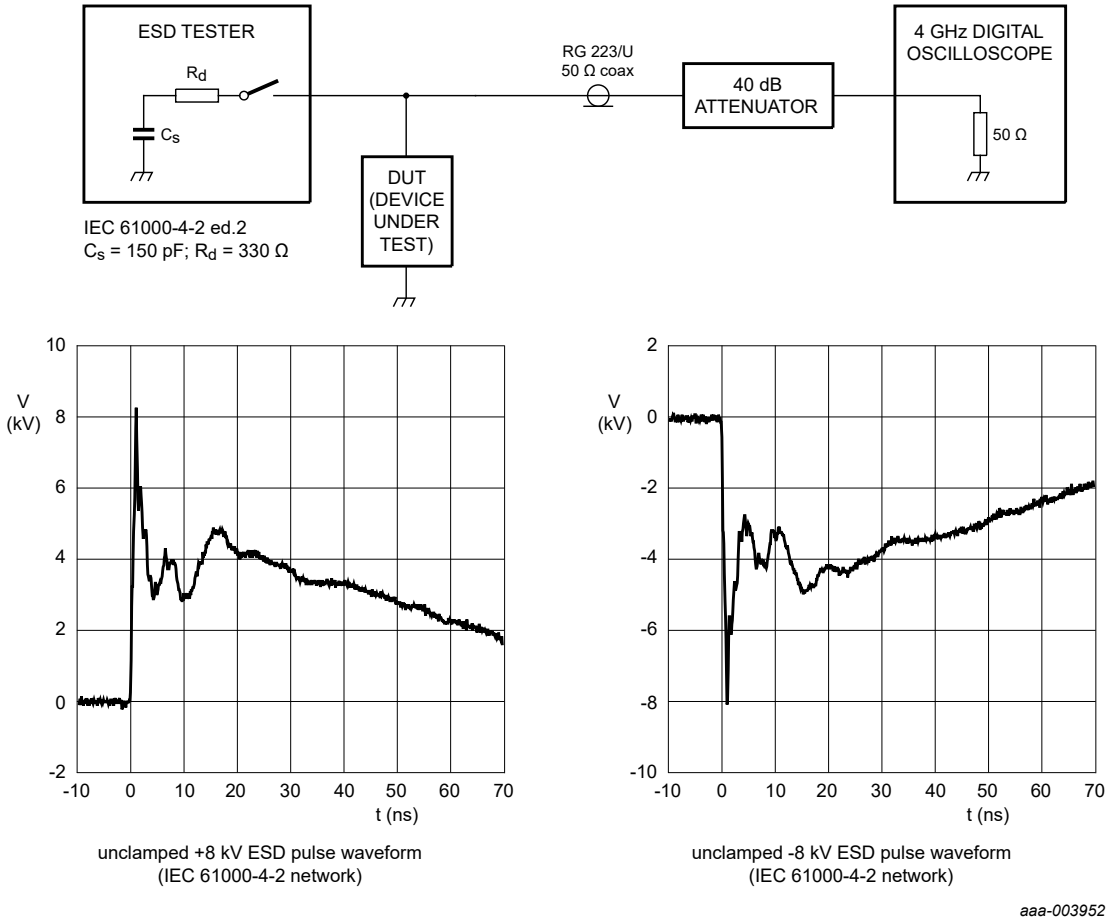


Fig. 6. ESD clamping test setup and waveforms

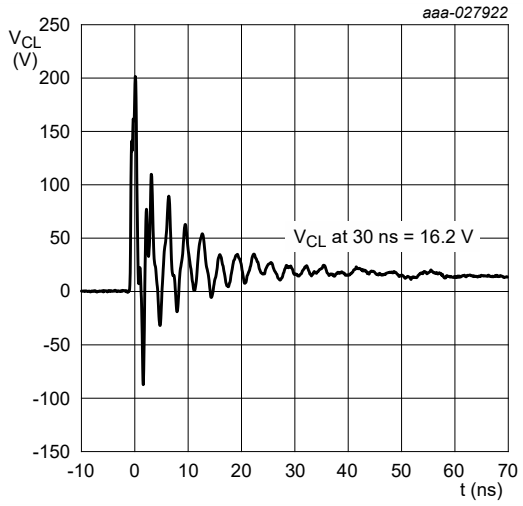


Fig. 7. Clamped +8kV pulse waveform (IEC61000-4-2 network)

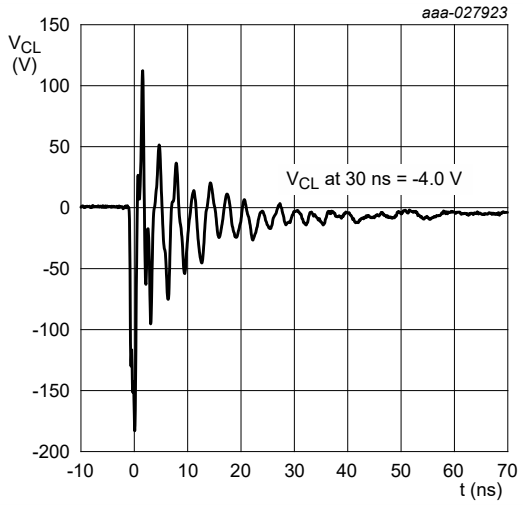


Fig. 8. Clamped -8kV pulse waveform (IEC61000-4-2 network)

10. Application information

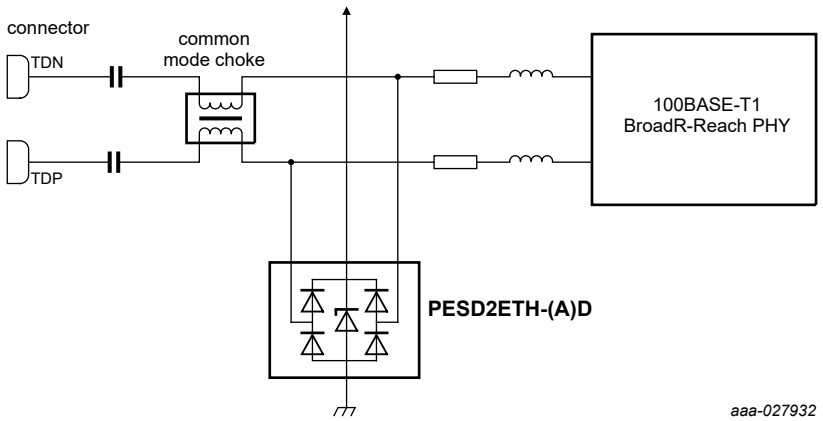


Fig. 9. Application diagram: BroadR-Reach PHY / 100BASE-T1

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

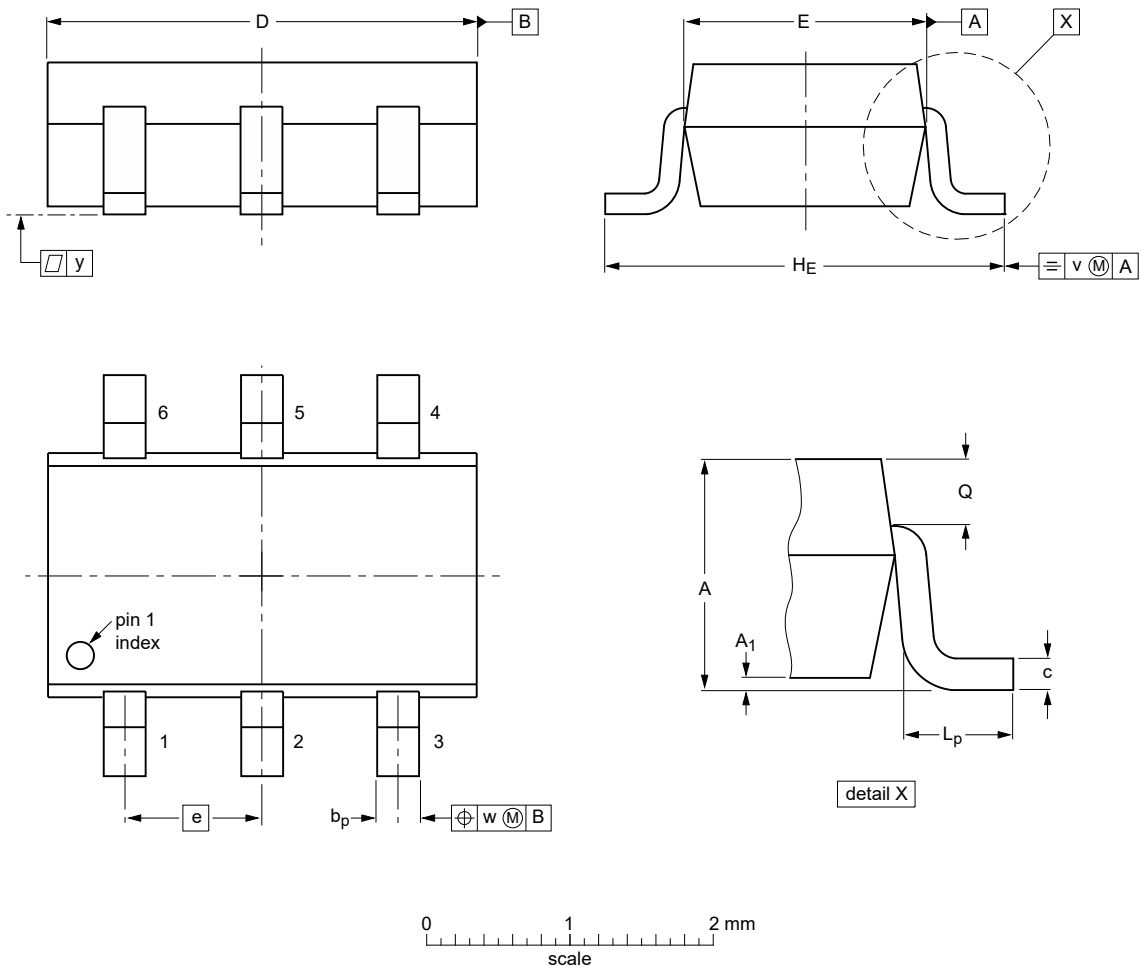
11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

Plastic, surface-mounted package (SC-74; TSOP6); 6 leads **SOT457**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	max	1.1	0.1	0.40	0.26	3.1	1.7	0.95	3.0	0.6	0.33	0.2	0.2	0.1
	nom													
	min	0.9	0.013	0.25	0.10	2.7	1.3		2.5	0.2	0.23			

sot457_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~06-03-16~~ 18-11-27

Fig. 10. Package outline TSOP6 (SOT457)

13. Soldering

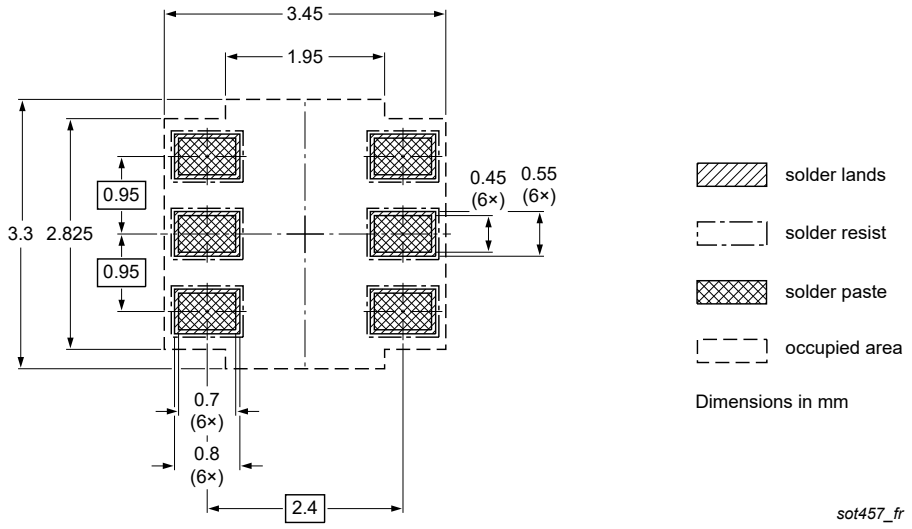


Fig. 11. Reflow soldering footprint for TSOP6 (SOT457)

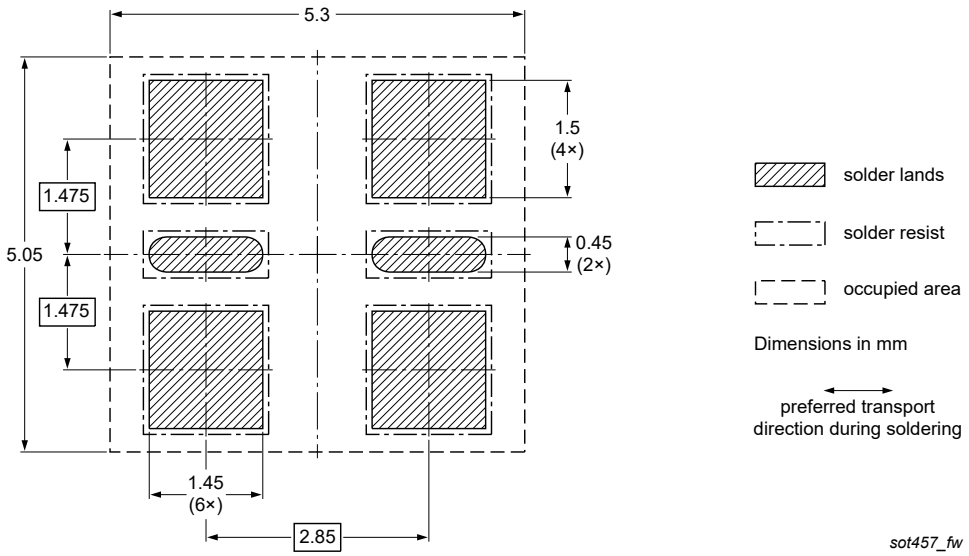


Fig. 12. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2ETHD-Q v.1	20230524	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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