

74HCT221

Dual non-retriggerable monostable multivibrator with reset

Rev. 4 — 4 April 2024

Product data sheet

1. General description

The 74HCT221 is a dual non-retriggerable monostable multivibrator. Each multivibrator features edge-triggered inputs ($\overline{nA}$ and nB), either of which can be used as an enable input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the nB inputs allow jitter-free triggering from inputs with slow transition rates, providing the circuit with excellent noise immunity. Once triggered, the outputs (nQ , $\overline{nQ}$) are independent of further transitions of $\overline{nA}$ and nB inputs. The output pulse width is defined by the following relationship:

$$t_W = 0.7 \times C_{EXT}R_{EXT}$$

The output pulses can be terminated by the active LOW reset inputs ($\overline{nRD}$). Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications pulse stability will only be limited by the accuracy of the external timing components. This device features reduced input threshold levels to allow interfacing to TTL logic levels. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

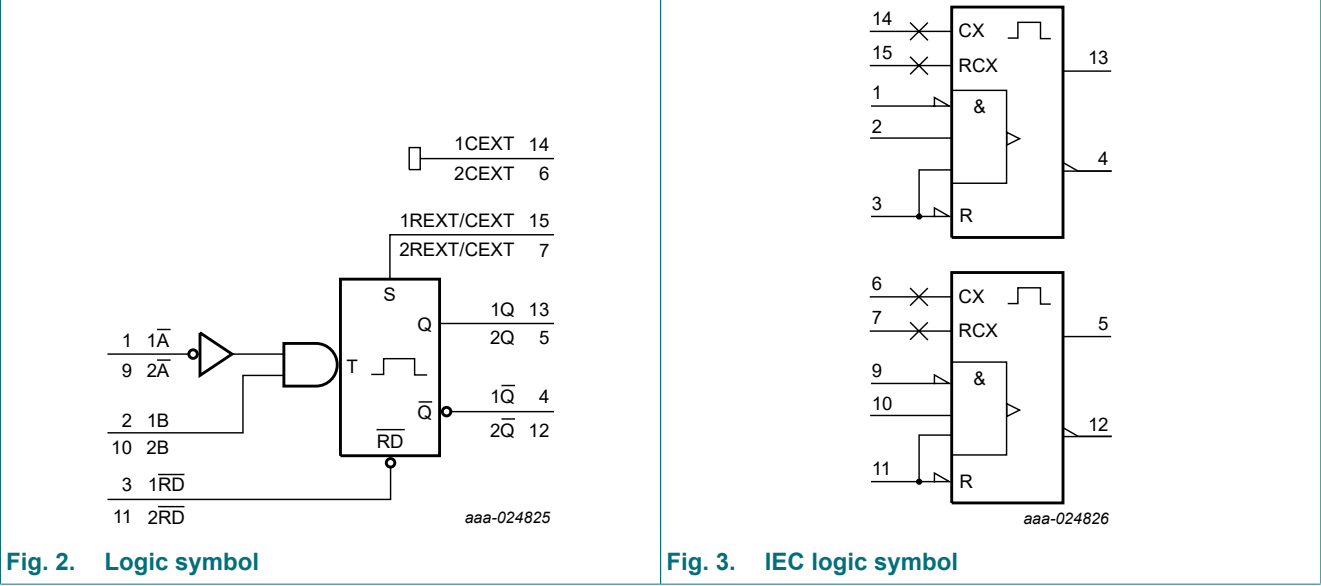
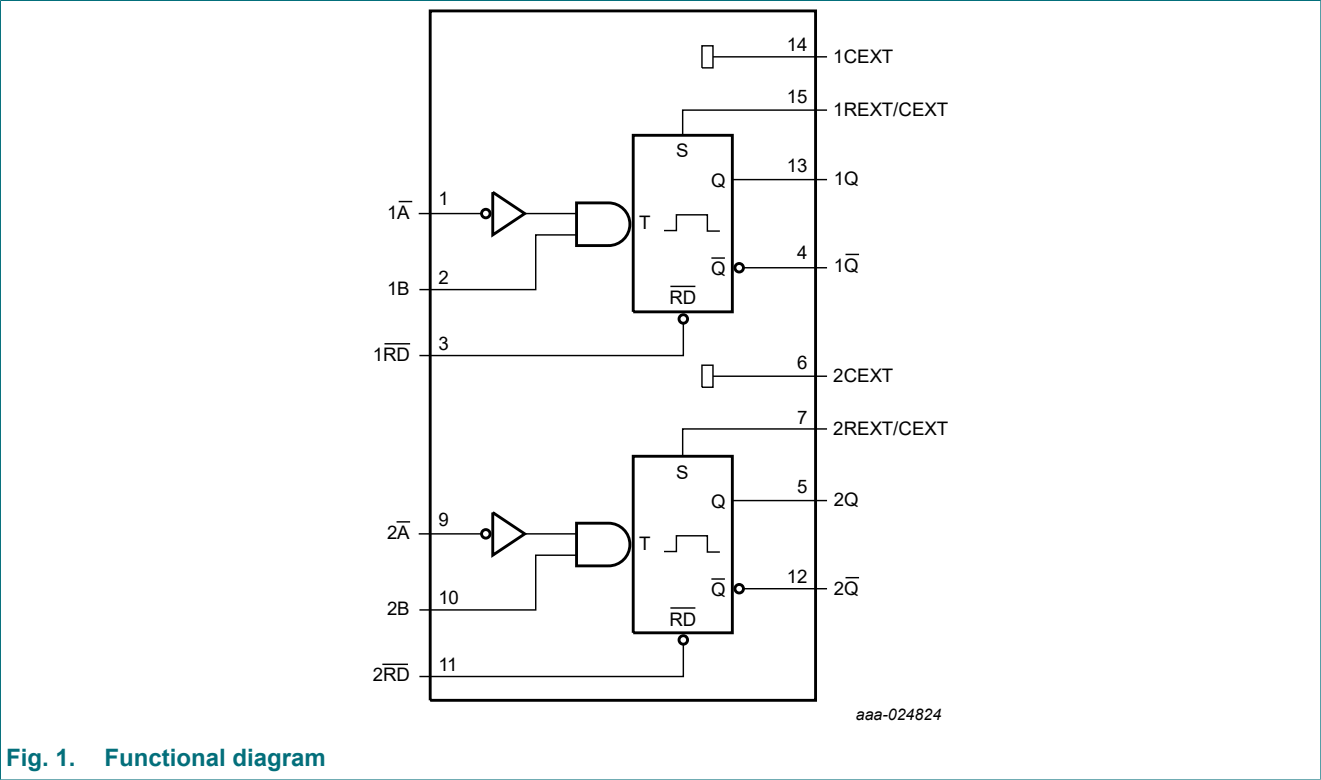
- Supply voltage range from 4.5 V to 5.5 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
 - For 74HCT221: TTL level
- Pulse width variance is typically less than $\pm 5\%$
- Direct reset terminates output pulse
- Schmitt-trigger action on nB inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCT221D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram



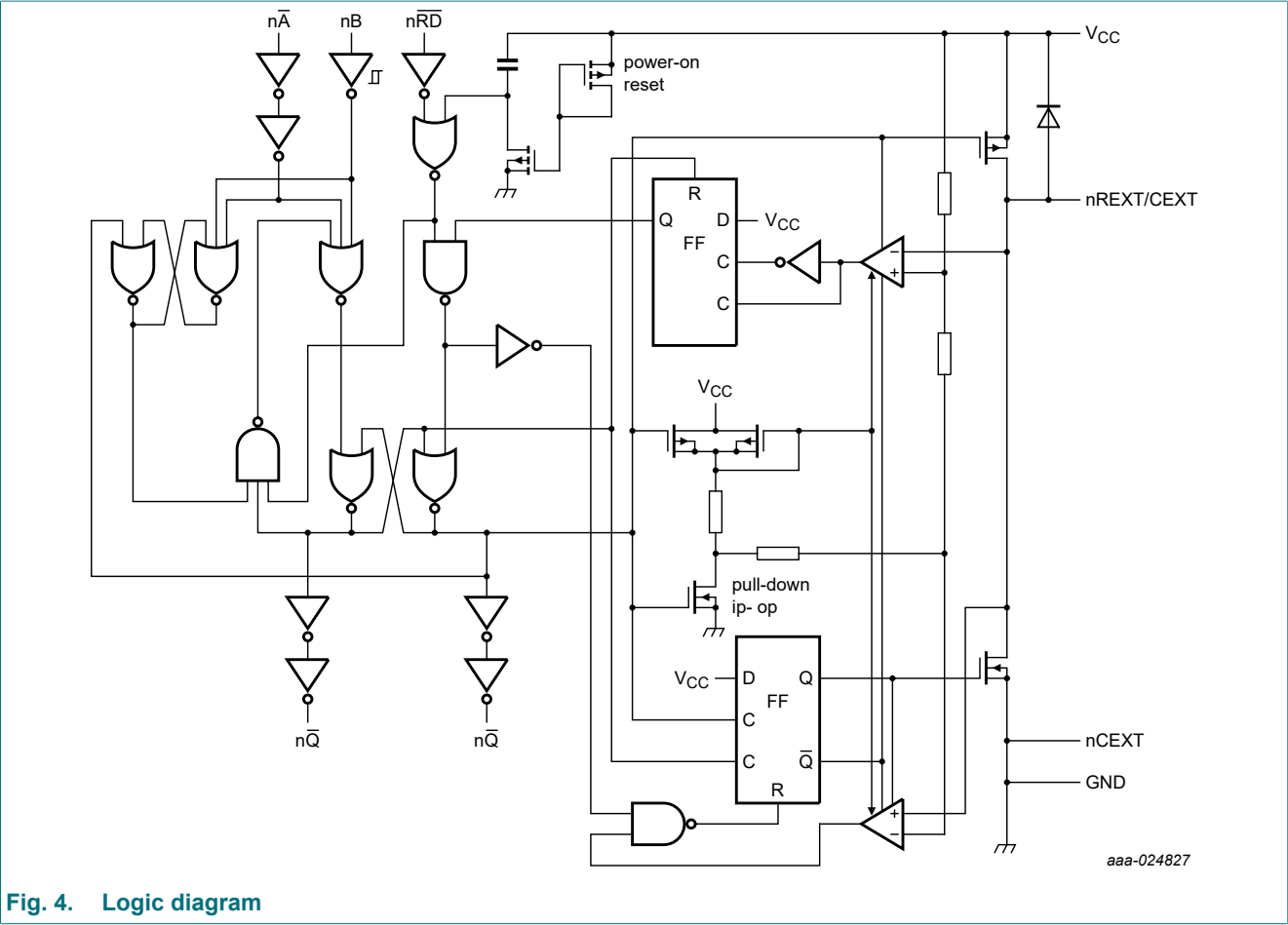


Fig. 4. Logic diagram

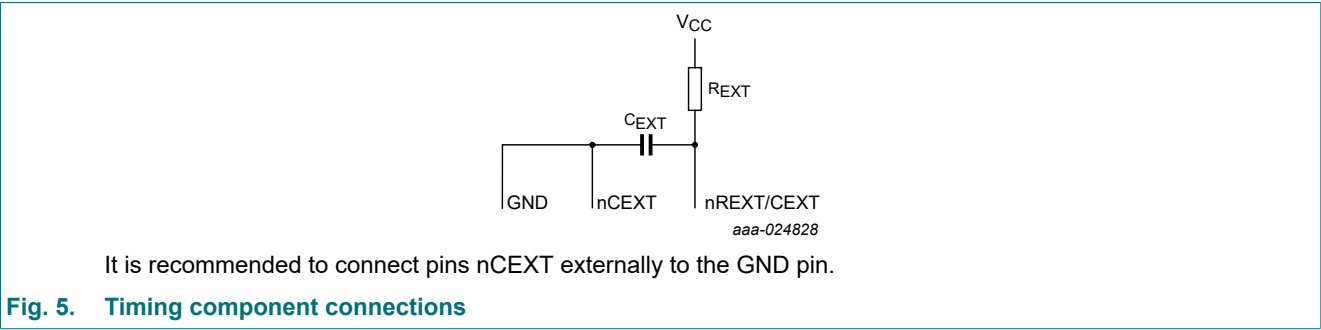


Fig. 5. Timing component connections

5. Pinning information

5.1. Pinning

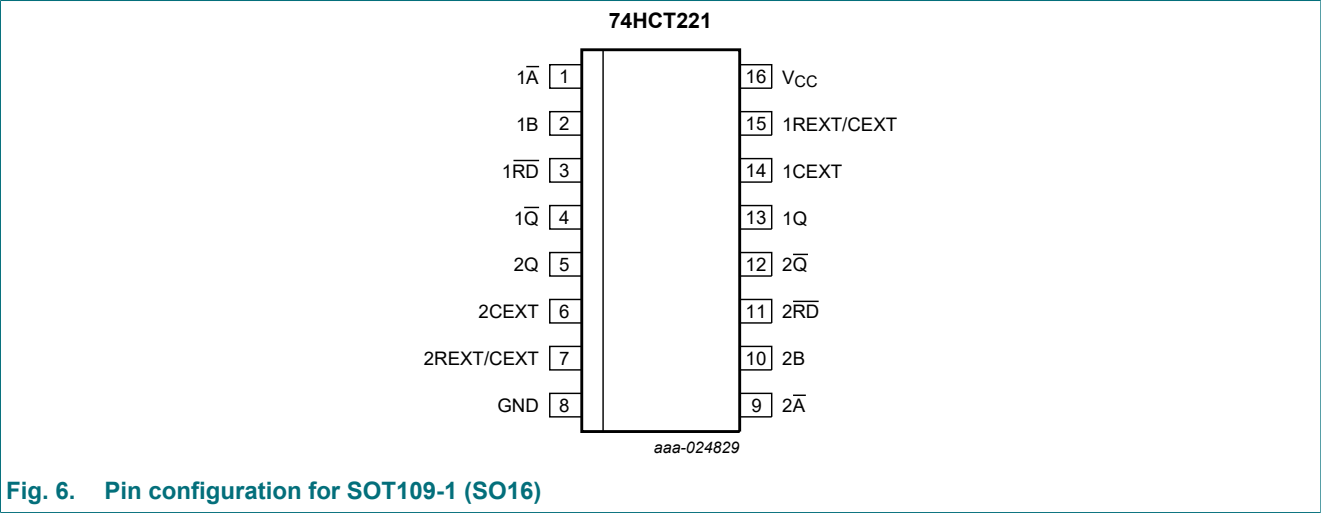


Fig. 6. Pin configuration for SOT109-1 (SO16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
1RD	3	direct reset LOW and positive-edge triggered input 1
1Q	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
2A	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
2RD	11	direct reset LOW and positive-edge triggered input 2
2Q	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
VCC	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition;
 = one HIGH level output pulse;  = one LOW level output pulse.

Input			Output	
nRD	nA	nB	nQ	nQ
L	X	X	L	H
X	H	X	L [1]	H [1]
X	X	L	L [1]	H [1]
H	L	↑		
H	↓	H		
↑	L	H	 [2]	 [2]

- [1] If the monostable was triggered before this condition was established, the pulse will continue as programmed.
[2] For this combination the reset input must be LOW and the following sequence must be used: pin nA must be set HIGH or pin nB set LOW; then pin nA must be LOW and pin nB set HIGH. Now the reset input goes from LOW-to-HIGH and the device will be triggered.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	except for pins nREXT/CEXT; V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	SO16 package [1]	-	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rate	nA, nRD input				
		V _{CC} = 4.5 V	-	1.67	139	ns/V
T _{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; I _O = 0 A; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		pin nB	-	30	108	-	135	-	147	µA
		pins nA, nRD	-	50	180	-	225	-	245	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 15.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; see Fig. 7 and Fig. 8								
		nA, nRD to nQ (trigger)								
		V _{CC} = 4.5 V	-	30	50	-	63	-	75	ns
		V _{CC} = 5 V; C _L = 15 pF	-	36	-	-	-	-	-	ns
		nB to nQ (trigger)								
		V _{CC} = 4.5 V	-	24	42	-	53	-	63	ns
		V _{CC} = 5 V; C _L = 15 pF	-	36	-	-	-	-	-	ns
		nRD to nQ (reset)								
		V _{CC} = 4.5 V	-	31	51	-	64	-	77	ns
		V _{CC} = 5 V; C _L = 15 pF	-	36	-	-	-	-	-	ns

Dual non-retriggerable monostable multivibrator with reset

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PHL}	HIGH to LOW propagation delay	C _{EXT} = 0 pF; R _{EXT} = 5 kΩ; see Fig. 7 and Fig. 8								
		n $\bar{A}$ to n $\bar{Q}$ (trigger)								
		V _{CC} = 4.5 V	-	26	44	-	55	-	75	ns
		V _{CC} = 5 V; C _L = 15 pF	-	32	-	-	-	-	-	ns
		nB to n $\bar{Q}$ (trigger)								
		V _{CC} = 4.5 V	-	21	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	32	-	-	-	-	-	ns
		nRD to n $\bar{Q}$ (trigger)								
		V _{CC} = 4.5 V	-	26	43	-	54	-	65	ns
		V _{CC} = 5 V; C _L = 15 pF	-	32	-	-	-	-	-	ns
		nRD to nQ (reset)								
		V _{CC} = 4.5 V	-	26	43	-	54	-	65	ns
		V _{CC} = 5 V; C _L = 15 pF	-	32	-	-	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see Fig. 7 [1]	-	7	15	-	19	-	22	ns
t _W	pulse width	n $\bar{A}$ LOW; nB HIGH; (trigger); see Fig. 7								
		V _{CC} = 4.5 V	20	13	-	25	-	30	-	ns
		nRD LOW; see Fig. 10								
		V _{CC} = 4.5 V	22	13	-	28	-	33	-	ns
		nQ HIGH and n $\bar{Q}$ LOW; see Fig. 8								
		V _{CC} = 5 V; C _{EXT} = 100 nF; R _{EXT} = 10 kΩ	630	700	770	602	798	595	805	μs
		nQ or n $\bar{Q}$ (trigger); see Fig. 8								
		V _{CC} = 4.5 V; C _{EXT} = 28 pF; R _{EXT} = 2 kΩ	-	140	-	-	-	-	-	ns
t _{rec}	recovery time	V _{CC} = 4.5 V; C _{EXT} = 1 nF; R _{EXT} = 2 kΩ	-	1.5	-	-	-	-	-	μs
		V _{CC} = 4.5 V; C _{EXT} = 1 nF; R _{EXT} = 10 kΩ	-	7	-	-	-	-	-	μs
t _{rec}	recovery time	nRD to n $\bar{A}$, nB; see Fig. 11	20	12	-	25	-	30	-	ns
R _{EXT}	external timing resistor	V _{CC} = 5.0 V; see Fig. 13	2	-	1 000	-	-	-	-	kΩ
C _{EXT}	external timing capacitor	V _{CC} = 5.0 V; see Fig. 13	no limits							pF
C _{PD}	power dissipation capacitance	per monostable; V _I = GND to V _{CC} - 1.5 V [2]	-	96	-	-	-	-	-	pF

[1] t_t is the same as t_{THL} and t_{TLH}

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + 0.33 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 28 \times V_{CC} \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz;

D = duty factor in %; C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

C_{EXT} = timing capacitance in pF; $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

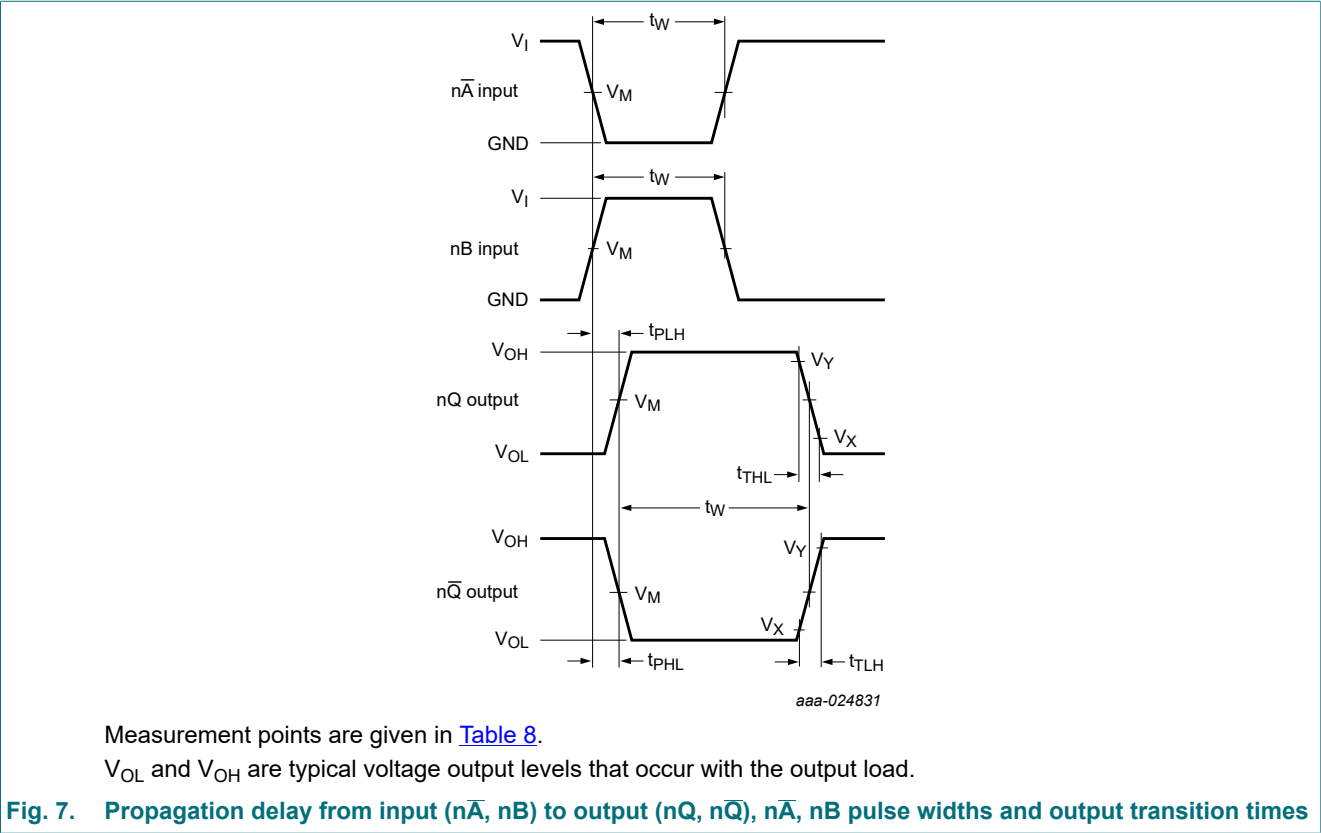
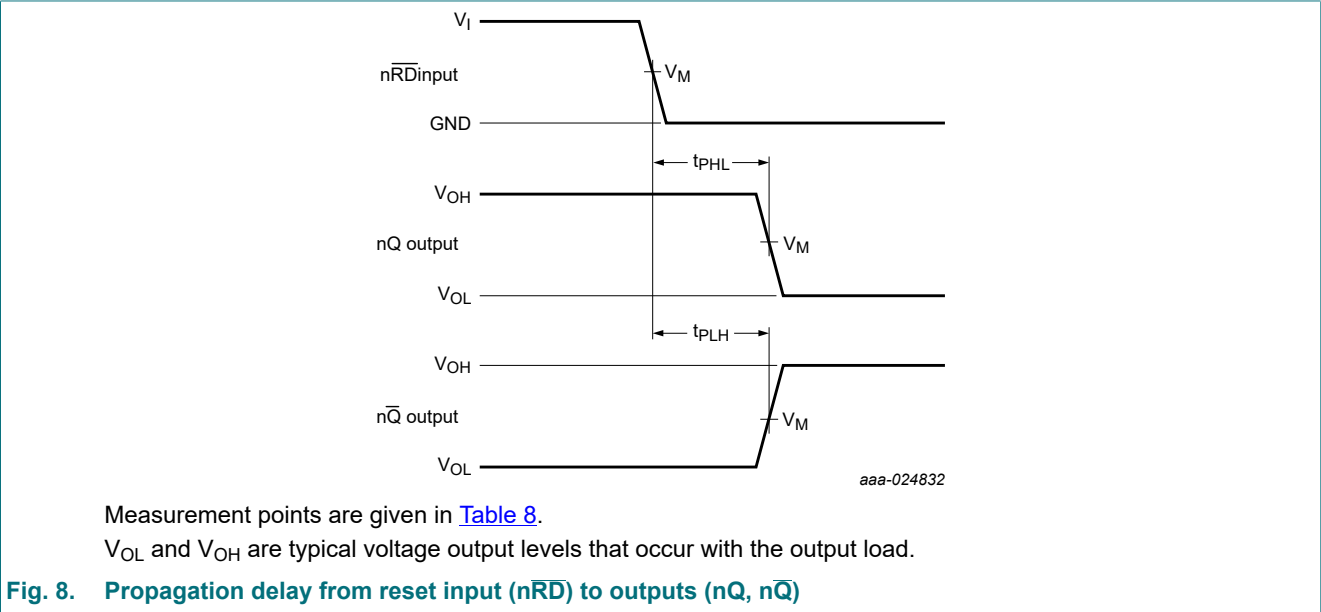
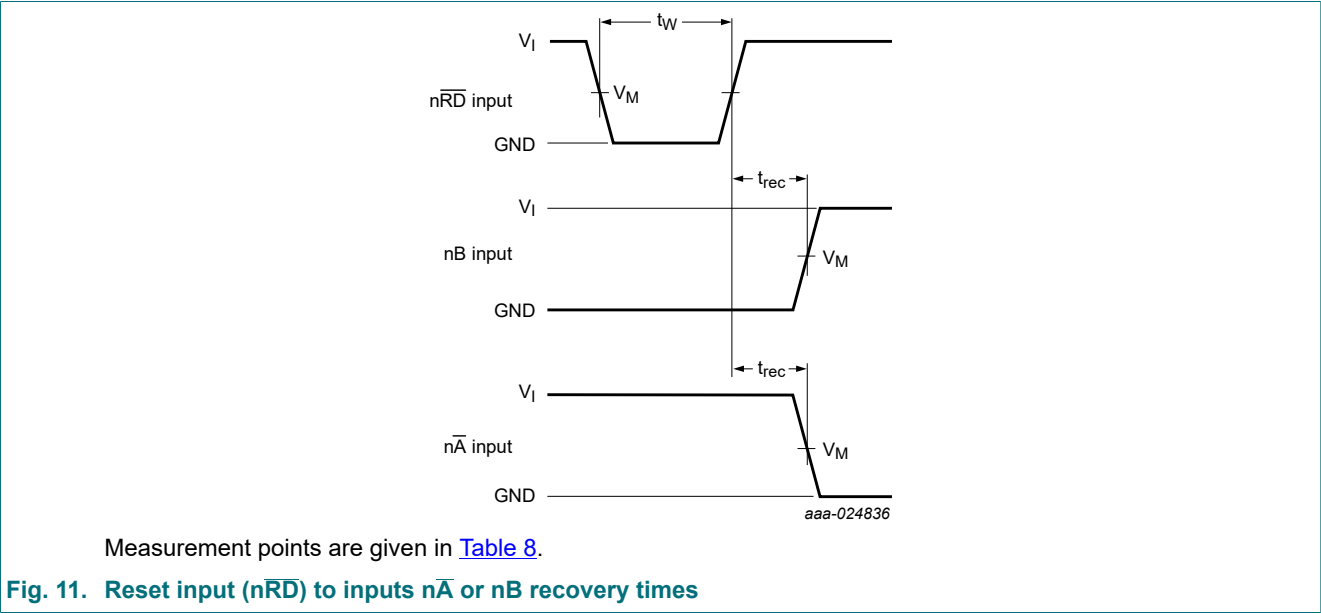
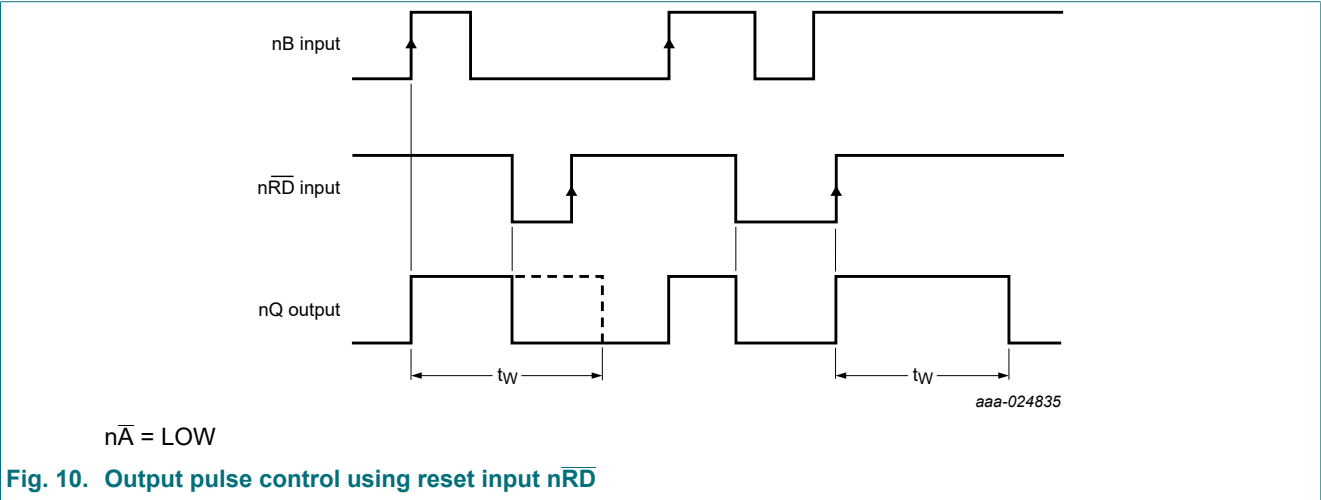
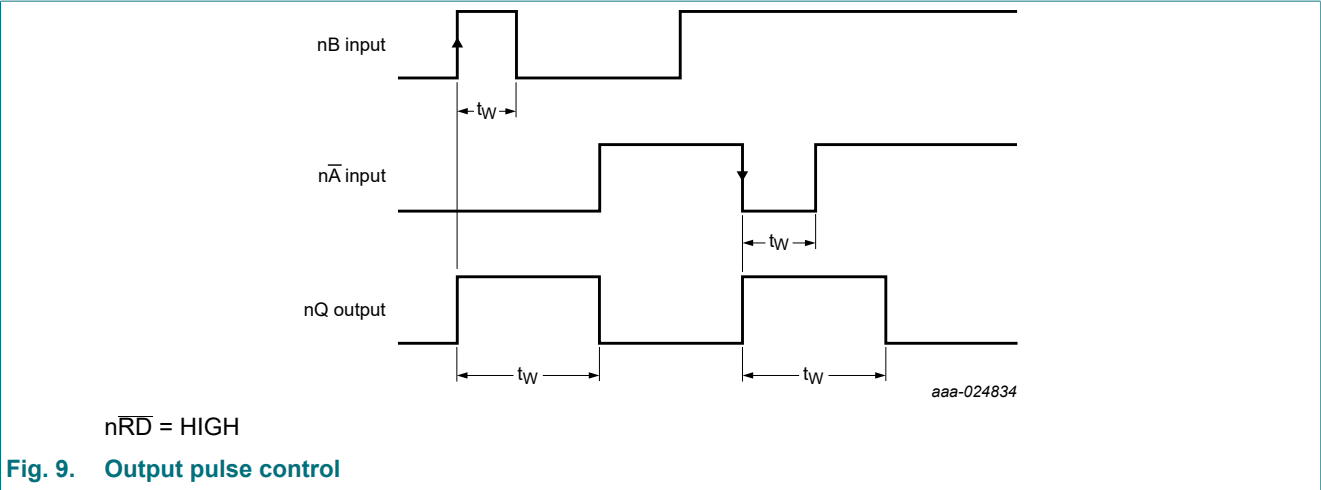


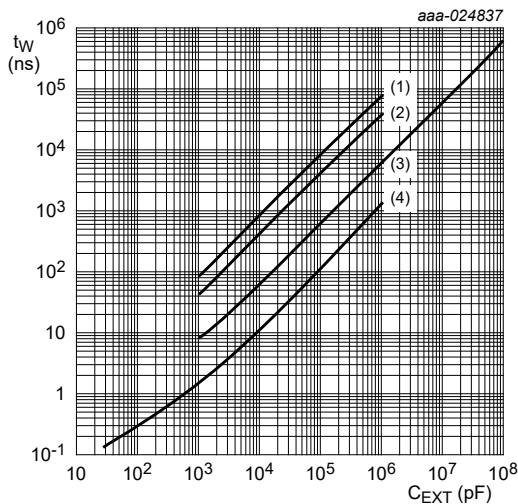
Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



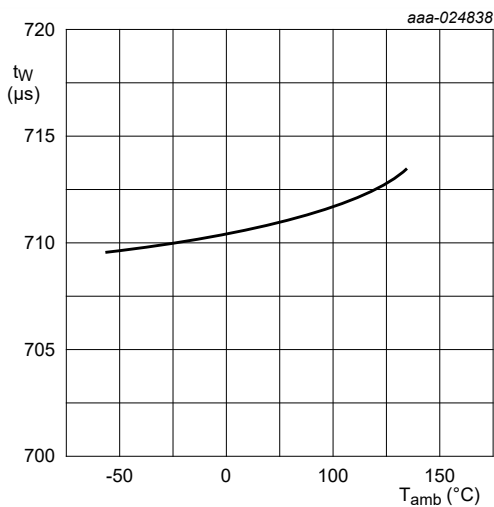
Dual non-retriggerable monostable multivibrator with reset





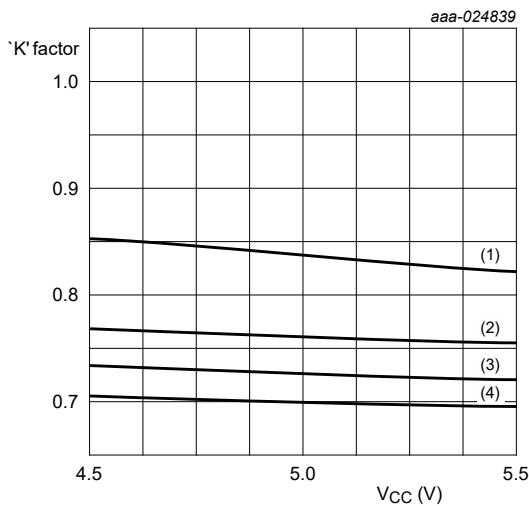
$V_{CC} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}.$
(1) $R_{EXT} = 100\text{ k}\Omega$
(2) $R_{EXT} = 50\text{ k}\Omega$
(3) $R_{EXT} = 10\text{ k}\Omega$
(4) $R_{EXT} = 2\text{ k}\Omega$

Fig. 12. Typical output pulse width as a function of the external capacitor



$C_{EXT} = 0.1\text{ }\mu\text{F}; R_{EXT} = 10\text{ k}\Omega; V_{CC} = 5.0\text{ V}$

Fig. 13. Typical output pulse width as a function of the ambient temperature



$R_{EXT} = 10\text{ k}\Omega; T_{amb} = 25\text{ }^{\circ}\text{C}.$
(1) $C_{EXT} = 0.001\text{ }\mu\text{F}$
(2) $C_{EXT} = 0.01\text{ }\mu\text{F}$
(3) $C_{EXT} = 0.1\text{ }\mu\text{F}$
(4) $C_{EXT} = 1\text{ }\mu\text{F}$

Fig. 14. "K" factor as function of the supply voltage

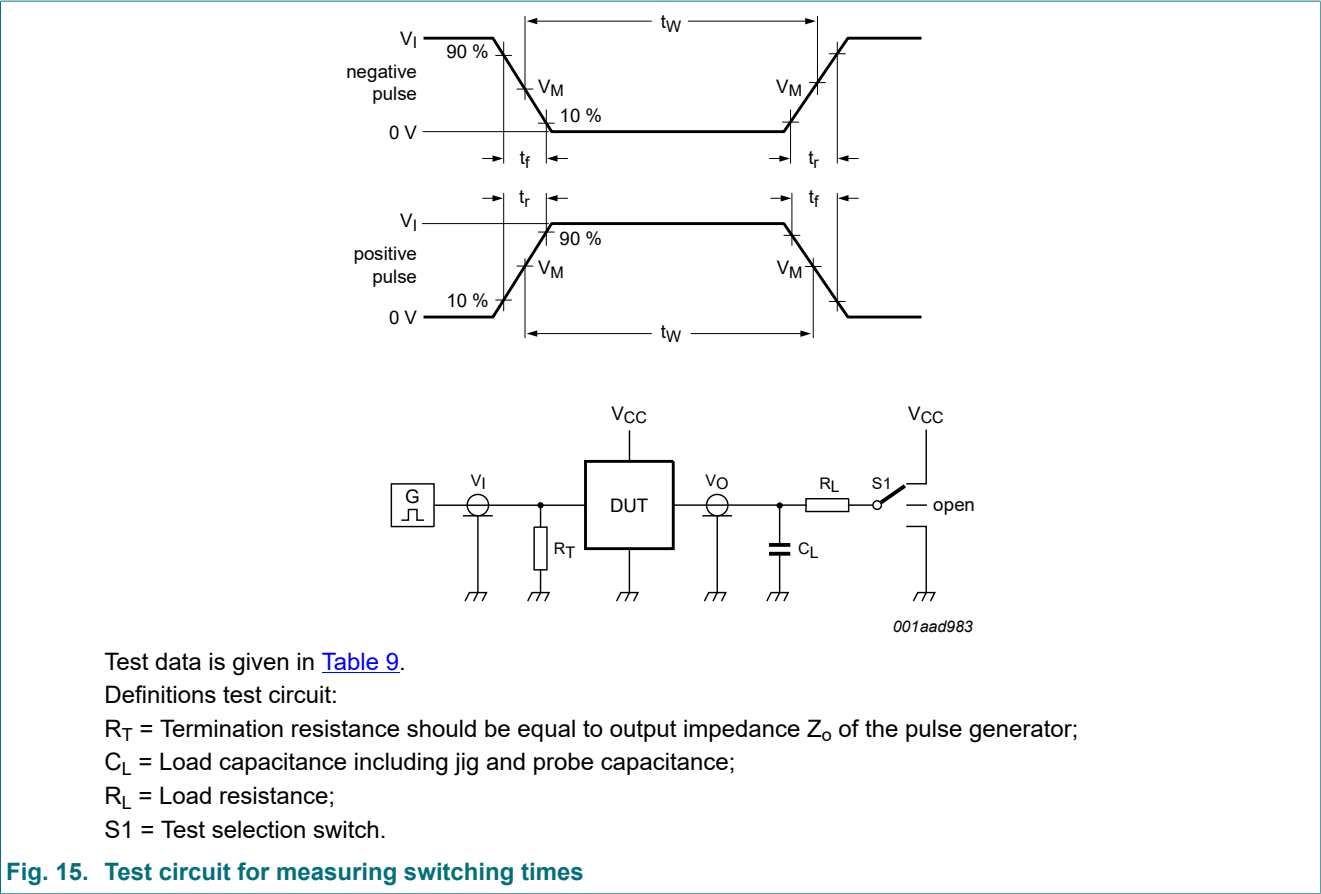


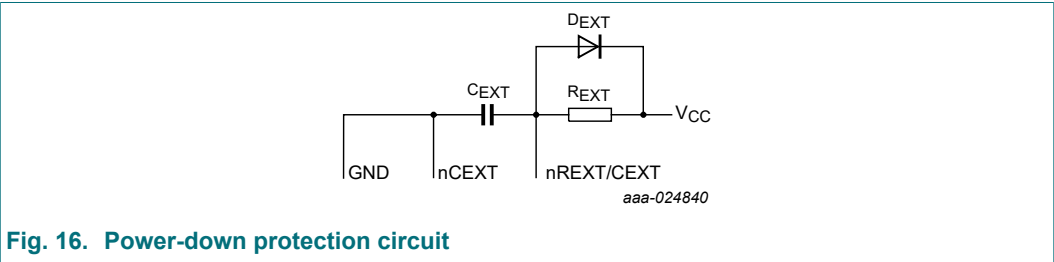
Table 9. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
3 V	6 ns	15 pF, 50 pF	1 kΩ	open

11. Application information

11.1. Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in [Fig. 16](#).



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

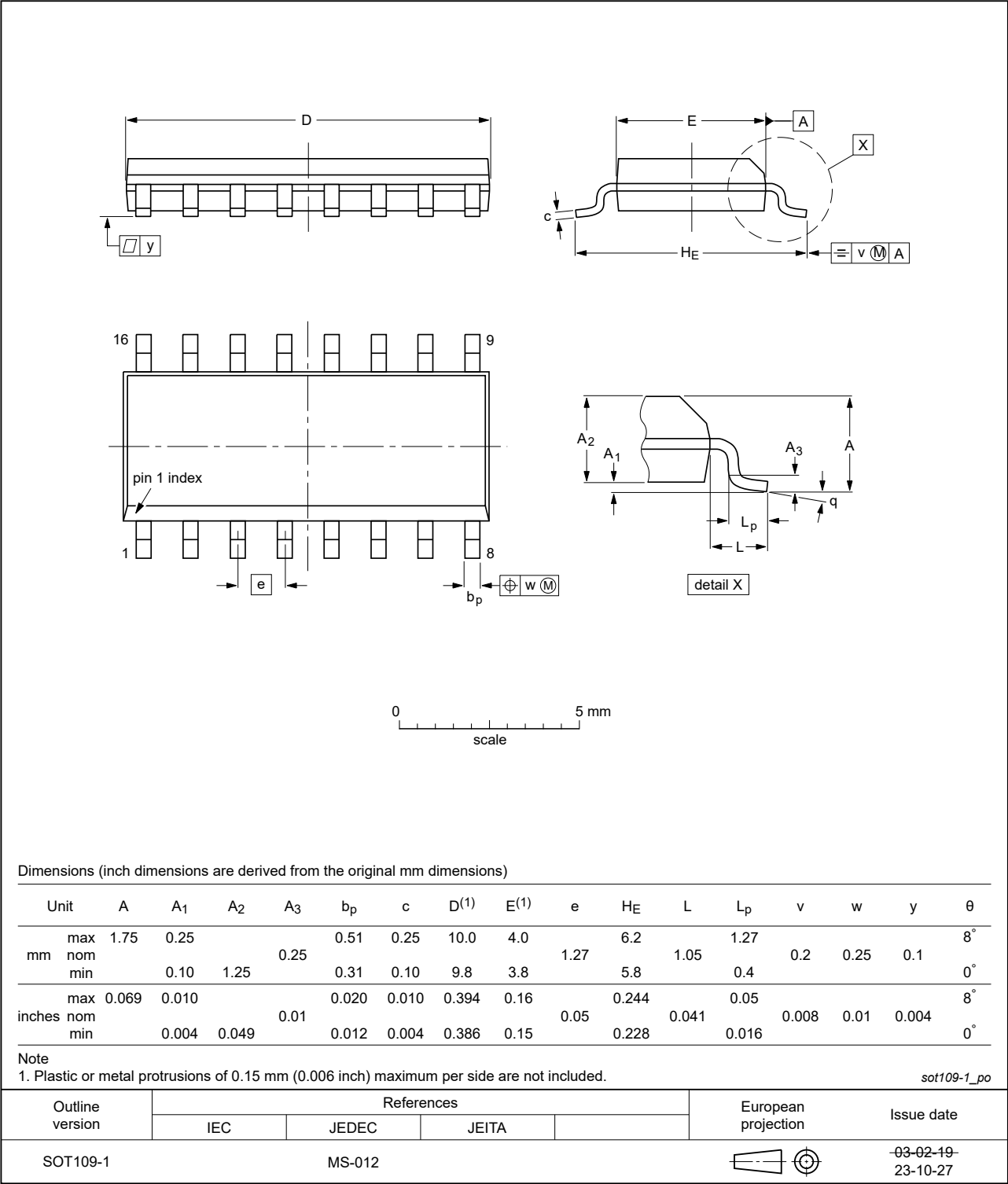


Fig. 17. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Abbreviation
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCT221 v.4	20240404	Product data sheet	-	74HC_HCT221 v.3
Modifications:	• Fig. 17: Aligned SO package outline drawing to JEDEC MS-012. • Section 2: ESD specification updated according to the latest JEDEC standard. • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 4: Derating values for P_{tot} total power dissipation updated.			
74HCT221 v.3	20161026	Product data sheet	-	74HC_HCT221 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC221N, 74HC221D, 74HC221DB and 74HCT221N removed.			
74HC_HCT221 v.2	19901201	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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