

74LVC373A-Q100

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Rev. 4 — 28 August 2023

Product data sheet

1. General description

The 74LVC373A-Q100 is an octal D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable (\overline{OE}) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- High-impedance outputs when $V_{CC} = 0$ V
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC373AD-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC373APW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC373ABQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

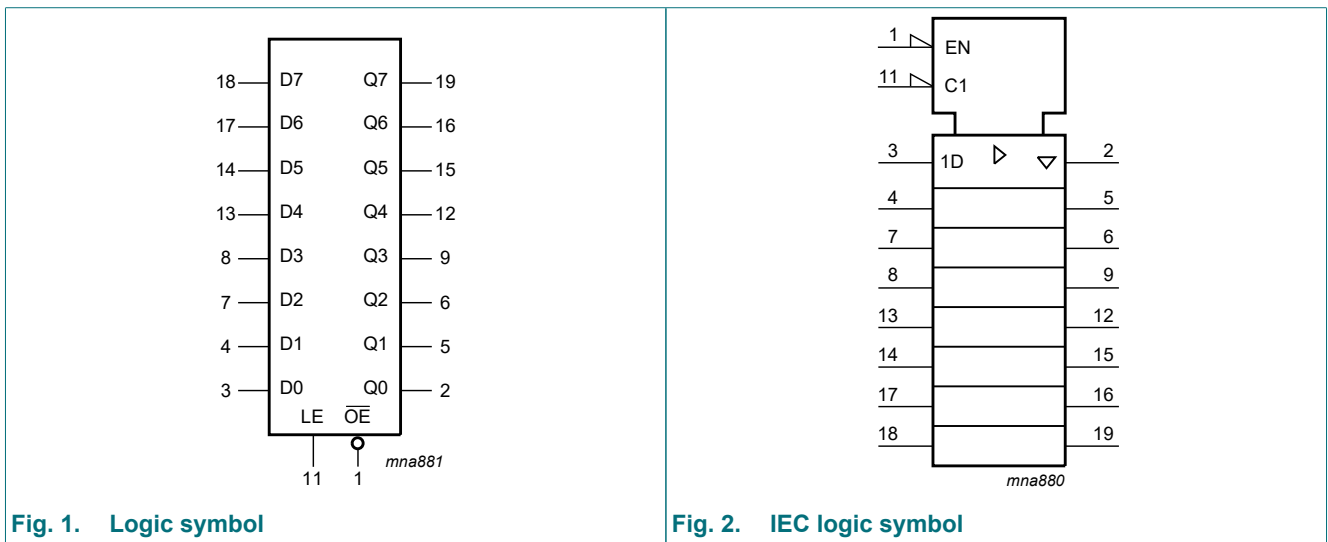


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

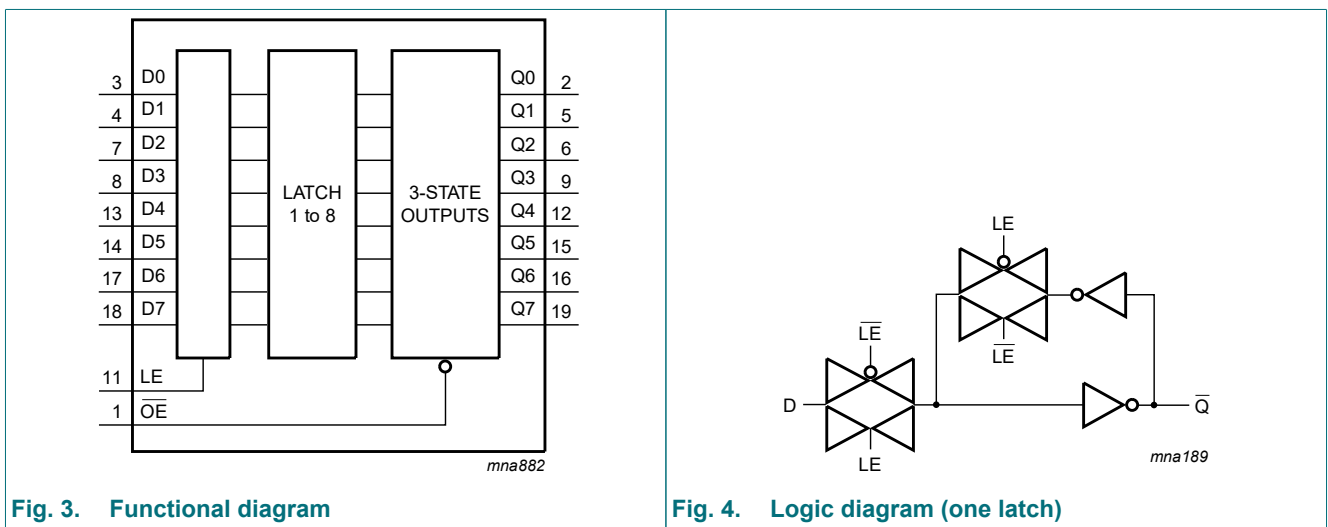
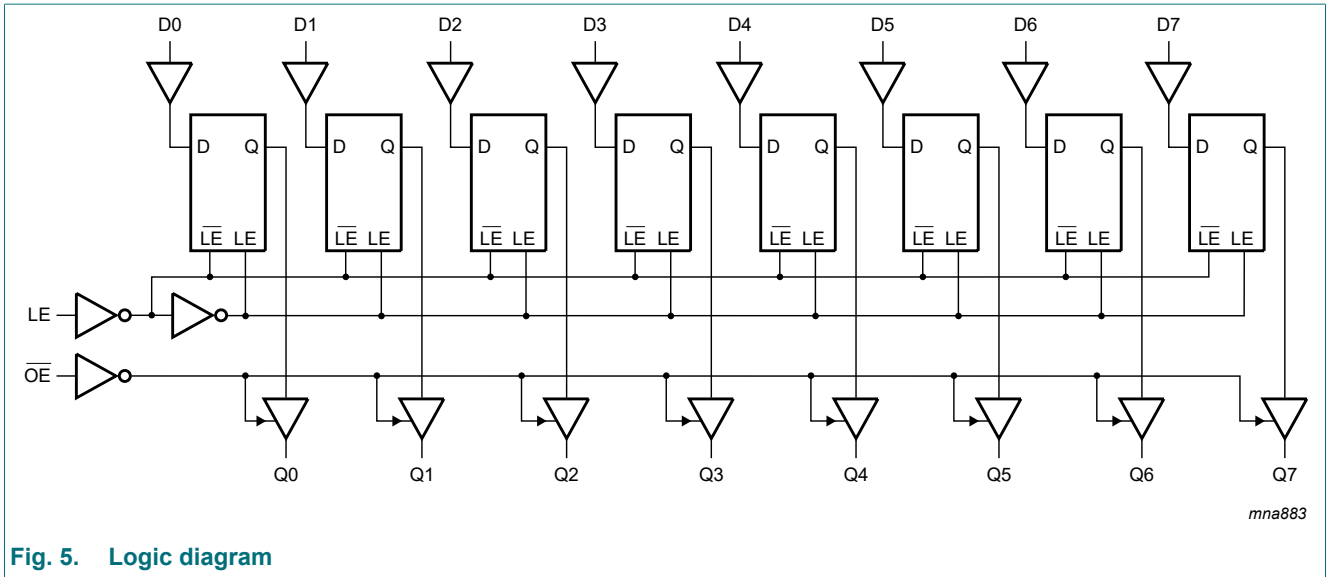


Fig. 3. Functional diagram

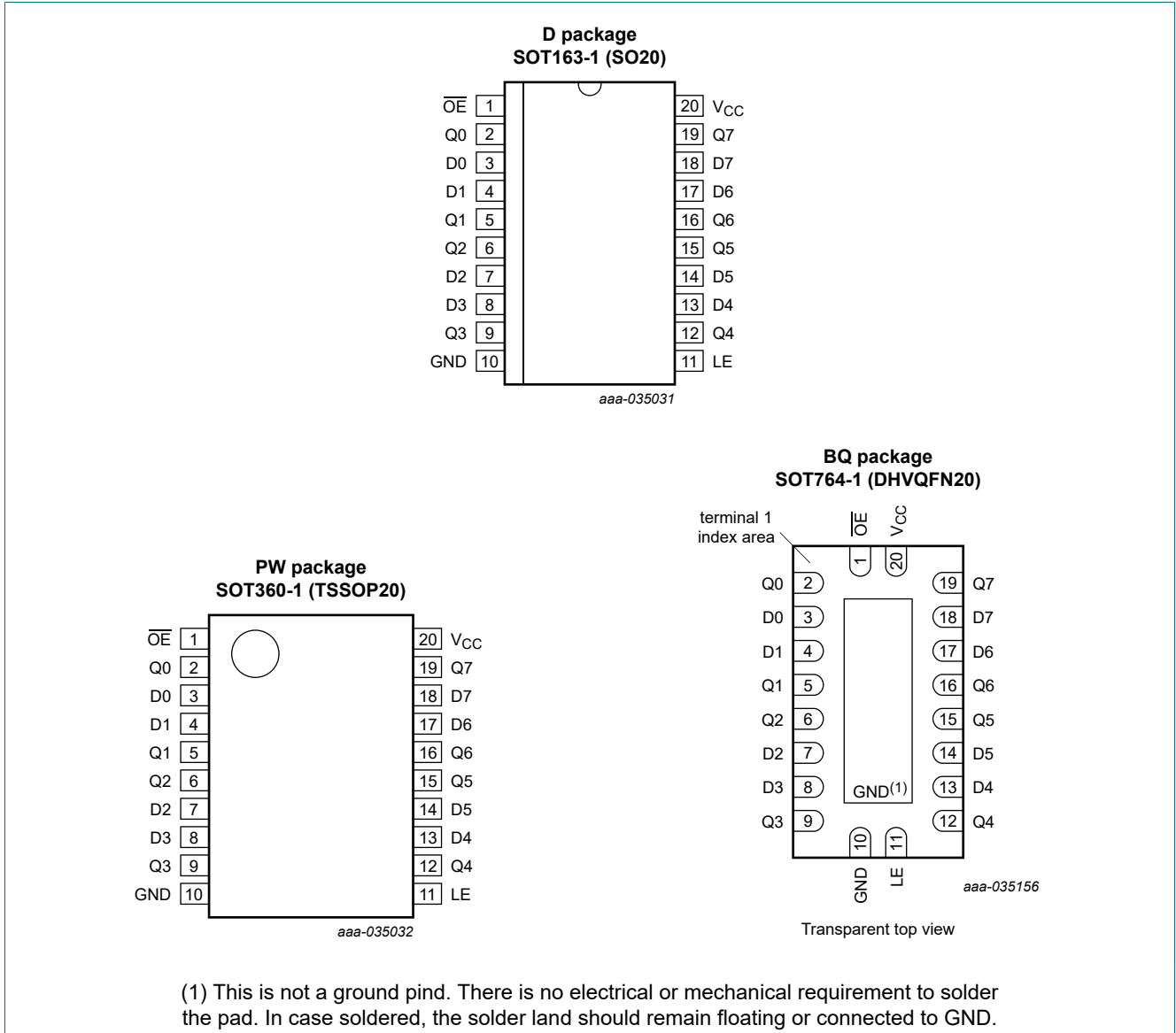
Fig. 4. Logic diagram (one latch)

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	output enable input (active LOW)
LE	11	latch enable input (active HIGH)
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	latch output
GND	10	ground (0 V)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table

*H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = High-impedance OFF-state.*

Operating modes	Input			Internal latch	Output
	OE	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	± 50	mA
V_O	output voltage	HIGH or LOW-state [2]	-0.5	$V_{CC} + 0.5$	V
		3-state [2]	-0.5	+6.5	V
I_O	output current	$V_O = 0 \text{ V to } V_{CC}$	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C to } +125 \text{ °C}$ [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.

For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

For SOT764-1 (DHFQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	HIGH or LOW-state	0	-	V _{CC}	V
		3-state	0	-	5.5	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V		
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND;	-	±0.1	±5	-	±20	μA

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I_{OFF}	power-off leakage supply	$V_{CC} = 0\text{ V}$; V_I or $V_O = 5.5\text{ V}$	-	± 0.1	± 10	-	± 20	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 2.7\text{ V}$ to 3.6 V ; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$	-	5	500	-	5000	μA
C_I	input capacitance	$V_{CC} = 0\text{ V}$ to 3.6 V ; $V_I = \text{GND}$ to V_{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ (unless stated otherwise) and $T_{amb} = 25\text{ °C}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 10.

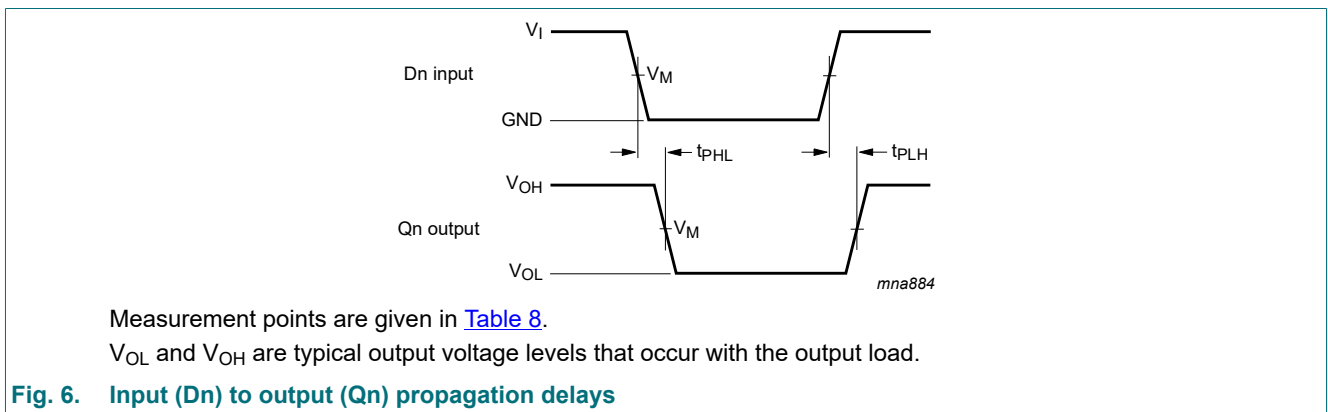
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	Dn to Qn; see Fig. 6 [2]						
		$V_{CC} = 1.2\text{ V}$	-	14	-	-	-	ns
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	1.5	6.5	15.8	1.5	18.2	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.0	3.4	8.2	1.0	9.4	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.4	7.8	1.5	10.0	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.5	2.9	6.8	1.5	8.5	ns
		LE to Qn; see Fig. 7 [2]						
		$V_{CC} = 1.2\text{ V}$	-	16	-	-	-	ns
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	2.2	7.3	16.8	2.2	19.3	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.5	3.9	8.6	1.5	10.0	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.5	8.2	1.5	10.5	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.5	3.3	7.2	1.5	9.0	ns
t_{en}	enable time	\overline{OE} to Qn; see Fig. 8 [2]						
		$V_{CC} = 1.2\text{ V}$	-	17	-	-	-	ns
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	1.5	6.8	17.6	1.5	20.3	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.5	3.8	9.7	1.5	11.2	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.8	8.7	1.5	11.0	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.5	3.1	7.7	1.5	10.0	ns
t_{dis}	disable time	\overline{OE} to Qn; see Fig. 8 [2]						
		$V_{CC} = 1.2\text{ V}$	-	8.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	2.3	4.3	10.3	2.3	11.9	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.0	2.4	5.8	1.0	6.8	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.2	7.1	1.5	9.0	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.5	3.0	6.1	1.5	8.0	ns

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

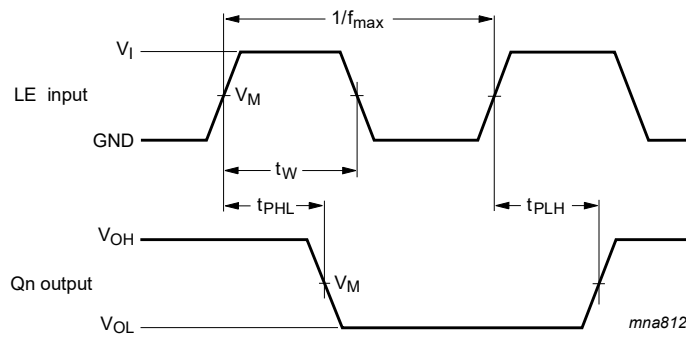
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _w	pulse width	LE HIGH; see Fig. 7						
		V _{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V _{CC} = 2.7 V	3.0	-	-	3.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	3.0	1.5	-	3.0	-	ns
t _{su}	set-up time	Dn to LE; see Fig. 9						
		V _{CC} = 1.65 V to 1.95 V	4.0	-	-	4.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	3.0	-	-	3.0	-	ns
		V _{CC} = 2.7 V	2.0	-	-	2.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	0.0	-	2.0	-	ns
t _h	hold time	Dn to LE; see Fig. 9						
		V _{CC} = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns
		V _{CC} = 2.7 V	1.5	-	-	1.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	0.3	-	1.5	-	ns
t _{sk(0)}	output skew time	V _{CC} = 3.0 V to 3.6 V [3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per latch; V _I = GND to V _{CC} [4]						
		V _{CC} = 1.65 V to 1.95 V	-	16.6	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	19.2	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	21.6	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

10.1. Waveforms and test circuit



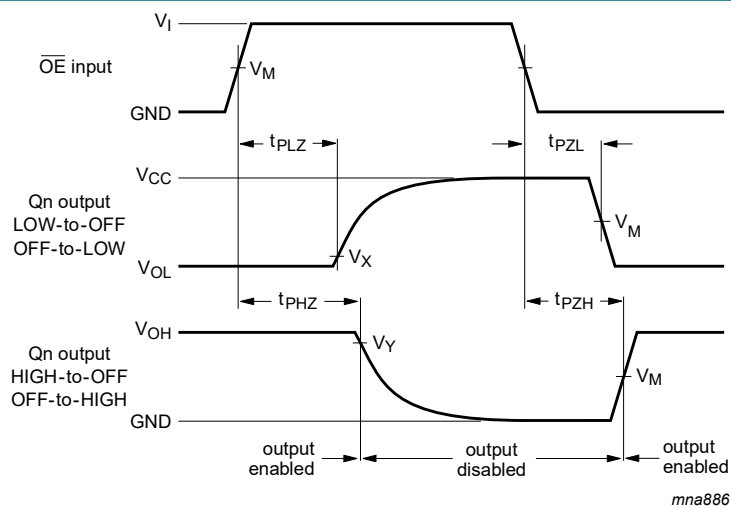
Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

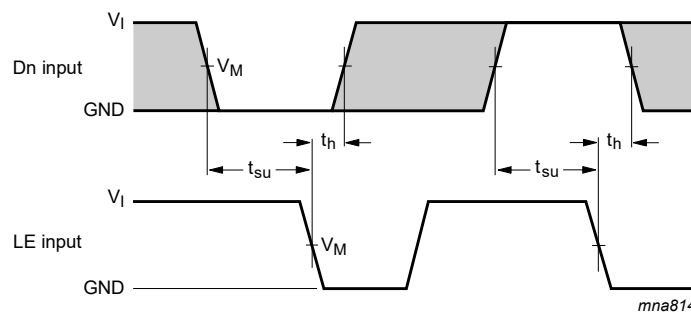
Fig. 7. Latch Enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. 3-state enable and disable times



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Data set-up and hold times for the Dn input to the LE input

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Table 8. Measurement points

Supply voltage	Input		Output		
V _{CC}	V _I	V _M	V _M	V _X	V _Y
1.2 V	V _{CC}	0.5 x V _{CC}	0.5 x V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
1.65 V to 1.95 V	V _{CC}	0.5 x V _{CC}	0.5 x V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.3 V to 2.7 V	V _{CC}	0.5 x V _{CC}	0.5 x V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V

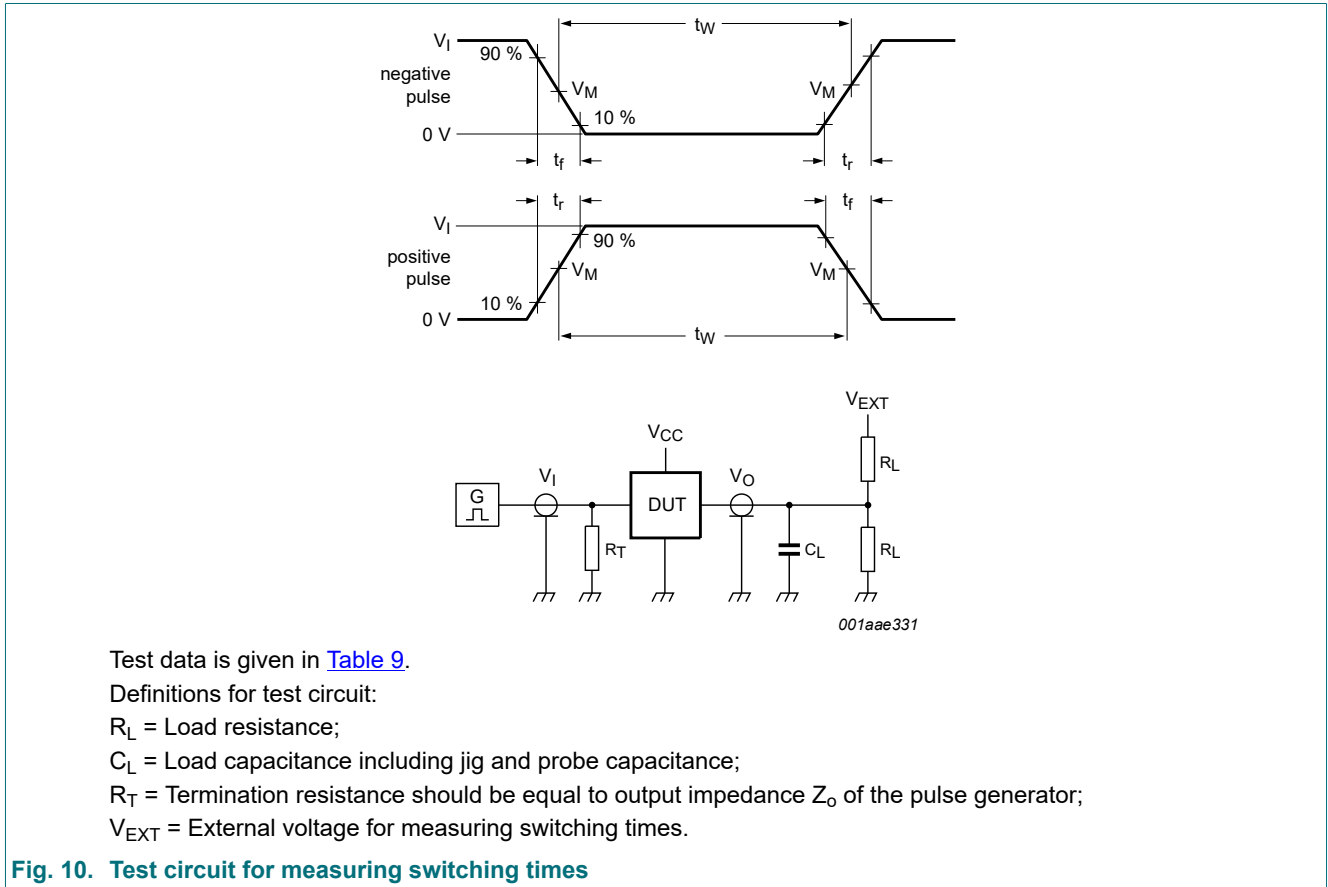


Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 x V _{CC}	GND
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 x V _{CC}	GND
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	2 x V _{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 x V _{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 x V _{CC}	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

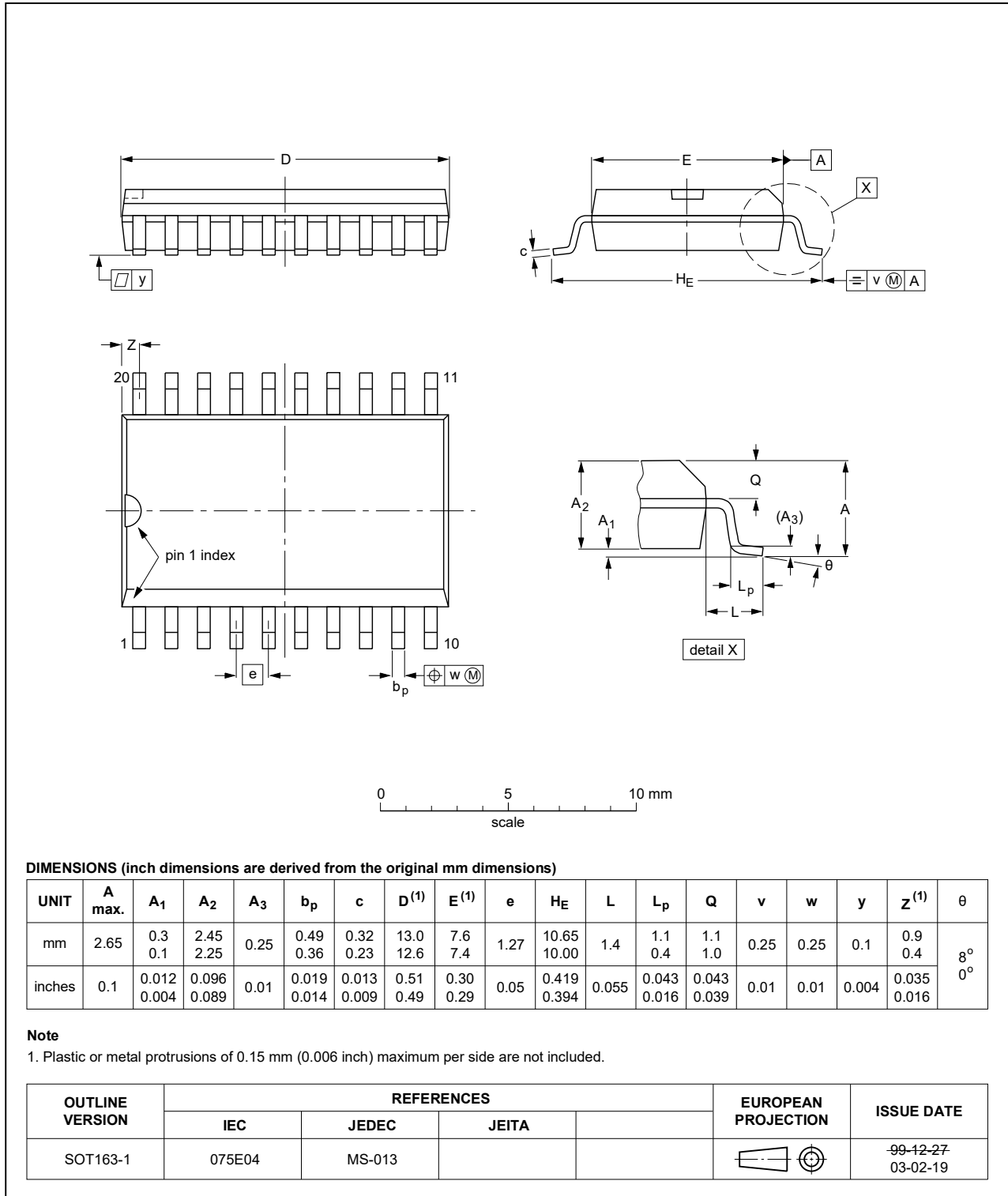


Fig. 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

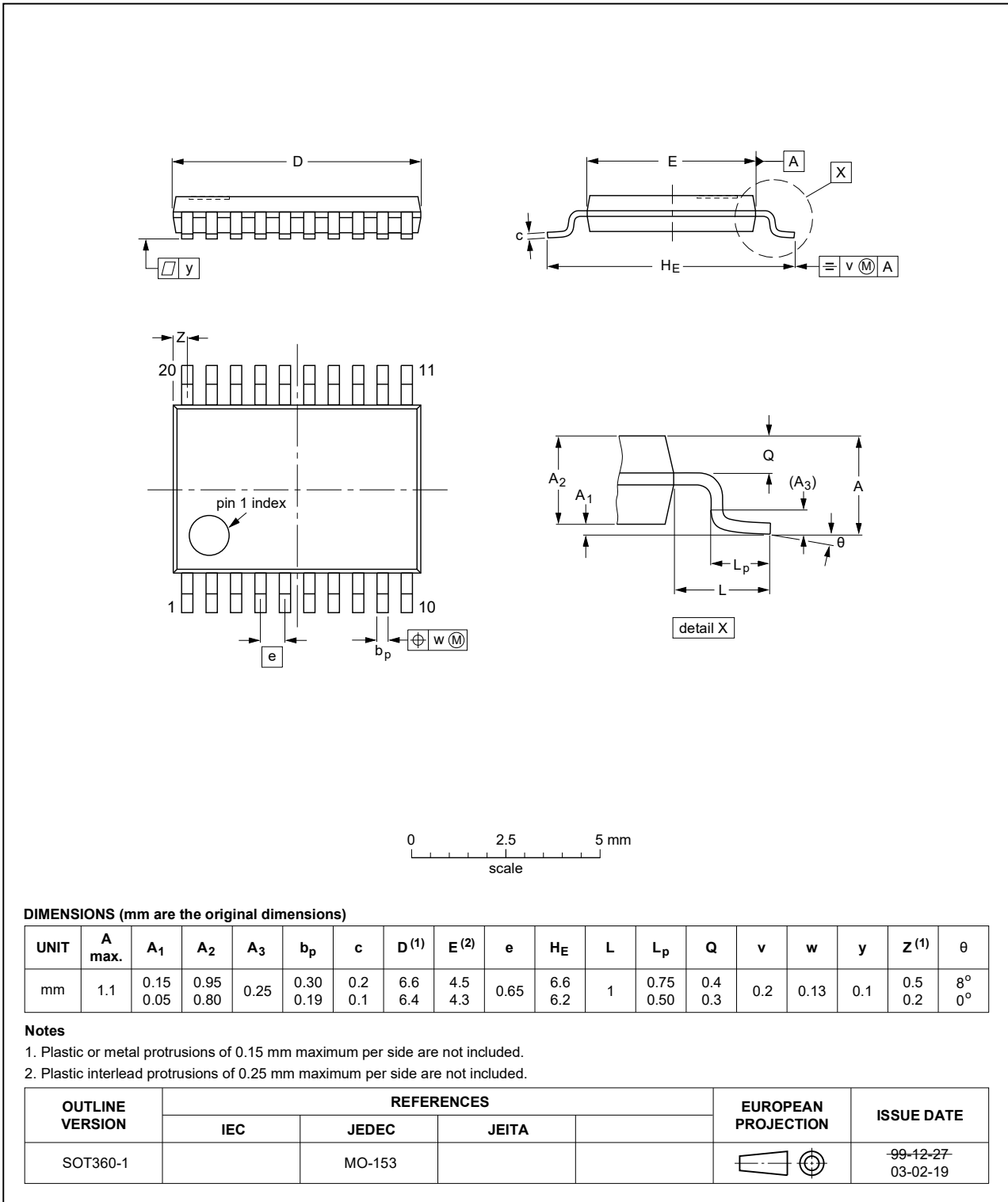


Fig. 12. Package outline SOT360-1 (TSSOP20)

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig. 13. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC373A_Q100 v.4	20230828	Product data sheet	-	74LVC373A_Q100 v.3
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVC373A_Q100 v.3	20210304	Product data sheet	-	74LVC373A_Q100 v.2
Modifications:	<ul style="list-style-type: none"> • Type number 74LVC373ADB-Q100 (SOT339-1 / SSOP20) removed. • Section 1 updated. • Fig. 7 and Fig. 9 corrected. 			
74LVC373A_Q100 v.2	20200824	Product data sheet	-	74LVC373A_Q100 v.1
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation have been updated. • Package outline drawing of SOT764-1 (Fig. 13) updated. 			
74LVC373A_Q100 v.1	20130417	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

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