BUK7J2R4-80M

N-channel 80 V, 2.4 mOhm, Standard level MOSFET in LFPAK56E

4 April 2024 **Preliminary data sheet**

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 14 low ohmic split-gate technology, for ultra-low R_{DSon} capability, housed in a LFPAK56E package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 14 split-gate technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
  - Fast and efficient switching with optimal damping and low spiking
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joints
- LFPAK copper clip technology:
  - Improved reliability, with reduced R_{th}, R_{DSon} and package inductance
  - Increases maximum current capability and improved current spreading

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motor, lighting and solenoid control
- Ultra high-performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	80	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	231	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	294	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		1.3	1.9	2.4	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; Fig. 13; Fig. 14		42.5	85	127	nC

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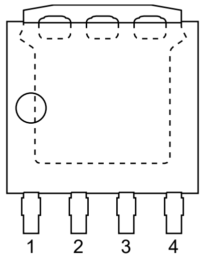
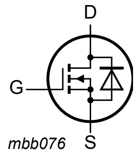
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56E; Power-SO8 (SOT1023)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7J2R4-80M	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56E); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7J2R4-80M	72M480J

8. Limiting values

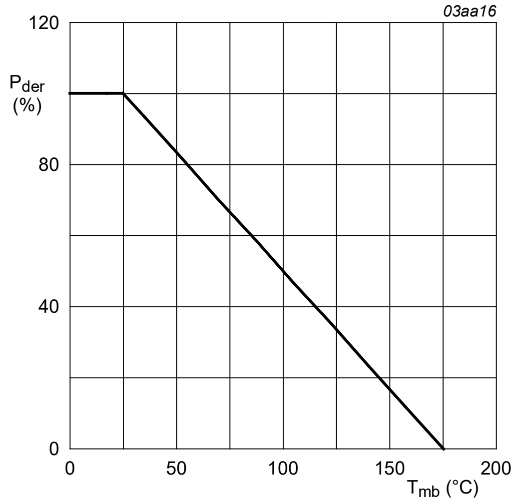
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	294	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	231	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	163	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	923	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	231	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	923	A

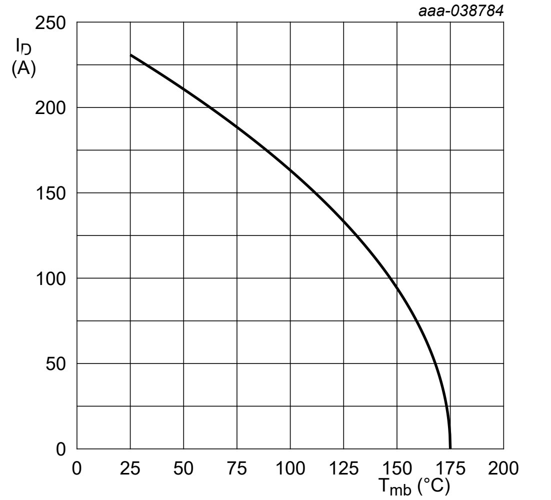
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 58 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[1] [2] [3]	-	383	mJ

[1] Protected by 100% test.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.



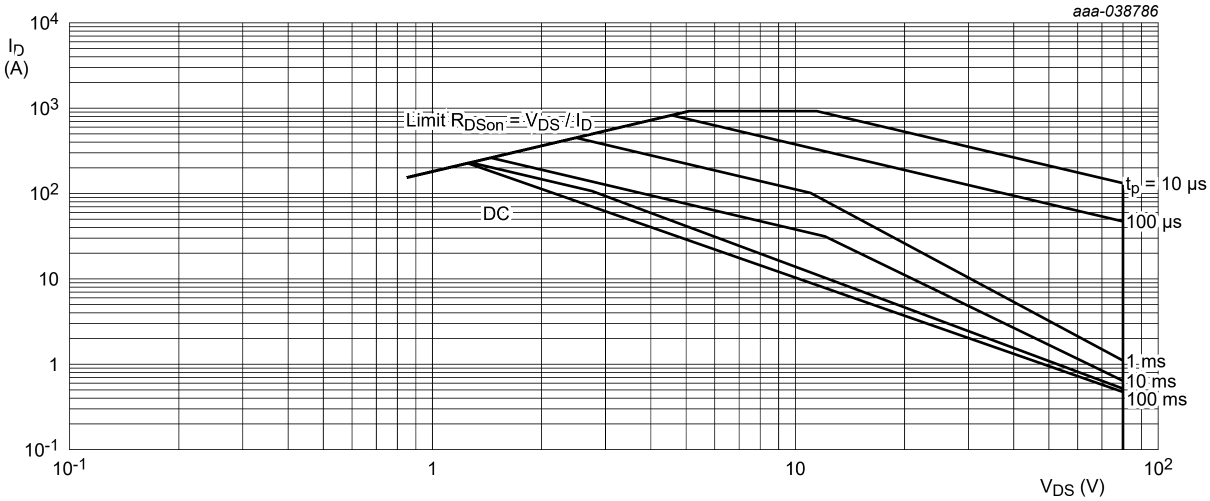
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



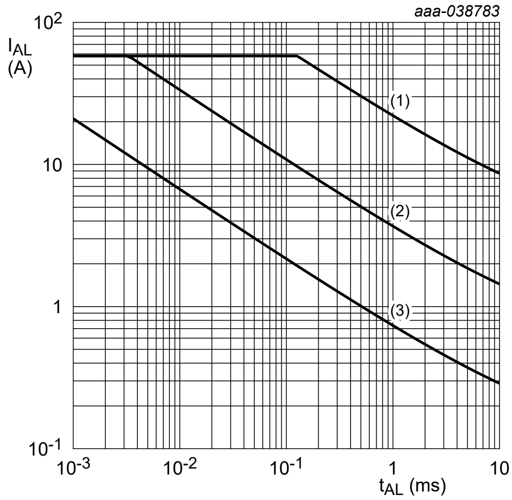
V_{GS} ≥ 10 V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.45	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	24	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.

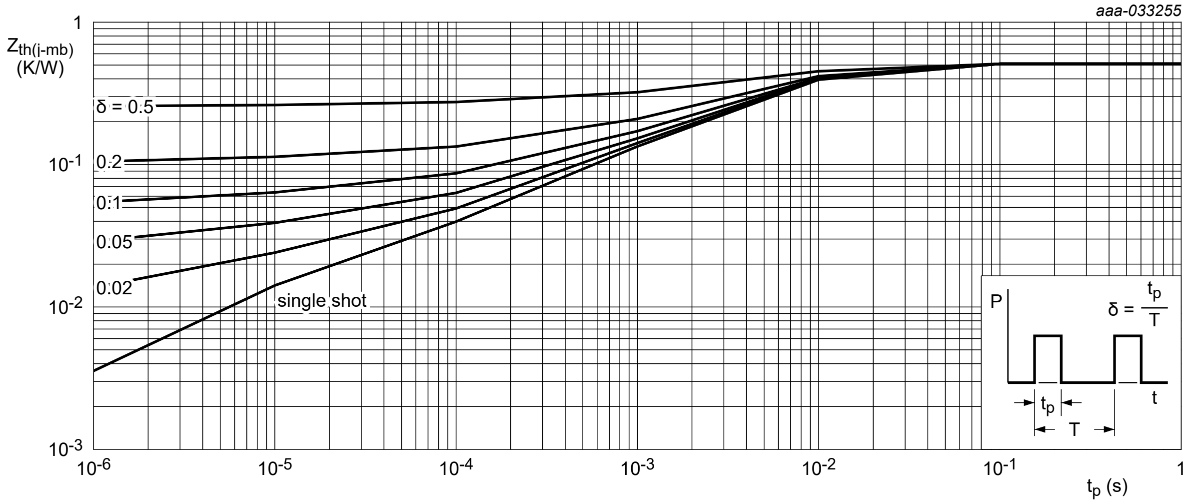


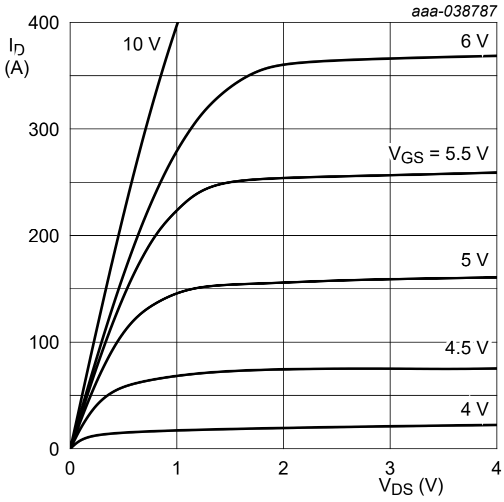
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

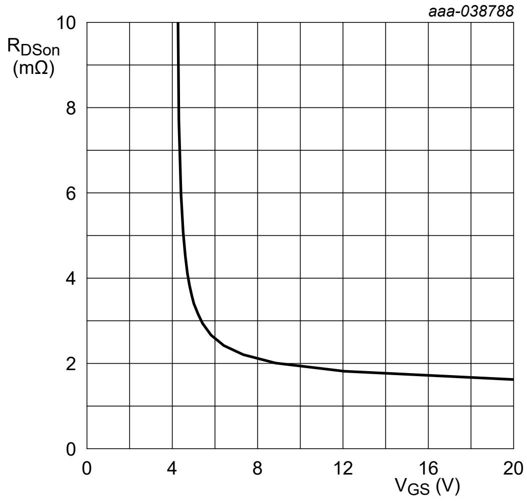
Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	80	87	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C	-	85	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	72	84	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9	2	3	4	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 10	1	1.9	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 10	-	3.3	4.6	V
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C	-	0.003	1	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 °C	-	3	100	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 175 °C	-	76	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11	1.3	1.9	2.4	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 12	2.2	3.1	4.3	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 12	2.5	3.4	4.9	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 12	2.8	4.4	5.5	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C	0.4	0.8	1.6	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; Fig. 13; Fig. 14	42.5	85	127	nC
Q_{GS}	gate-source charge		8.8	22	35	nC
Q_{GD}	gate-drain charge		5.8	16.5	38	nC
C_{iss}	input capacitance	V_{DS} = 40 V; V_{GS} = 0 V; f = 1 MHz; Fig. 15	3510	5850	8191	pF
C_{oss}	output capacitance		554	1385	2493	pF
C_{rss}	reverse transfer capacitance		4	44	102	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 40 V; R_L = 1.6 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω	-	19	-	ns
t_r	rise time		-	18	-	ns
$t_{d(off)}$	turn-off delay time		-	53	-	ns
t_f	fall time		-	29	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16	-	0.79	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V; Fig. 17	-	38	-	ns
Q_r	recovered charge		-	33	-	nC



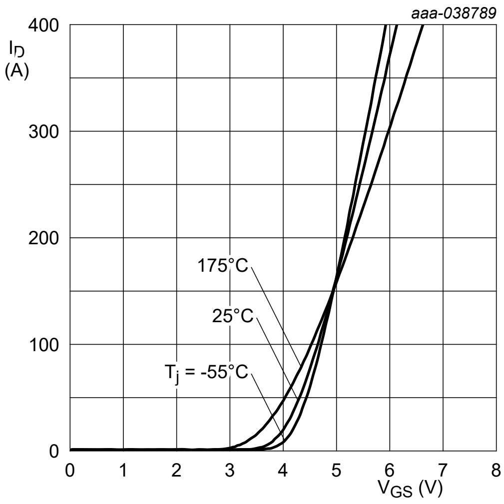
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



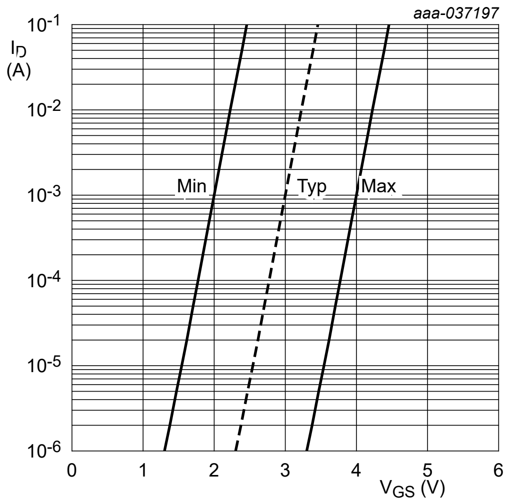
T_j = 25 °C; I_D = 25 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



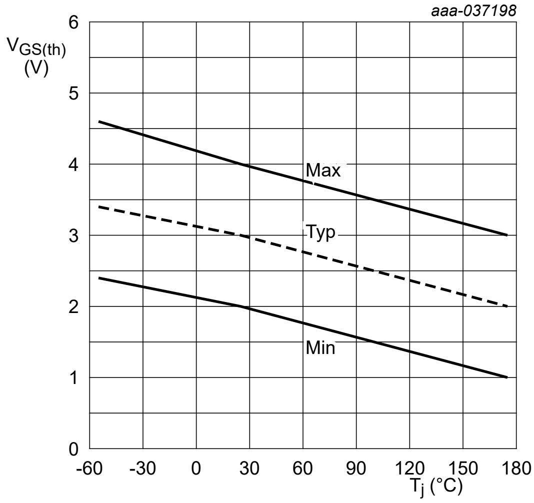
V_{DS} = 8 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



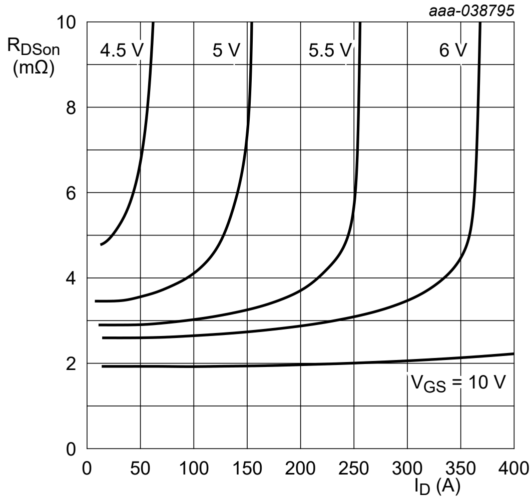
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage



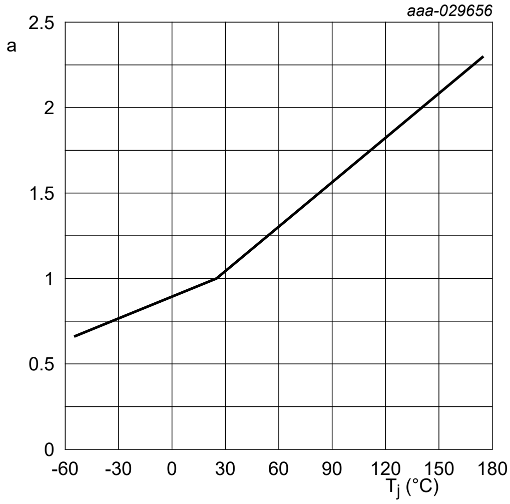
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 10. Gate-source threshold voltage as a function of junction temperature



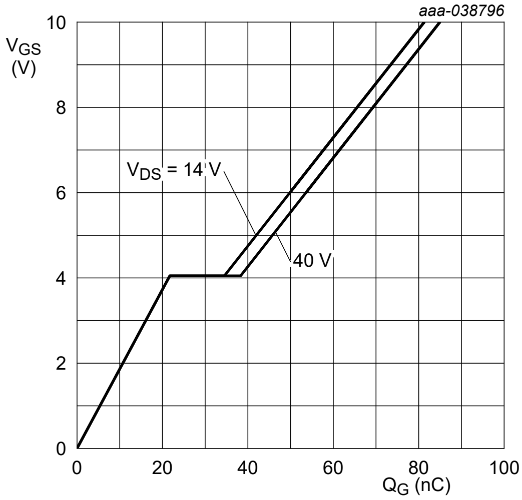
T_j = 25 °C

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}\ (25°C)}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 13. Gate-source voltage as a function of gate charge; typical values

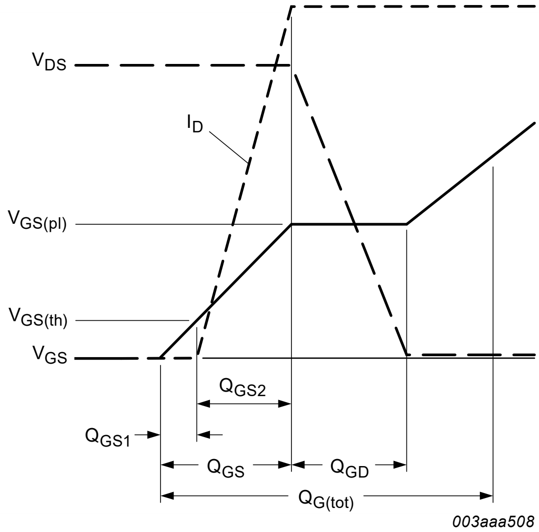
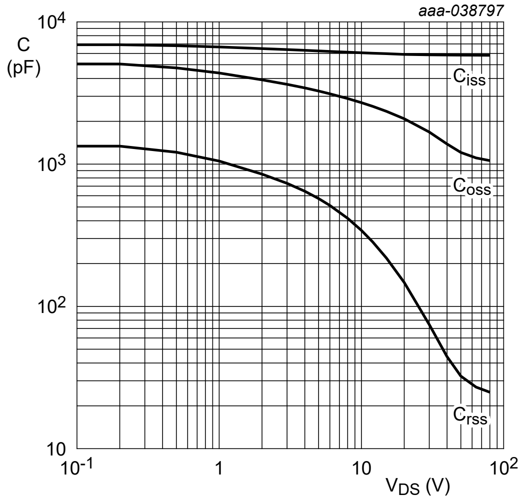
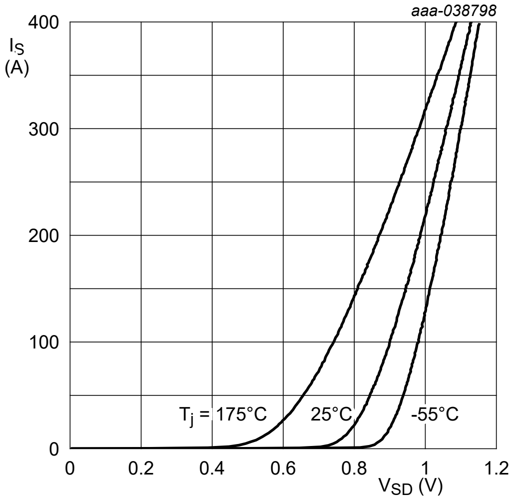


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

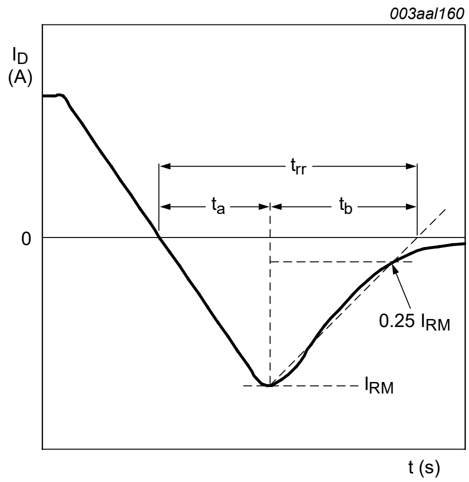
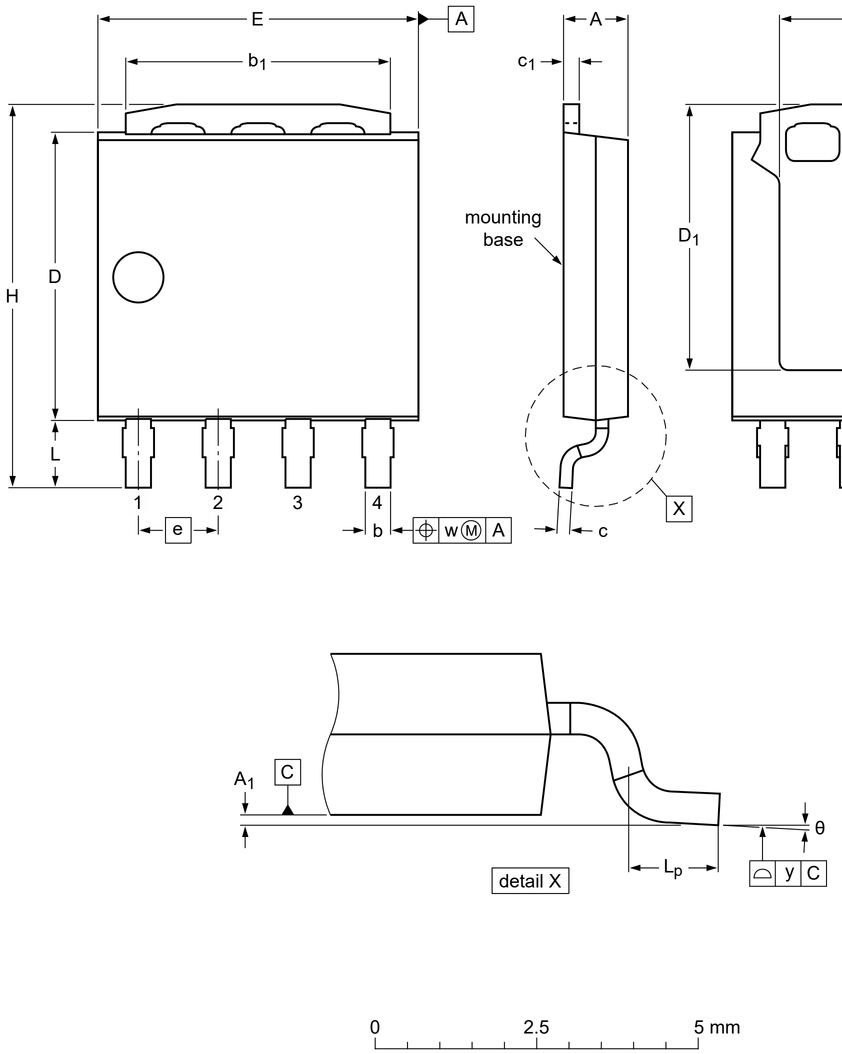


Fig. 17. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56E); 4 leads **SOT1023**



Dimensions

Unit		A	A1	b	b1	b2	c	c1	D(1)	D1(1)	E(1)	E1(1)	e	H	L	Lp	w	y	θ
mm	max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
	nom					0.85							1.27				0.25	0.1	
	min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

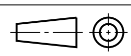
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1023						~~13-03-05~~ 17-07-31

Fig. 18. Package outline LFPAK56E; Power-SO8 (SOT1023)

12. Soldering

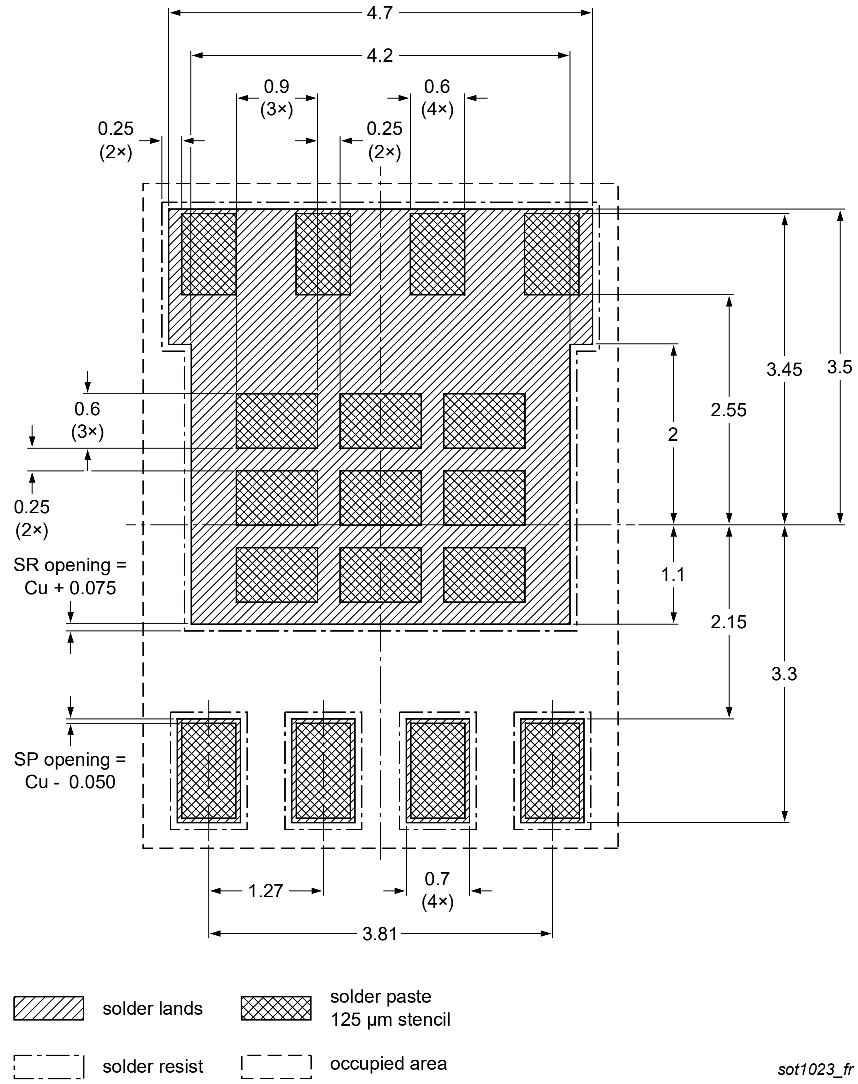


Fig. 19. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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