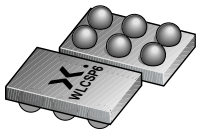

PMCM650CUNE

20 V, Common Drain N-channel Trench MOSFET

Rev. 1.0 — 8 November 2017 Product data sheet

1 Product profile

1.1 General description

N-channel enhancement mode common-drain dual Field-Effect Transistor (FET) in a 6 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

1.2 Features and benefits

- Common-drain type for bi-directional current flow
- Low threshold voltage
- Ultra small package: 0.98 × 1.48 × 0.35 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

1.3 Applications

- Loadswitch
- Battery Protection
- Battery Management

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SS}	source-source voltage	T_j = 25 °C	-	-	20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_S	source current	T_{amb} = 25 °C; V_{GS} = 4.5 V; t ≤ 5 s [1]	-	-	5.3	A
Static characteristics						
R_{SSon}	source-source on-state resistance	V_{GS} = 4.5 V; I_S = 3 A; T_j = 25 °C	-	40	52	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm^2.

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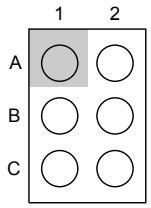
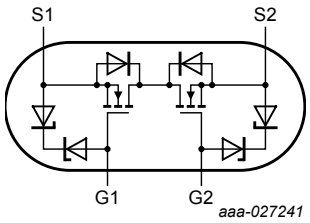
2 Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1	G1	gate 1	 Transparent top view	
A2	S1	source 1		
B1	S2	source 2		
B2	S1	source 1		
C1	S2	source 2		
C2	G2	gate 2		

3 Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCM650CUNE	WLCSP6	wafer level chip-size package; 6 bumps (3 x 2)	WLCSP6_3-2

4 Marking

Table 4. Marking codes

Type number	Marking code
PMCM650CUNE	AH

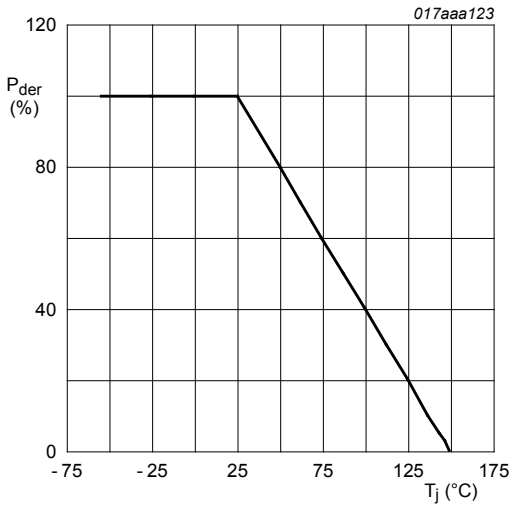
5 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

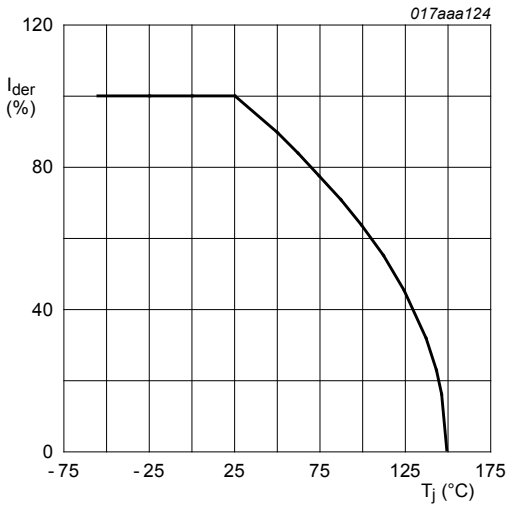
Symbol	Parameter	Conditions		Min	Max	Unit
V_{SS}	source-source voltage	T_j = 25 °C		-	20	V
V_{GS}	gate-source voltage	T_j = 25 °C		−8	8	V
I_S	source current	T_{amb} = 25 °C; V_{GS} = 4.5 V; t ≤ 5 s	[1]	-	5.3	A
		T_{amb} = 25 °C; V_{GS} = 4.5 V	[1]	-	4.1	A
		T_{amb} = 100 °C; V_{GS} = 4.5 V	[1]	-	2.6	A
I_{SM}	peak source current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	16	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	556	mW
		T_{amb} = 25 °C	[1]	-	1300	mW
		T_{sp} = 25 °C		-	12500	mW
T_j	junction temperature			−55	150	°C
T_{amb}	ambient temperature			−55	150	°C
T_{stg}	storage temperature			−65	150	°C
Source-Forward diode						
I_{FS}	source-forward current	T_{amb} = 25 °C	[1]	-	1.2	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm^2.
[2] Device mounted on an FR4 PCB, single-sided copper; tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\%$$

Figure 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_{SS}}{I_{SS(25\,°C)}} \times 100\%$$

Figure 2. Normalized continuous source-source current as a function of junction temperature

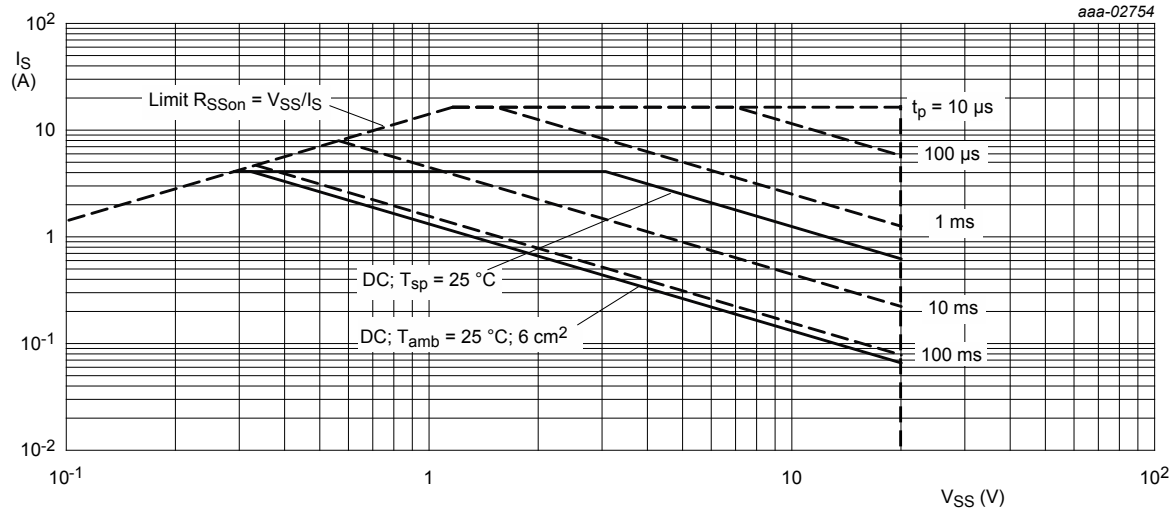


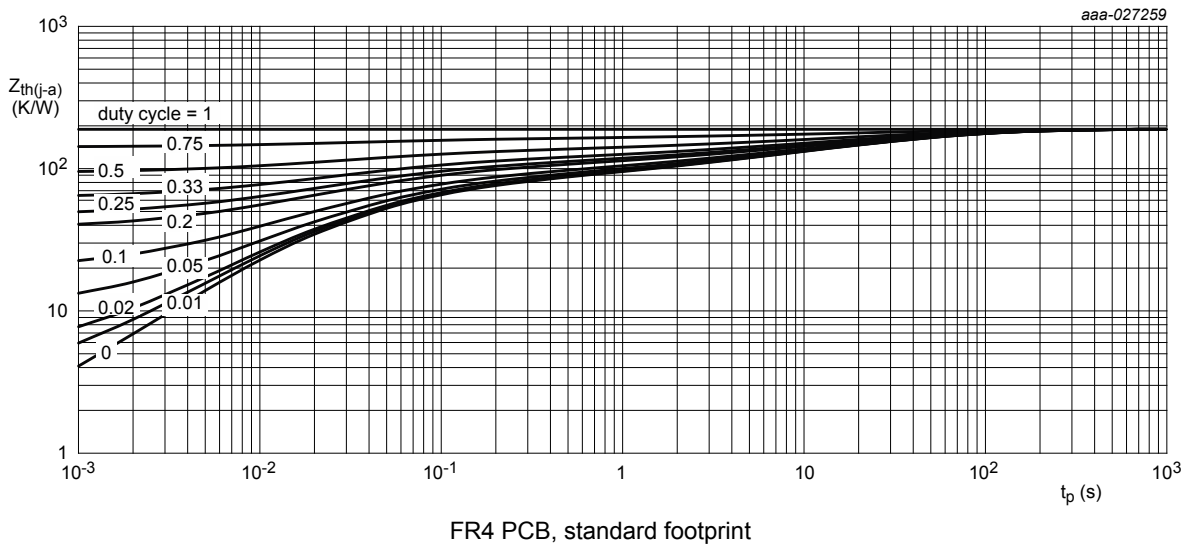
Figure 3. Safe operating area; junction to ambient; continuous and peak source currents as a function of source-source voltage

6 Thermal characteristics

Table 6. Thermal characteristics

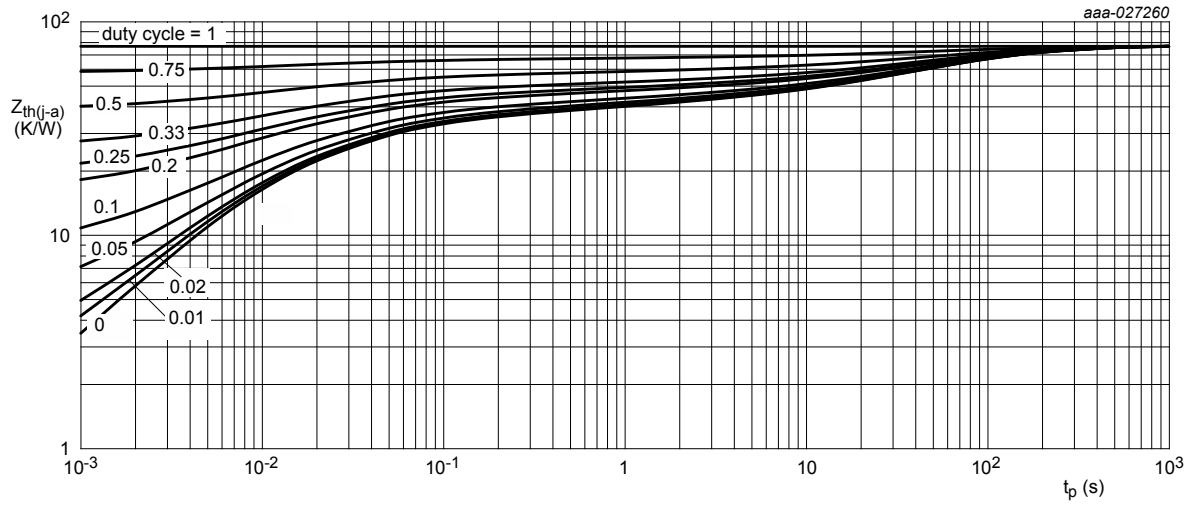
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	180	225	K/W
			[2]	-	65	85	K/W
			[3]	-	75	95	K/W
		in free air; t ≤ 5 s	[3]	-	45	55	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain, 4 layer, 1 cm^2.
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2.



FR4 PCB, standard footprint

Figure 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm^2

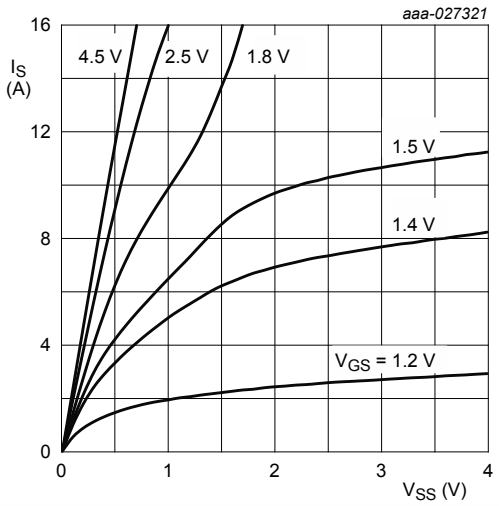
Figure 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7 Characteristics

Table 7. Characteristics

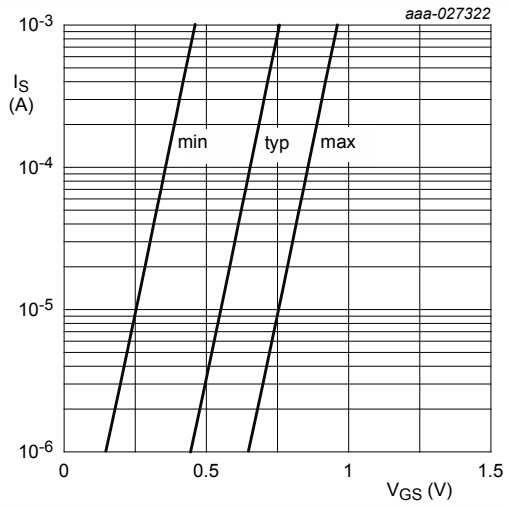
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristic							
$V_{(BR)SS}$	source-source breakdown voltage	I_S = 250 µA; V_{GS} = 0 V;		20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{SS} = V_{GS}		0.4	0.7	0.9	V
I_{SSS}	source leakage current	V_{GS} = 0 V; V_{SS} = 20 V		-	-	1	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{SS} = 0 V		-	-	10	µA
		V_{GS} = −8 V; V_{SS} = 0 V		-	-	−10	µA
		V_{GS} = 4.5 V; V_{SS} = 0 V		-	-	1	µA
		V_{GS} = −4.5 V; V_{SS} = 0 V		-	-	−1	µA
		V_{GS} = 2.5 V; V_{SS} = 0 V		-	-	200	nA
		V_{GS} = −2.5 V; V_{SS} = 0 V		-	-	−200	nA
R_{SSon}	source-source on-state resistance	V_{GS} = 4.5 V; I_S = 3 A; T_j = 25 °C		-	40	52	mΩ
		V_{GS} = 4.5 V; I_S = 3 A; T_j = 150 °C		-	55	71	mΩ
		V_{GS} = 2.5 V; I_S = 2 A; T_j = 25 °C		-	50	62	mΩ
		V_{GS} = 1.8 V; I_S = 1 A; T_j = 25 °C		-	63	95	mΩ
g_{fs}	forward transconductance	V_{GS} = 4.5 V; I_S = 3 A		-	22	-	S
R_G	gate resistance	f = 1 MHz		-	6.6	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{SS} = 10 V; I_S = 3 A; V_{GS} = 4.5 V		-	9	13	nC
Q_{GS}	gate-source charge			-	0.7	-	nC
Q_{GD}	gate-drain charge			-	2.9	-	nC
C_{iss}	input capacitance	V_{SS} = 10 V; f = 1 MHz; V_{GS} = 0 V		-	480	-	pF
C_{oss}	output capacitance			-	96	-	pF
C_{rss}	reverse transfer capacitance			-	96	-	pF
$t_{d(on)}$	turn-on delay time	V_{SS} = 10 V; I_S = 3 A; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω		-	6	-	ns
t_r	rise time			-	20	-	ns
$t_{d(off)}$	turn-off delay time			-	39	-	ns
t_f	fall time			-	15	-	ns
Source-Foward diode							
V_{FS}	source-forward voltage	V_{G1S1} = 0 V ; V_{G2S2} = 4.5 V; I_S = 1.2 A		-	0.7	1.2	V



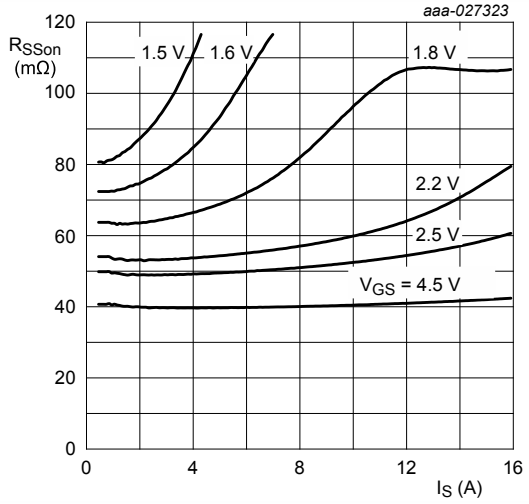
T_j = 25 °C

Figure 6. Output characteristics: source current as a function of source-source voltage; typical values



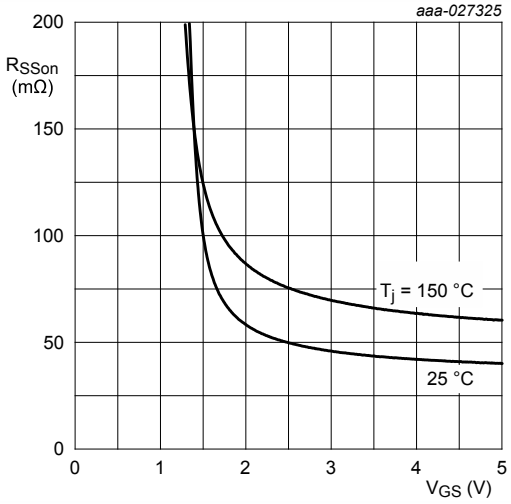
V_{SS} = 5 V; T_j = 25 °C

Figure 7. Sub-threshold source current as a function of gate-source voltage



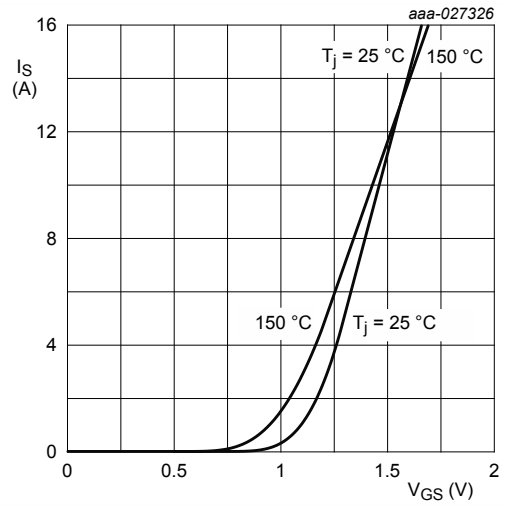
T_j = 25 °C

Figure 8. Source-source on-state resistance as a function of source current; typical values



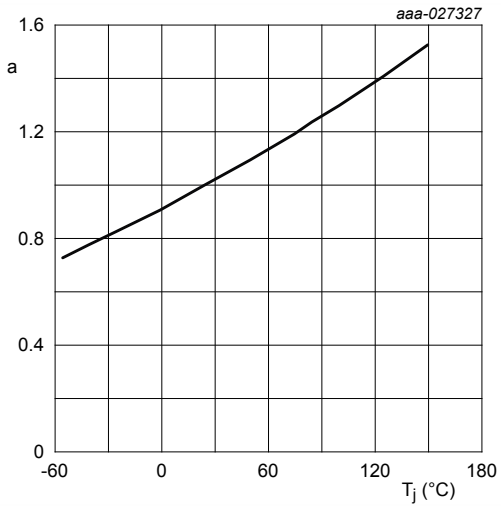
I_S = 3 A

Figure 9. Source-source on-state resistance as a function of gate-source voltage; typical values



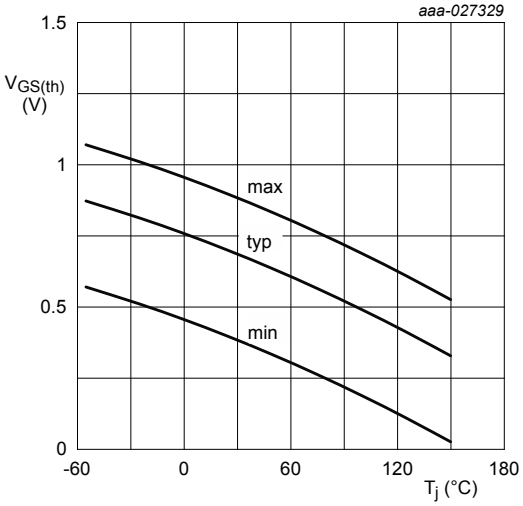
$V_{SS} > I_S \times R_{SSon}$

Figure 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



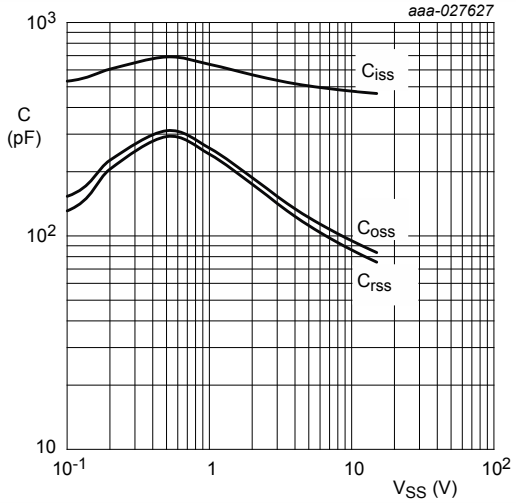
$$a = \frac{R_{SSon}}{R_{SSon(25\,°C)}} \times 100\%$$

Figure 11. Normalized source-source on-state resistance as a function of junction temperature; typical values



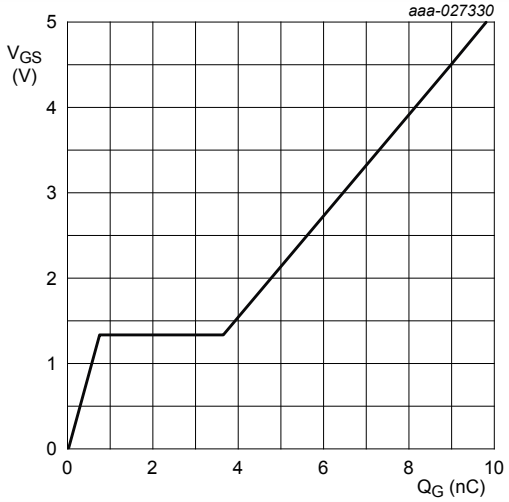
I_S = 250 µA; $V_{SS} = V_{GS}$

Figure 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Figure 13. Input, output and reverse transfer capacitances as a function of source-source voltage; typical values



V_{SS} = 10 V; I_S = 3 A; T_{amb} = 25 °C

Figure 14. Gate-source voltage as a function of gate charge; typical values

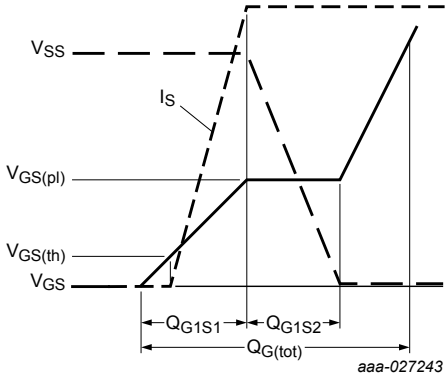
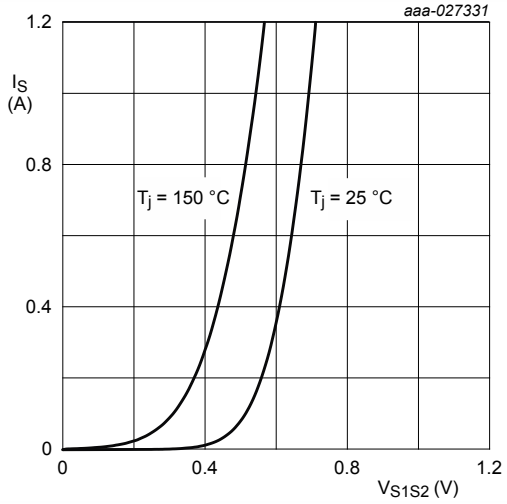


Figure 15. Common Drain MOSFET gate charge definitions



V_{G1S1} = 0 V; V_{G2S2} = 4.5 V

Figure 16. Source current as a function of source-source voltage; typical values

8 Test information

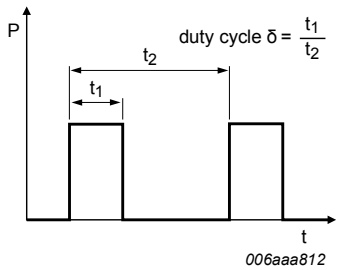


Figure 17. Duty cycle definition

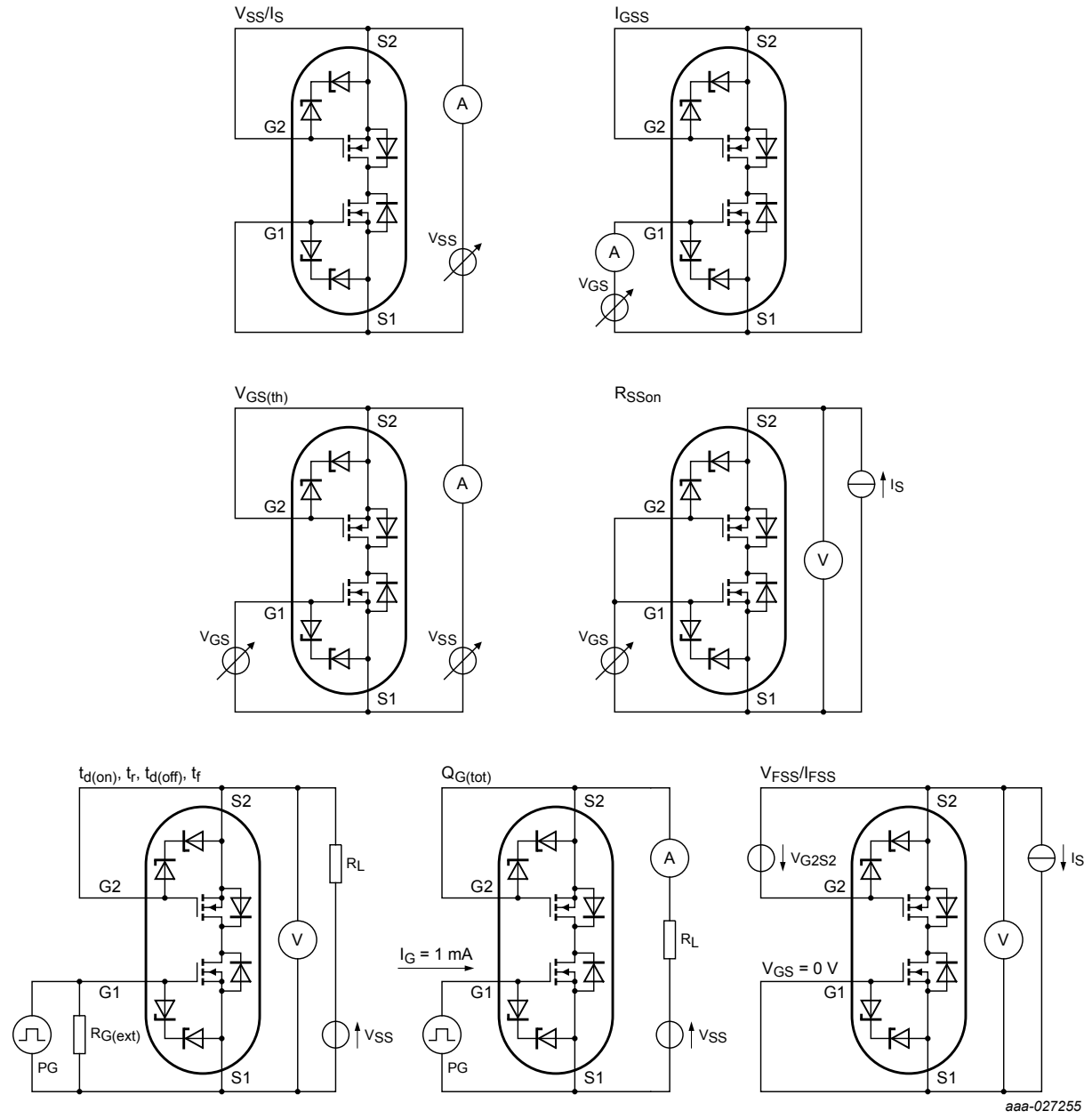
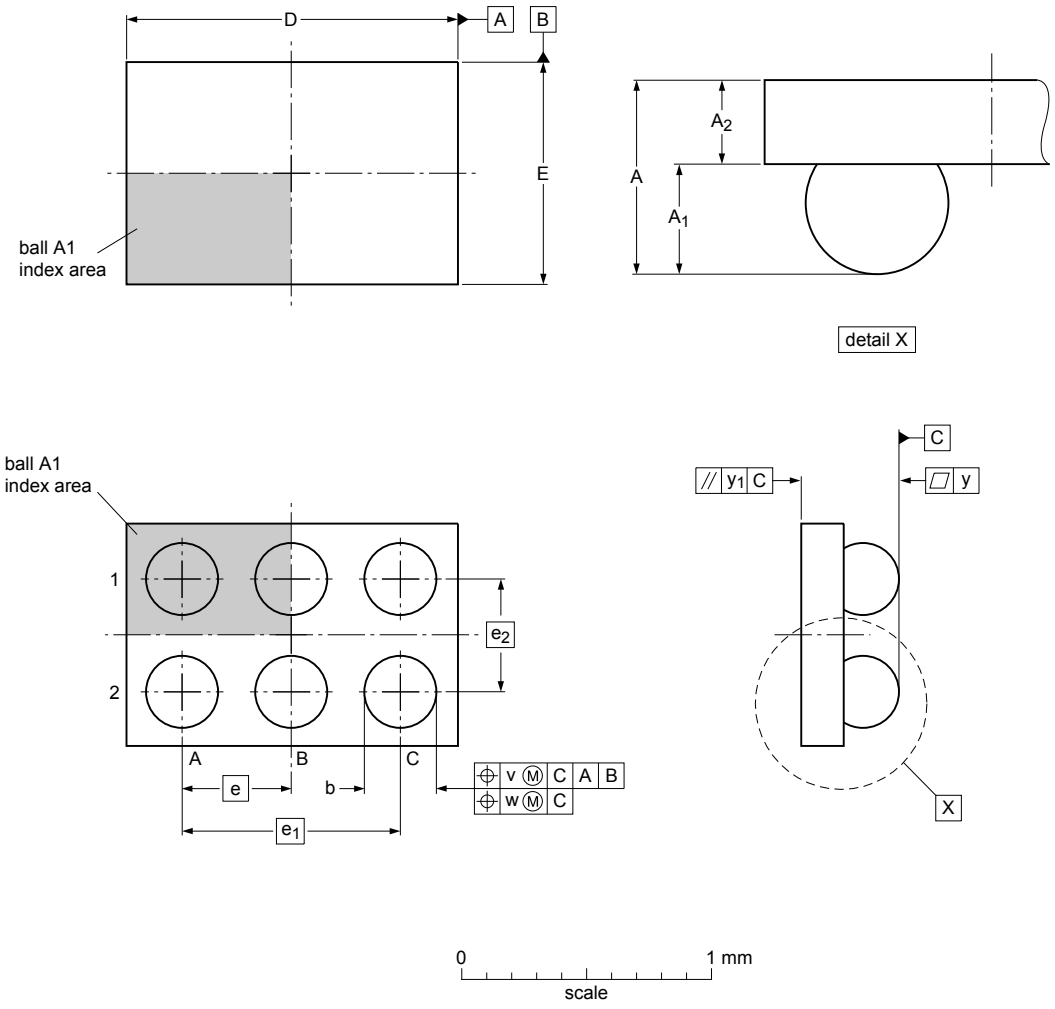


Figure 18. Test circuits

9 Package outline

WLCSP6: wafer level chip-size package; 6 bumps (3 x 2) **WLCSP6_3-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.375	0.215	0.160	0.275	1.51	1.01						
	nom	0.345	0.200	0.145	0.260	1.48	0.98	0.50	1.00	0.50	0.15	0.05	0.05
	min	0.315	0.185	0.130	0.245	1.45	0.95						

Note
Device back is metal coated on Drain potential.

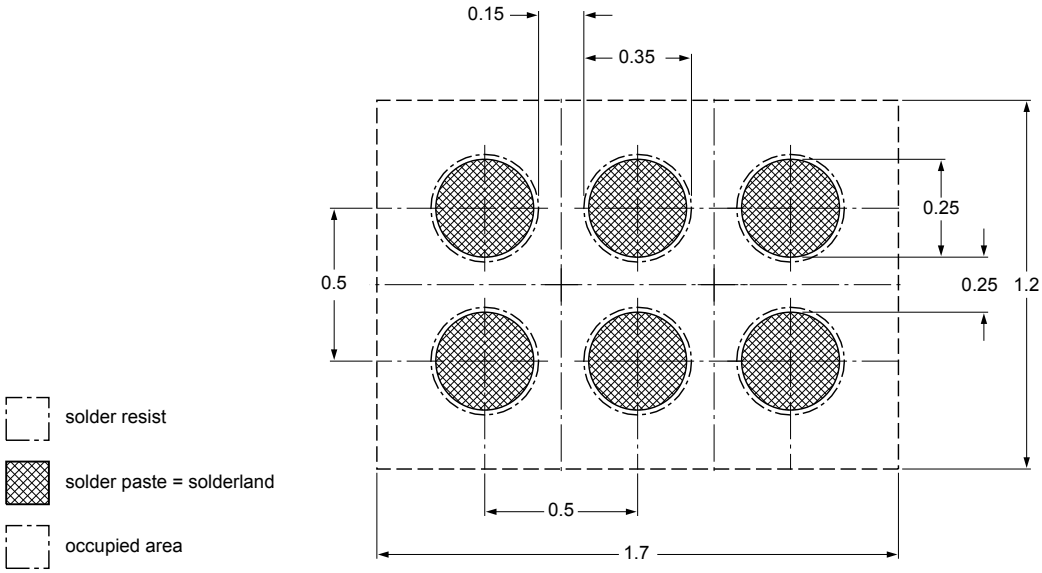
wlcsp6_3-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
WLCSP6_3-2						~~17-04-26~~ 17-05-03

Figure 19. Package outline WLCSP6_3-2

10 Soldering

Footprint information for reflow soldering **WLCSP6_3-2**



Reflow soldering is the only recommended soldering method.
Dimensions in mm.

Figure 20. Reflow soldering footprint WLCSP6

11 Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMCM650CUNE v.1	20171108	Product data sheet	-	-

12 Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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Tables

Figures

Contents

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Document identifier: PMCM650CUNE v.1

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>>Nexperia(安世)