



BUK9K45-100E

Dual N-channel TrenchMOS logic level FET

26 March 2013

Product data sheet

1. General description

Dual logic level N-channel MOSFET in a LPAK56D package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)} > 0.5 \text{ V @ } 175 \text{ °C}$

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

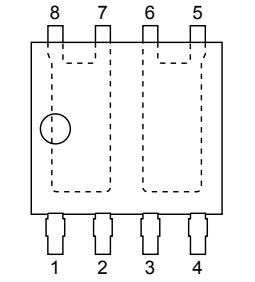
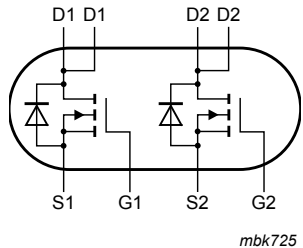
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ °C}; T_j \leq 175 \text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C}; \text{Fig. 1}$	-	-	21	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ °C}; \text{Fig. 2}$	-	-	53	W
Static characteristics FET1 and FET2						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}; \text{Fig. 12}$	-	38.3	45	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ °C}; \text{Fig. 15}; \text{Fig. 14}$	-	7.3	-	nC

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFAK56D (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K45-100E	LFAK56D	Plastic single ended surface mounted package (LFAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K45-100E	94510E

8. Limiting values

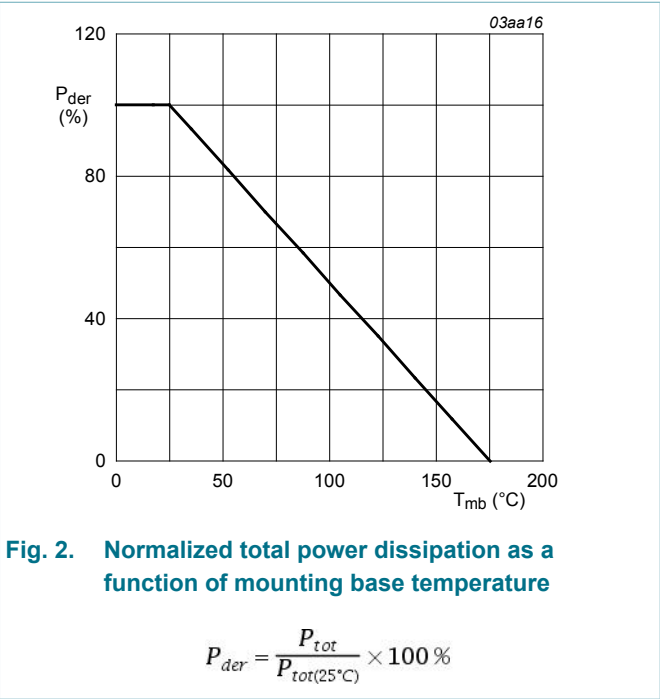
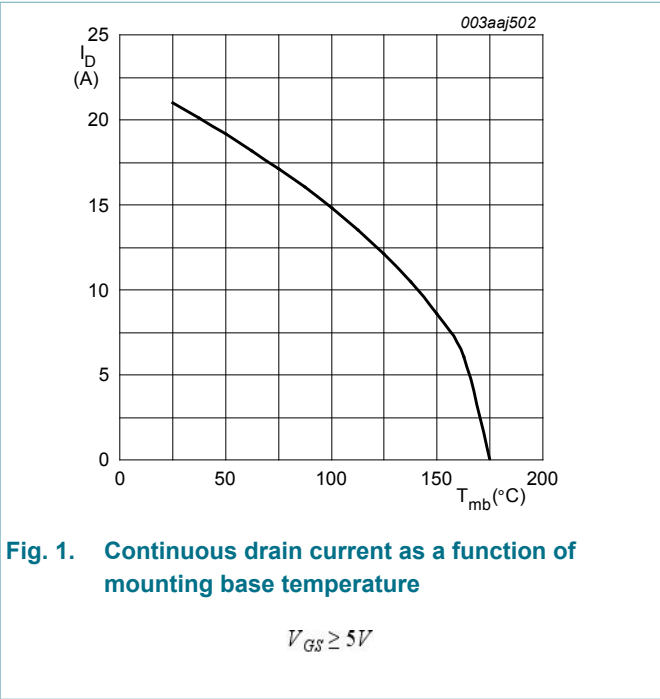
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ; T _j ≥ 25 °C; T _j ≤ 175 °C	-	100	V
V _{GS}	gate-source voltage	T _j ≤ 175 °C; DC	-10	10	V
		T _j ≤ 175 °C; Pulsed	[1][2] -15	15	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; Fig. 1	-	21	A
		T _{mb} = 100 °C; V _{GS} = 5 V; Fig. 1	-	15	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Fig. 4	-	83	A

Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	53	W
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C		-	21	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	83	A
Avalanche Ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 21 A; V _{sup} ≤ 100 V; V _{GS} = 5 V; T _{j(init)} = 25 °C; Fig. 3	[3][4]	-	48	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}.
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



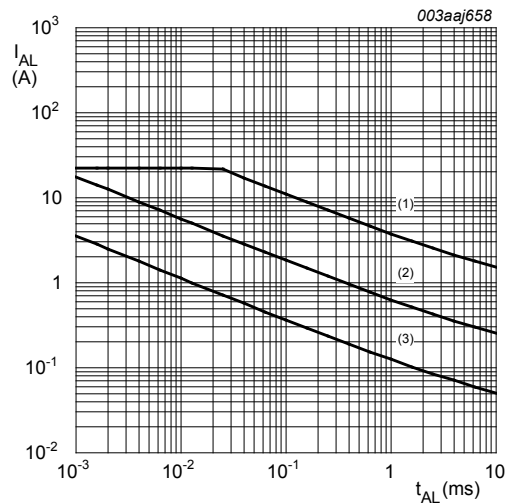


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

- (1) Single-pulse; $T_j = 25\text{ }^{\circ}\text{C}$.
- (2) Single-pulse; $T_j = 150\text{ }^{\circ}\text{C}$.
- (3) Repetitive.

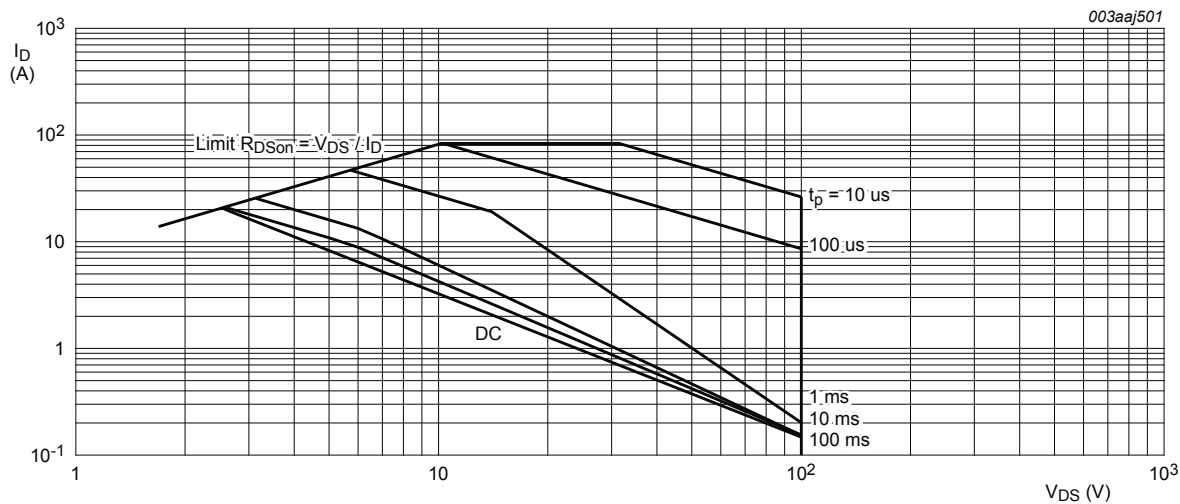


Fig. 4. Safe operating area; continuous and peak drain current as a function of drain-source voltage

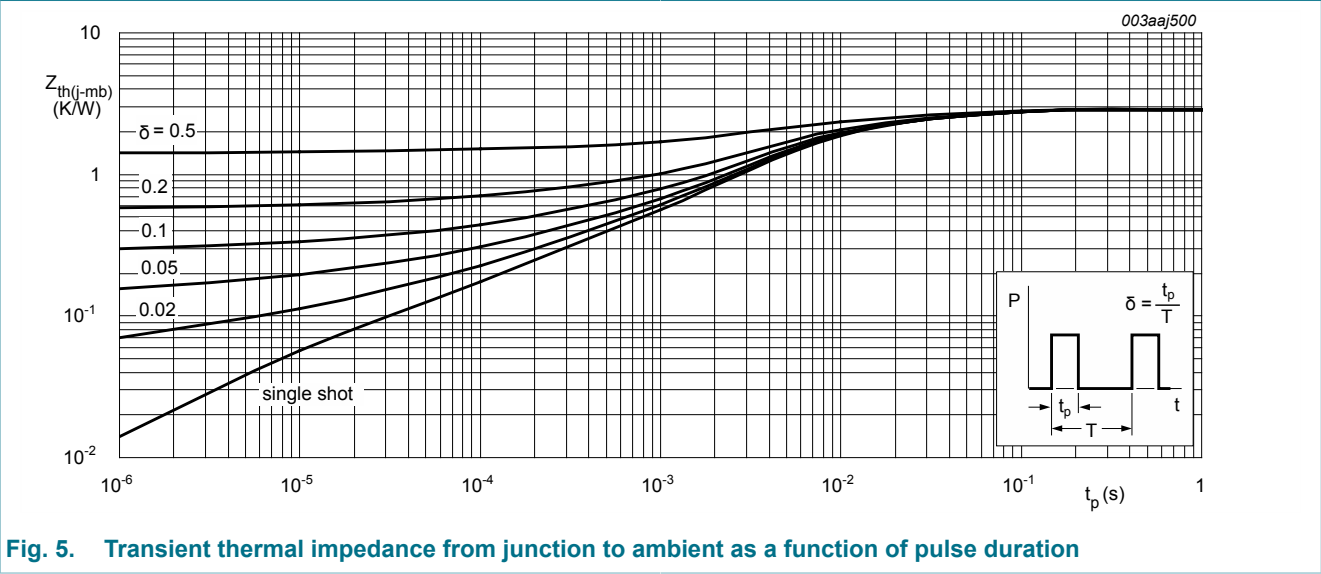
$T_{mb} = 25\text{ }^{\circ}\text{C}$; I_{DM} is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.84	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = -55\text{ }^\circ\text{C}$	90	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 10 ; Fig. 11	1.4	1.7	2.1	V
		$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_J = 175\text{ }^\circ\text{C}$; Fig. 10 ; Fig. 11	0.5	-	-	V
		$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; $T_J = -55\text{ }^\circ\text{C}$; Fig. 10 ; Fig. 11	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 175\text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = 10\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 12	-	38.3	45	m Ω
		$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_J = 175\text{ }^\circ\text{C}$; Fig. 12 ; Fig. 13	-	103	124	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 12	-	35.3	42	m Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 5\text{ A}$; $V_{DS} = 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 14 ; Fig. 15	-	33.5	-	nC
Q_{GS}	gate-source charge		-	3.5	-	nC
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}$; $V_{DS} = 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 15 ; Fig. 14	-	7.3	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 16	-	1614	2152	pF
C_{oss}	output capacitance		-	113	136	pF
C_{rss}	reverse transfer capacitance		-	72	99	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 80\text{ V}$; $R_L = 16\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_{G(ext)} = 10\text{ }\Omega$; $T_J = 25\text{ }^\circ\text{C}$; $I_D = 5\text{ A}$	-	4	-	ns
t_r	rise time		-	8.47	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = 80\text{ V}$; $R_L = 16\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_{G(ext)} = 10\text{ }\Omega$; $I_D = 18\text{ A}$; $T_J = 25\text{ }^\circ\text{C}$; $I_D = 5\text{ A}$	-	41.34	-	ns
t_f	fall time		-	27.75	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 17	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	-	29.6	-	ns
Q_r	recovered charge		-	42.9	-	nC

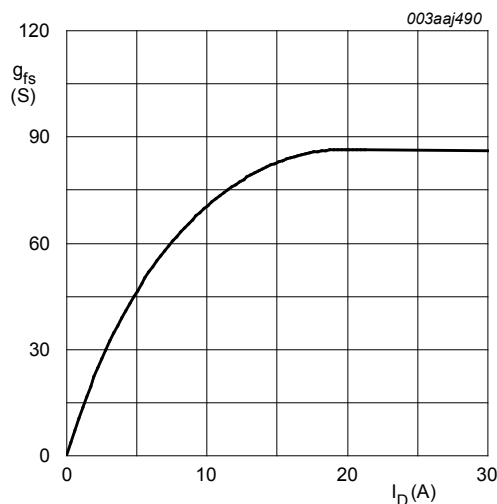


Fig. 6. Forward transconductance as a function of drain current; typical values

$$T_J = 25\text{ }^\circ\text{C}; V_{DS} = 15\text{ V}$$

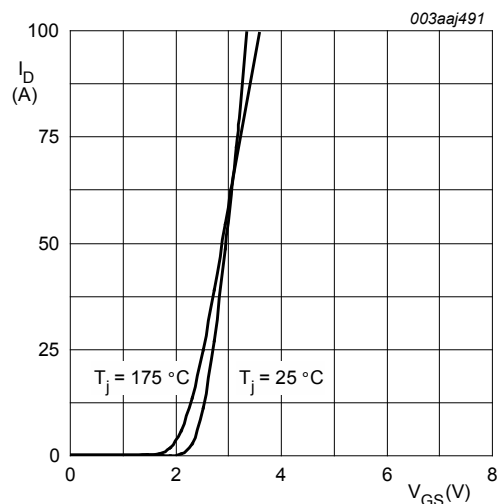


Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10\text{ V}$$

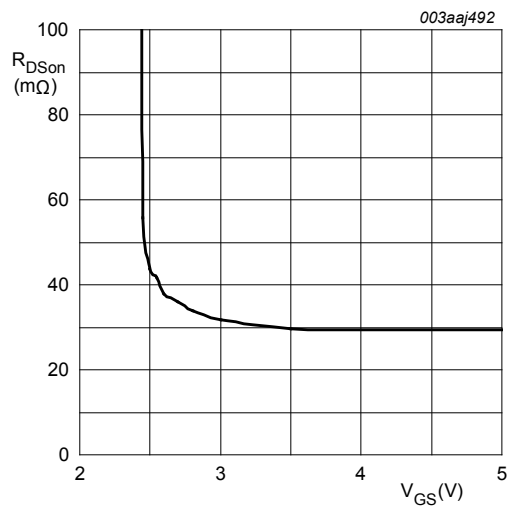


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}$; $I_D = 5\text{ A}$

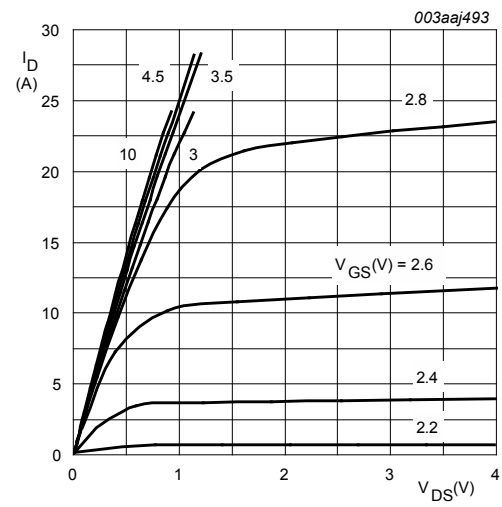


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}$

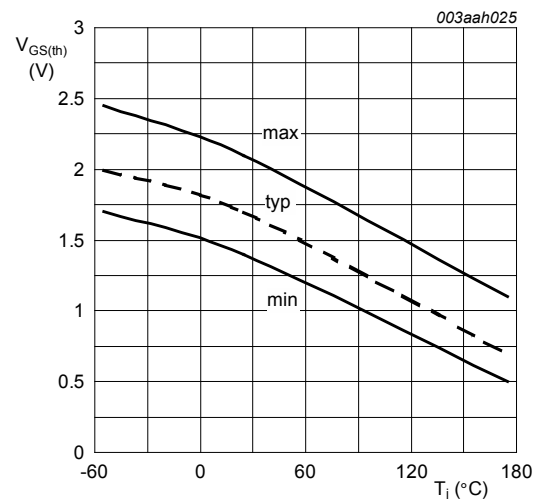


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

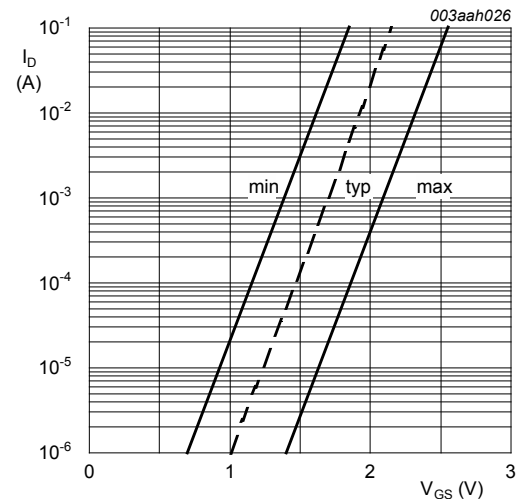


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 5\text{ V}$

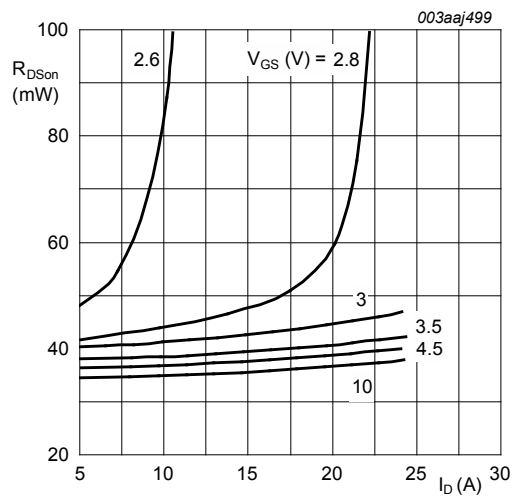


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

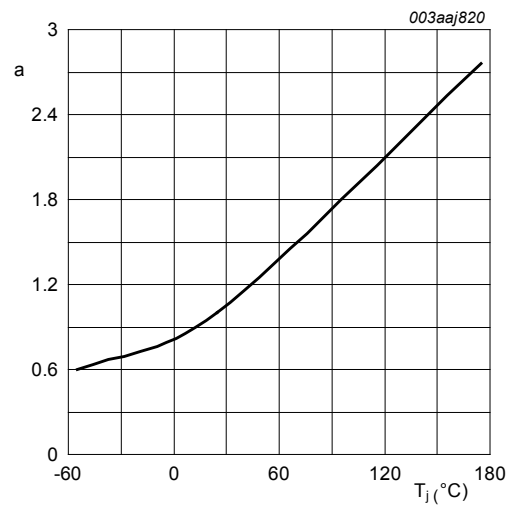


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

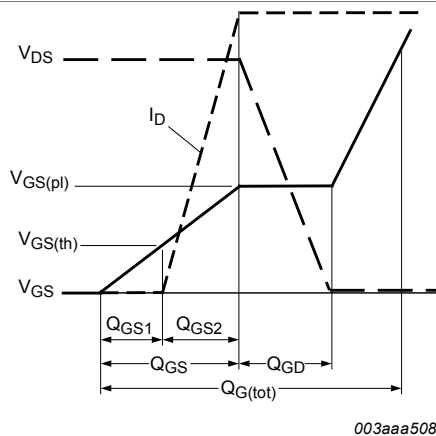


Fig. 14. Gate charge waveform definitions

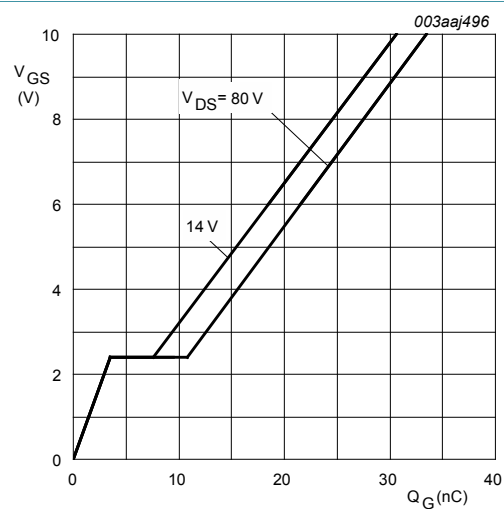


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 5\text{ A}$

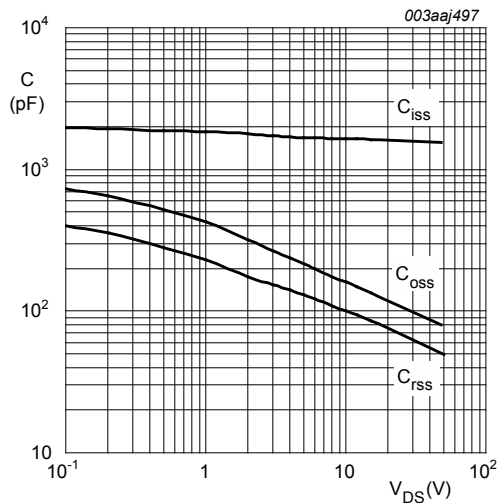


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

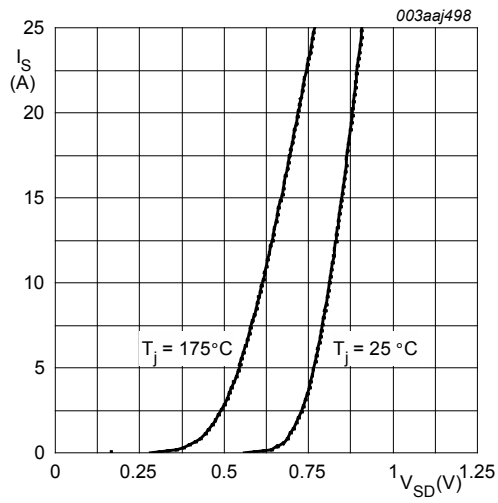


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{ V}$

11. Package outline

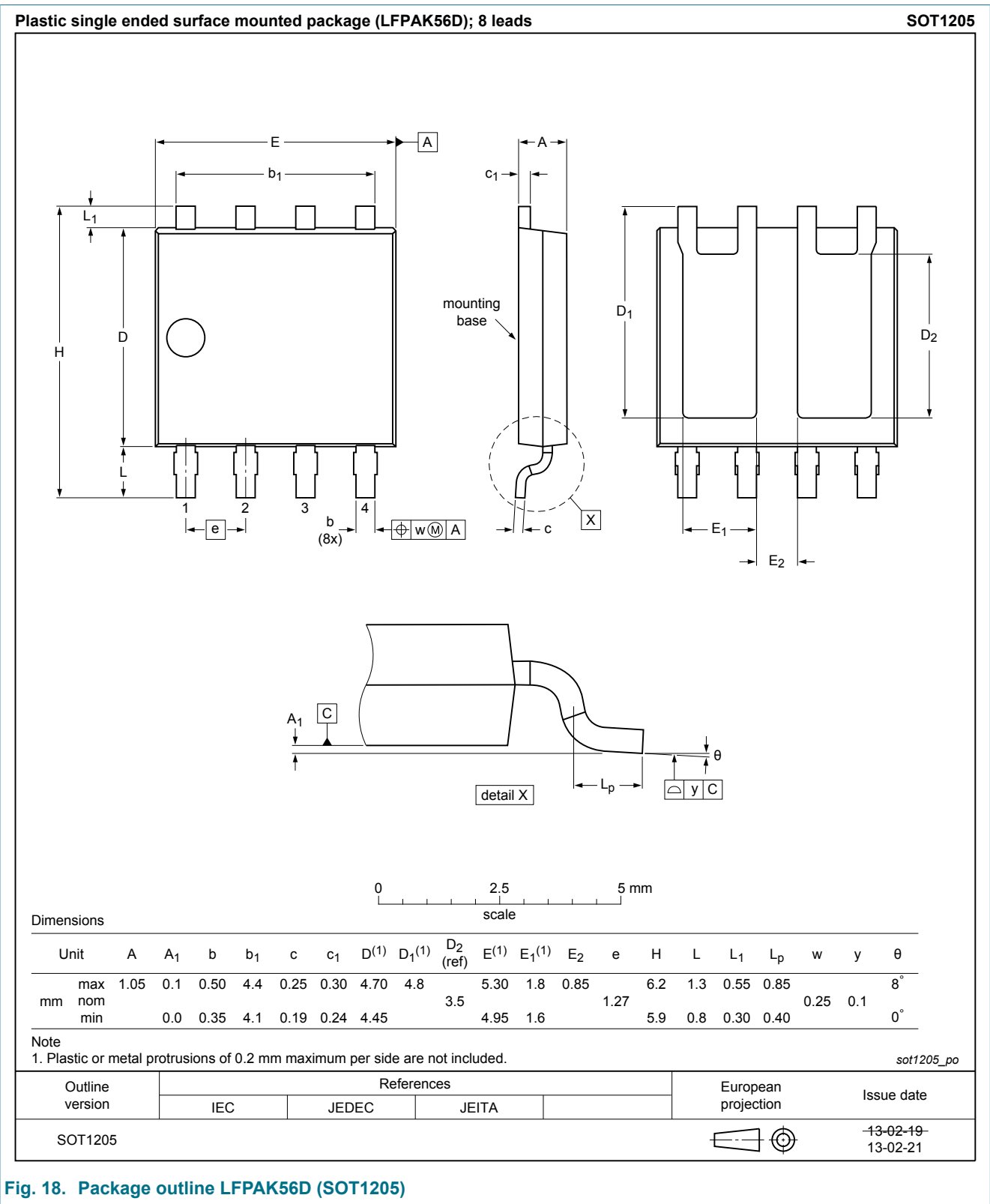


Fig. 18. Package outline LPAK56D (SOT1205)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 26 March 2013

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