



PSMN4R2-40VSH

Dual N-channel 40 V, 4.2 mOhm standard level MOSFET in LFPAK56D (half-bridge configuration)

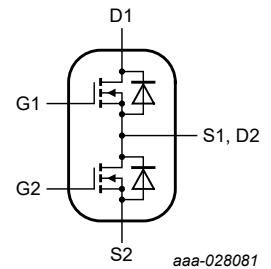
16 August 2021

Product data sheet

1. General description

Dual, standard level N-channel MOSFET in an LFPAK56D package (half-bridge configuration), using NextpowerS3 technology.

An internal connection is made between the source (S1) of the high-side FET to the drain (D2) of the low-side FET, making the device ideal to use as a half-bridge switch in high-performance PWM and space constrained motor drive applications



2. Features and benefits

- LFPAK56D package with half-bridge configuration enables:
 - Reduced PCB layout complexity
 - Module shrinkage through reduced component count
 - Improved system level $R_{th(j-amb)}$ due to optimized package design
 - Lower parasitic inductance to support higher efficiency
 - Footprint compatibility with LFPAK56D Dual package
- NextpowerS3 technology
- Low power losses, high power density
- Superior avalanche performance
- Repetitive avalanche rated
- LFPAK copper clip packaging provides high robustness and reliability
- Gull wing leads support high manufacturability and Automated Optical Inspection (AOI)

3. Applications

- Handheld power tools, portable appliance and space constrained applications
- Brushless or brushed DC motor drive
- DC-to-DC systems
- LED lighting

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Limiting values FET1 and FET2						
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	[1]	-	98	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	85	W
T_j	junction temperature		-55	-	175	°C

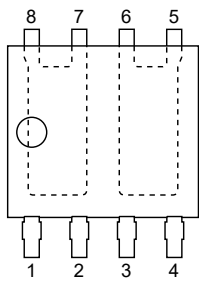
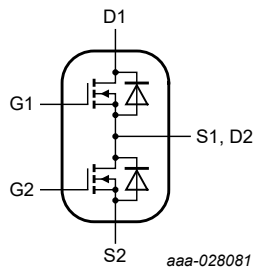
Dual N-channel 40 V, 4.2 mOhm standard level MOSFET in LFPAK56D (half-bridge configuration)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 8	-	3.5	4.2	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 20\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 10; Fig. 11	1.4	4.7	9.4	nC
$Q_{G(tot)}$	total gate charge		17	26	37	nC

[1] 98A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S2	source2	 <p>LFPAK56D; Dual LFPAK (SOT1205)</p>	 <p>aaa-028081</p>
2	G2	gate2		
3	S1	source1		
4	G1	gate1		
5	D1	drain1		
6	D1	drain1		
7	S1, D2	source1, drain2		
8	S1, D2	source1, drain2		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN4R2-40VSH	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R2-40VSH	4H2S40V

8. Limiting values

Table 5. Limiting values

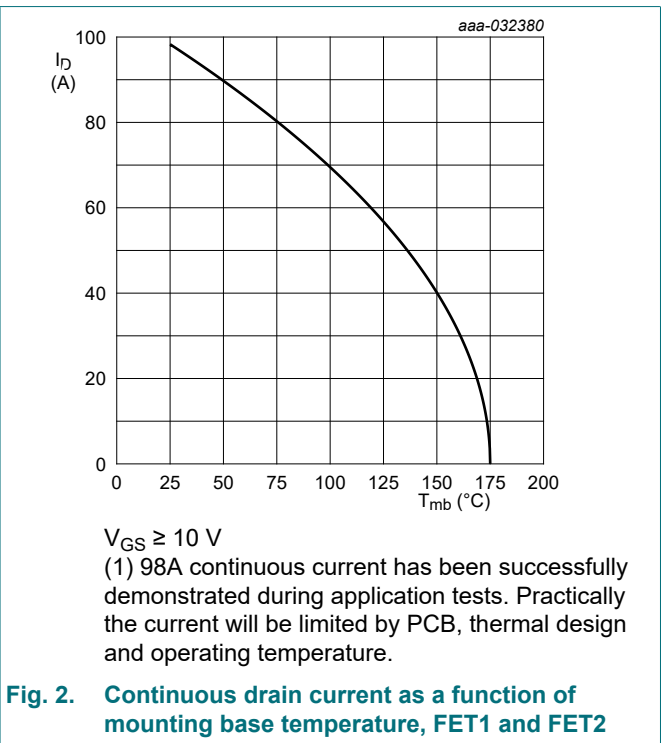
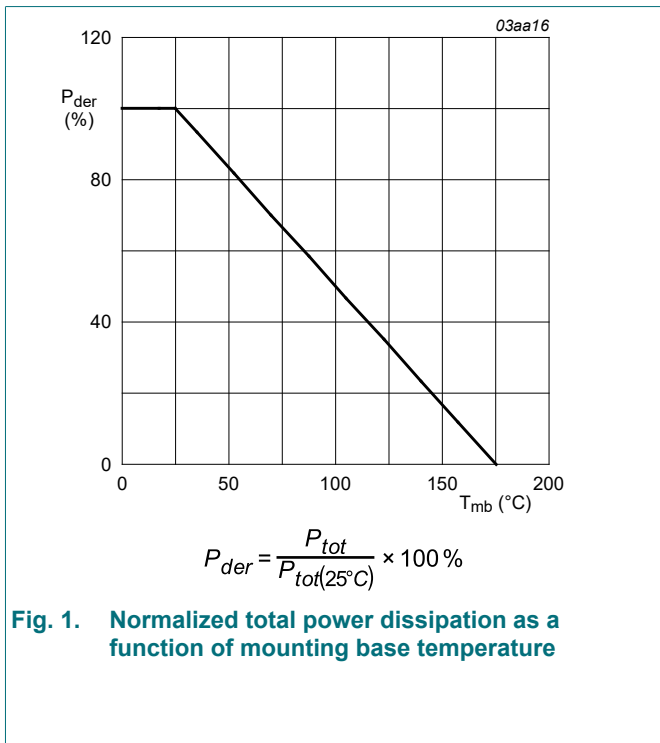
In accordance with the Absolute Maximum Rating System (IEC 60134).

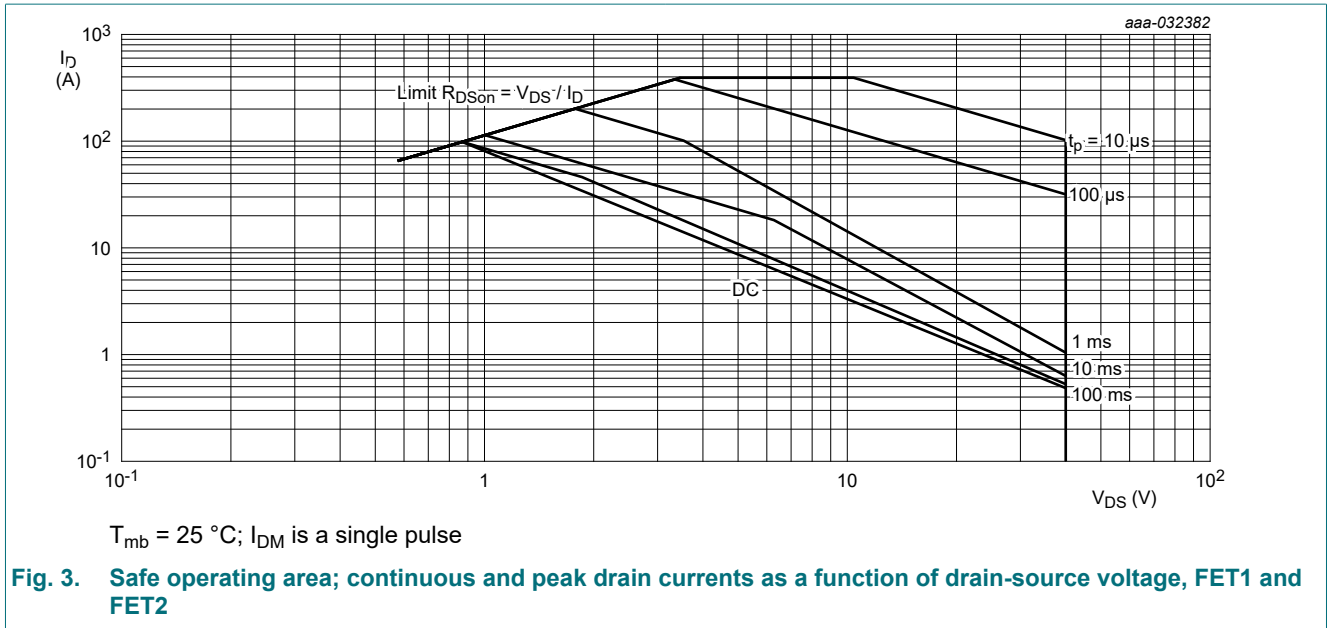
Symbol	Parameter	Conditions	Min	Max	Unit
Limiting values FET1 and FET2					
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
V_{DSM}	peak drain-source voltage	$t_p = 20\text{ ns}$; $f = 500\text{ kHz}$; $E_{DS(AL)} = 200\text{ nJ}$; pulsed	-	45	V

Dual N-channel 40 V, 4.2 mOhm standard level MOSFET in LPAK56D (half-bridge configuration)

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ		-	40	V
V _{GS}	gate-source voltage	T _j ≤ 175 °C		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	85	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	98	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	69.5	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	393	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C		-	85	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	393	A
Avalanche ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 82.6 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 20 μs		-	42.3	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	82.6	A

- [1] 98A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

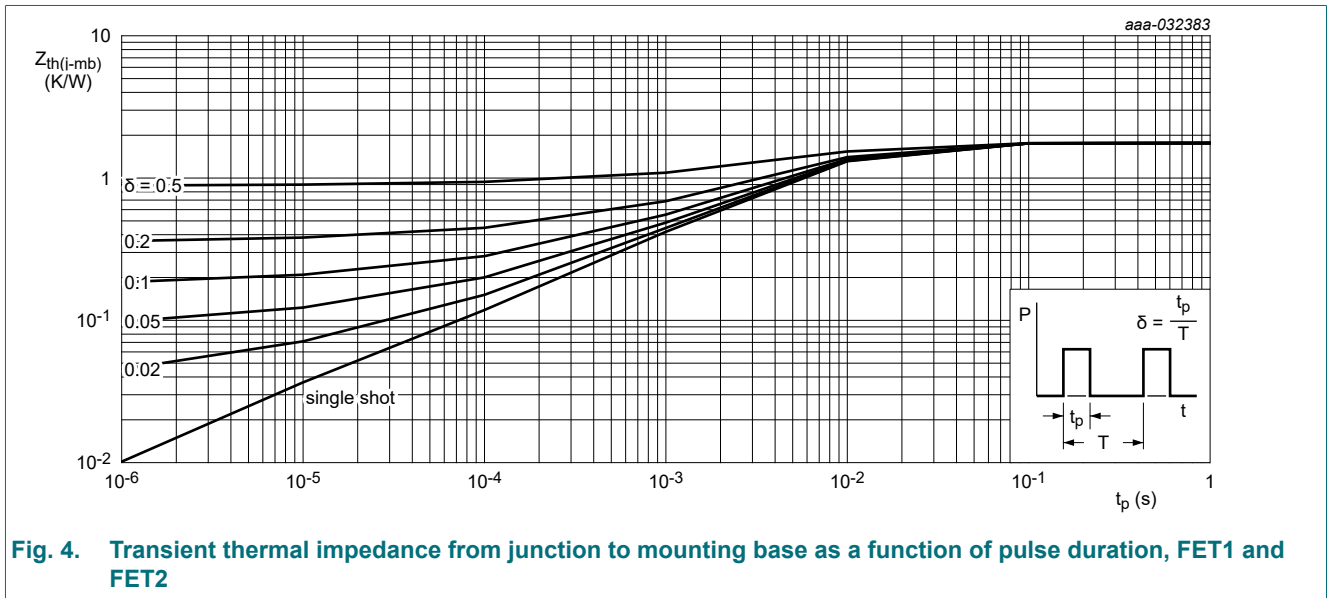




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.64	1.76	K/W



10. Characteristics

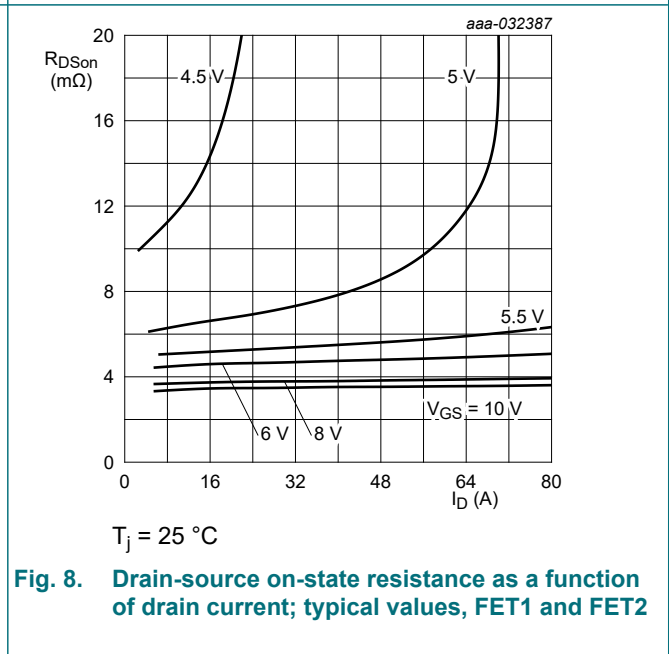
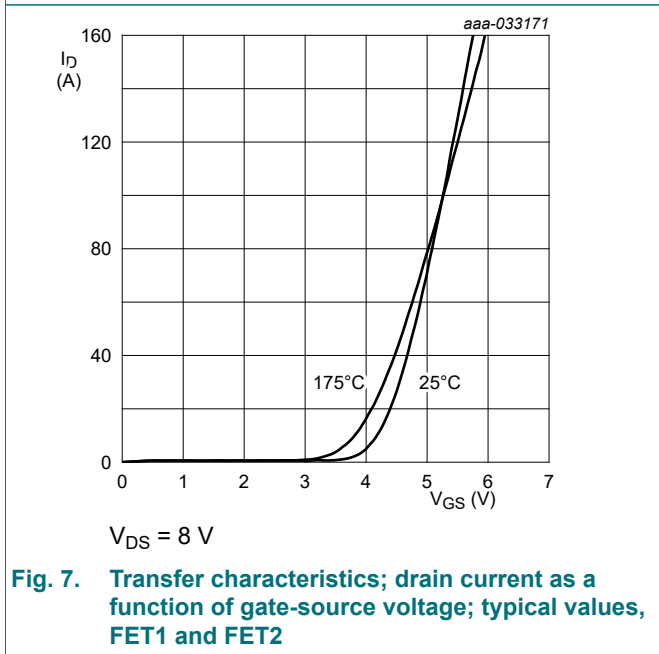
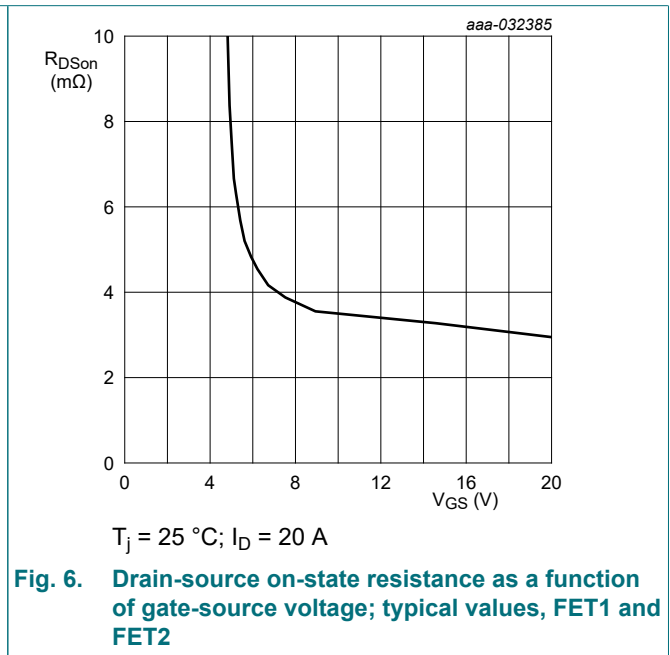
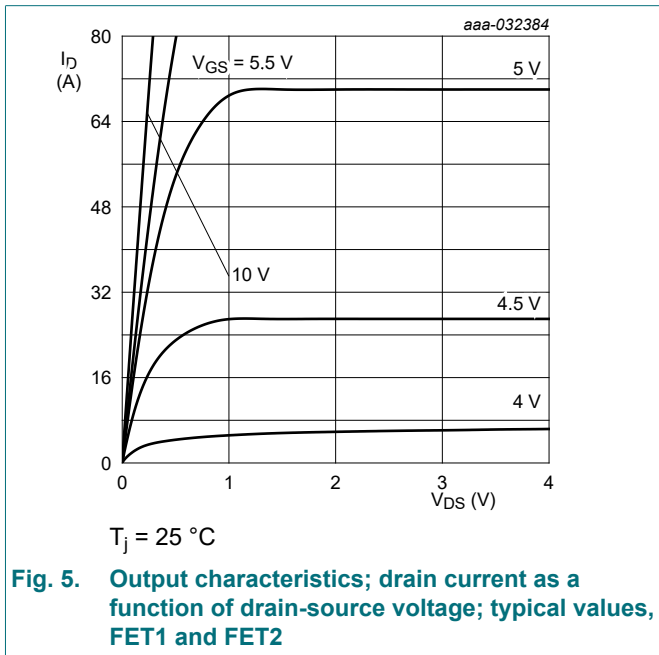
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	2.4	3	3.6	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-6.2	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	μA
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	0.3	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 8	-	3.5	4.2	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 9	-	-	8.8	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.72	1.8	4.5	Ω
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 20 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V}$; Fig. 10 ; Fig. 11	17	26	37	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	13	-	nC
Q_{GS}	gate-source charge	$I_D = 20 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V}$; Fig. 10 ; Fig. 11	4.7	7.8	12	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		3	5.1	7.7	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		1.6	2.7	4	nC
Q_{GD}	gate-drain charge		1.4	4.7	9.4	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 20 \text{ A}; V_{DS} = 32 \text{ V}$; Fig. 10 ; Fig. 11	-	4.4	-	V
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 12	1202	1850	2590	pF
C_{oss}	output capacitance		367	565	791	pF
C_{rss}	reverse transfer capacitance		27	91	200	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.5 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega$	-	7	-	ns
t_r	rise time		-	9	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	11.8	-	ns
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	22	-	nC
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 20 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 13	-	0.81	1	V

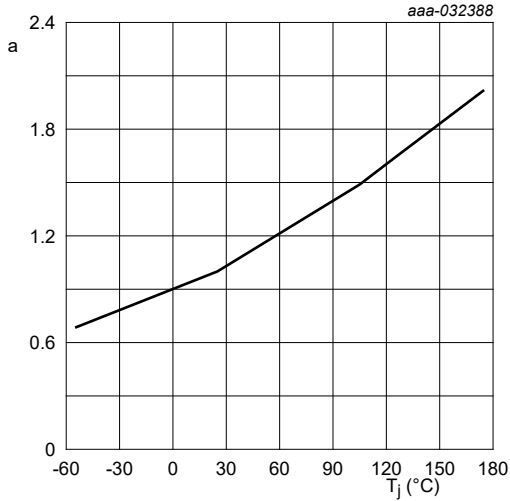
Dual N-channel 40 V, 4.2 mOhm standard level MOSFET in LPAK56D (half-bridge configuration)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 14	-	18.6	-	ns	
Q_r	recovered charge		[1]	-	9.2	-	nC
t_a	reverse recovery rise time		-	-	10.3	-	ns
t_b	reverse recovery fall time		-	-	8.2	-	ns

[1] includes capacitive recovery



Dual N-channel 40 V, 4.2 mOhm standard level MOSFET in LPAK56D (half-bridge configuration)



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

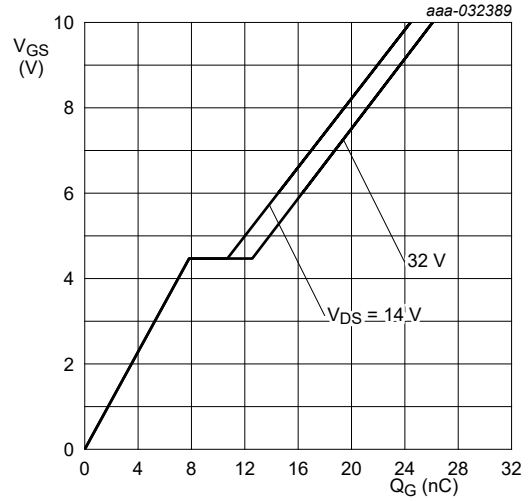


Fig. 10. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

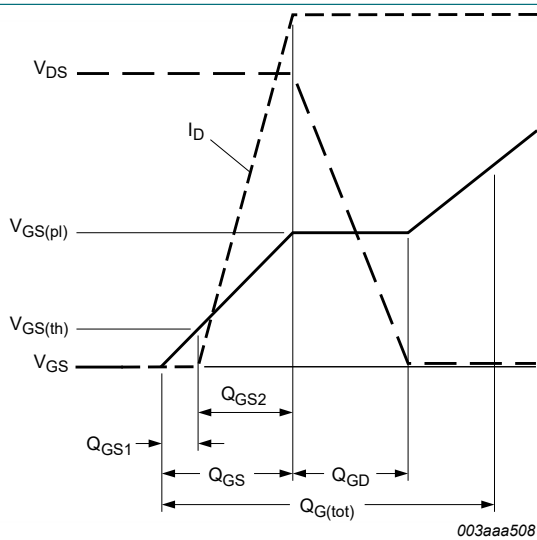


Fig. 11. Gate charge waveform definitions

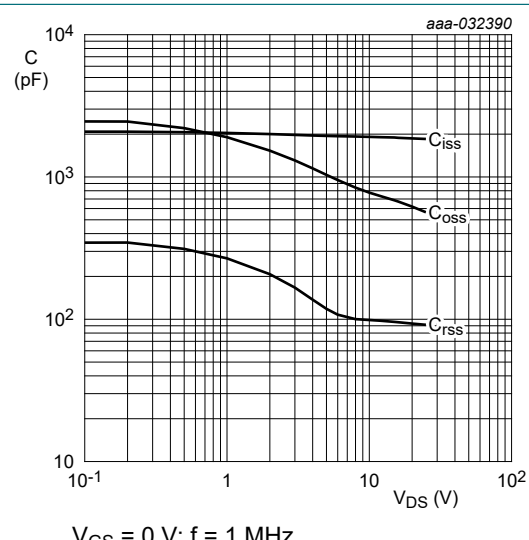
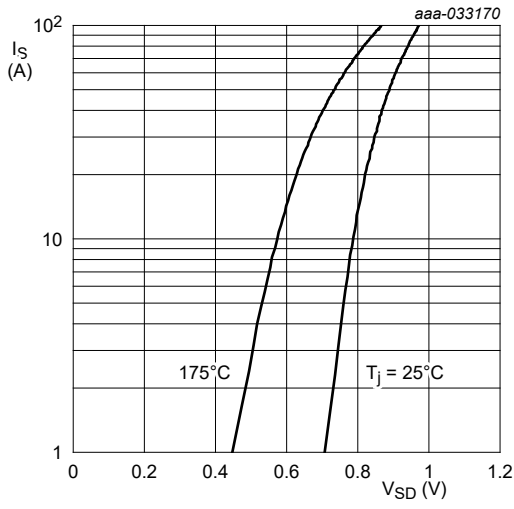


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

Dual N-channel 40 V, 4.2 mOhm standard level MOSFET in LFPAK56D (half-bridge configuration)



$V_{GS} = 0\text{ V}$

Fig. 13. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

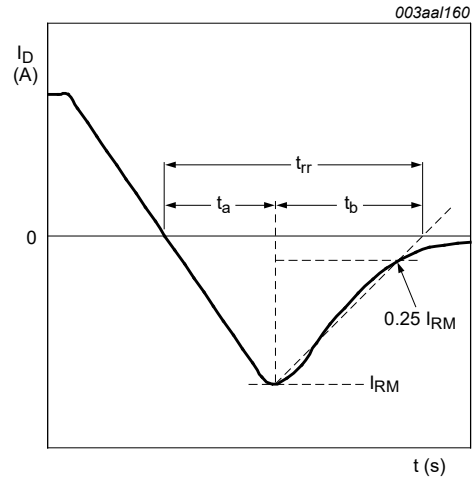


Fig. 14. Reverse recovery timing definition

11. Package outline

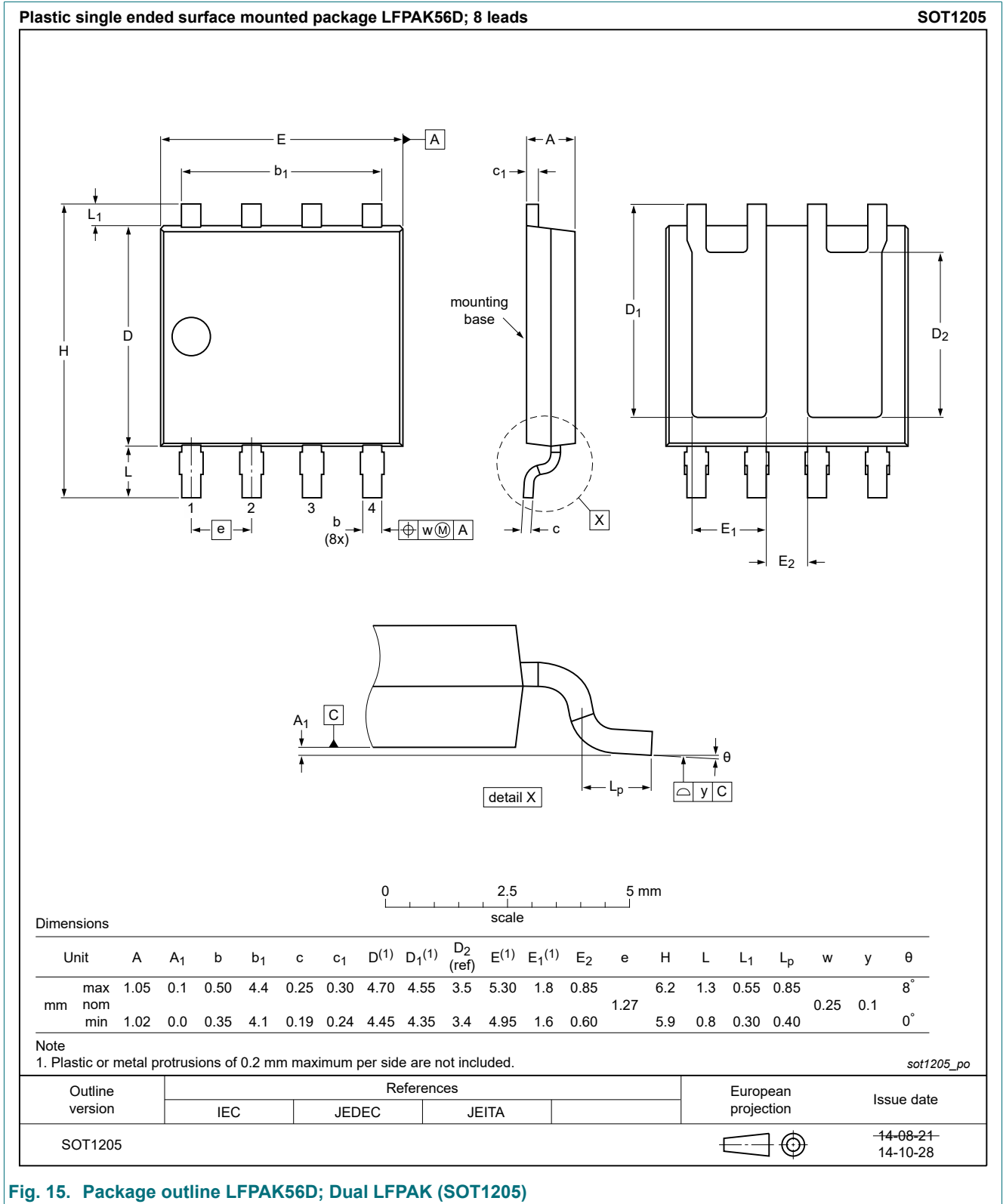


Fig. 15. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

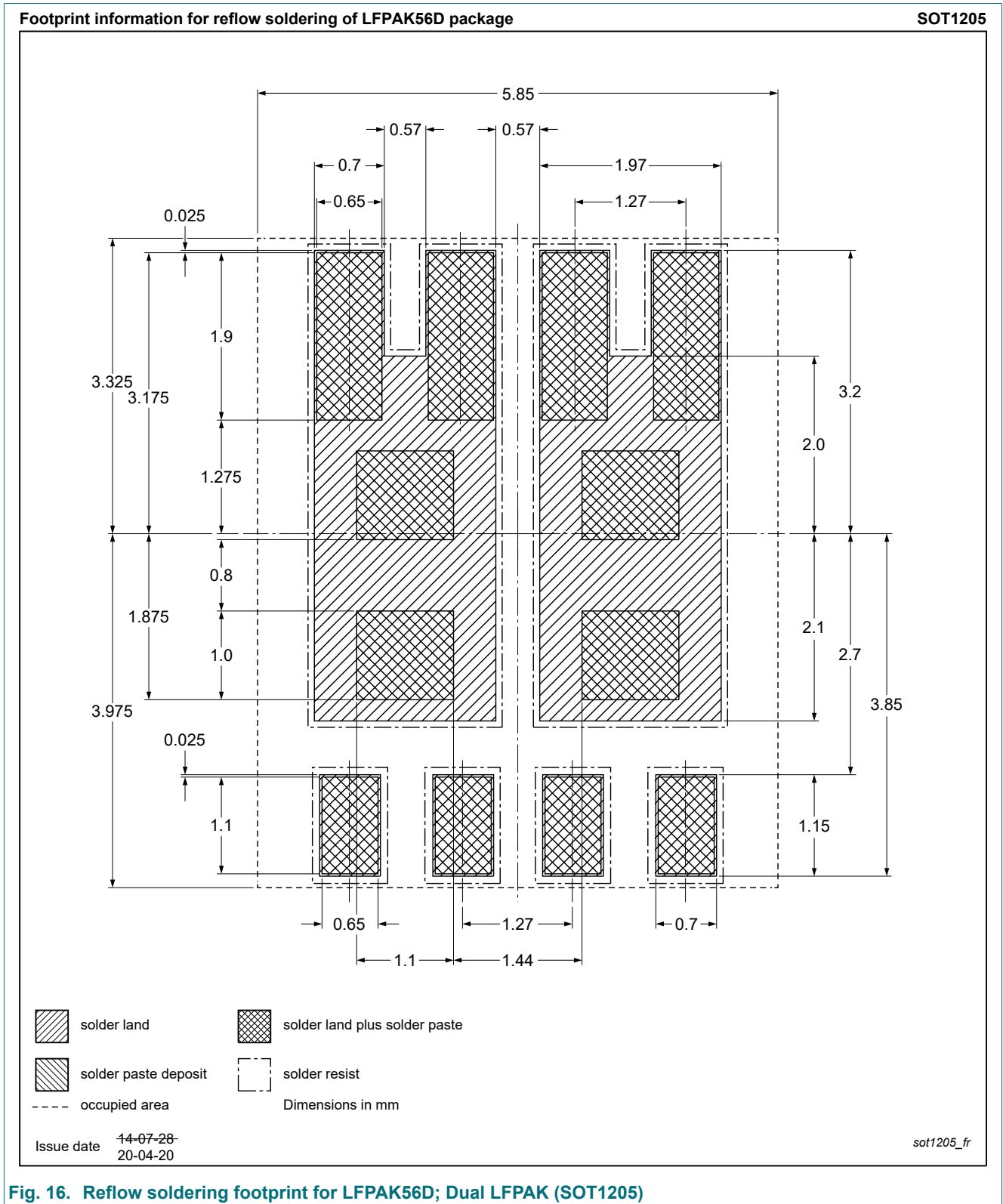


Fig. 16. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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