



BUK764R0-55B

N-channel TrenchMOS standard level FET

Rev. 5 — 22 April 2011

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using Nexperia High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 4	[1] -	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	300	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 7 ; see Figure 12	-	3.4	4	mΩ

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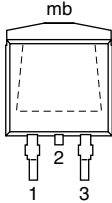
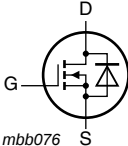
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped	-	-	1.2	J
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 44\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 13	-	25	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		
			SOT404 (D2PAK)	

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK764R0-55B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 4	[1] -	75	A
			[2][3] -	193	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	[1] -	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 4	-	774	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	300	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	[2][1] -	193	A
			[1] -	75	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	774	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	1.2	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[4][5][6][7] -	-	J

[1] Continuous current is limited by package.

[2] Current is limited by power dissipation chip rating.

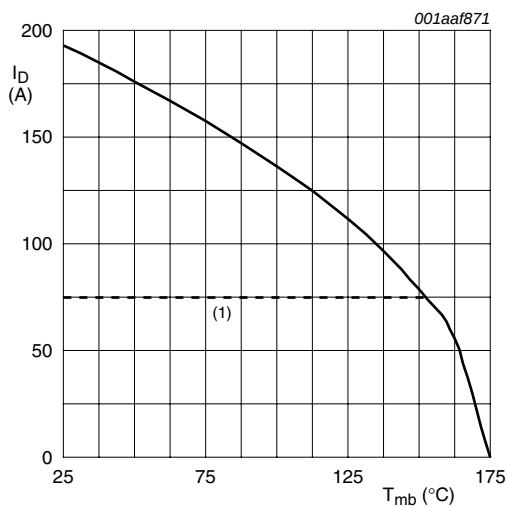
[3] Refer to document 9397 750 12572 for further information.

[4] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.

[5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

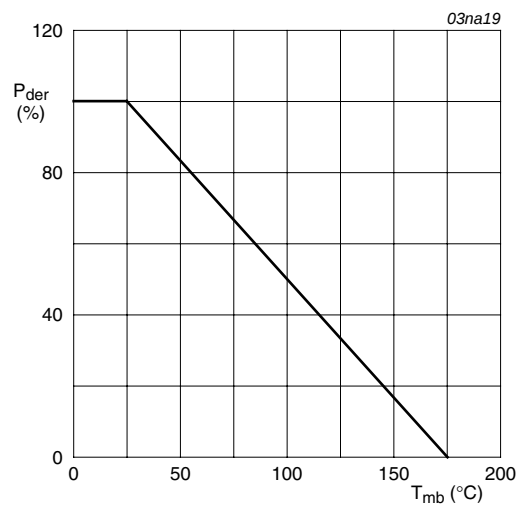
[6] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[7] Refer to application note AN10273 for further information.



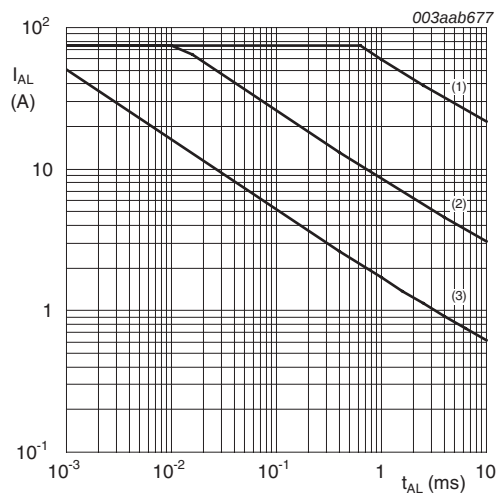
$V_{GS} \geq 10\text{ V}$
(1) Capped at 75 A due to package.

Fig. 1. Continuous drain current as a function of mounting base temperature.



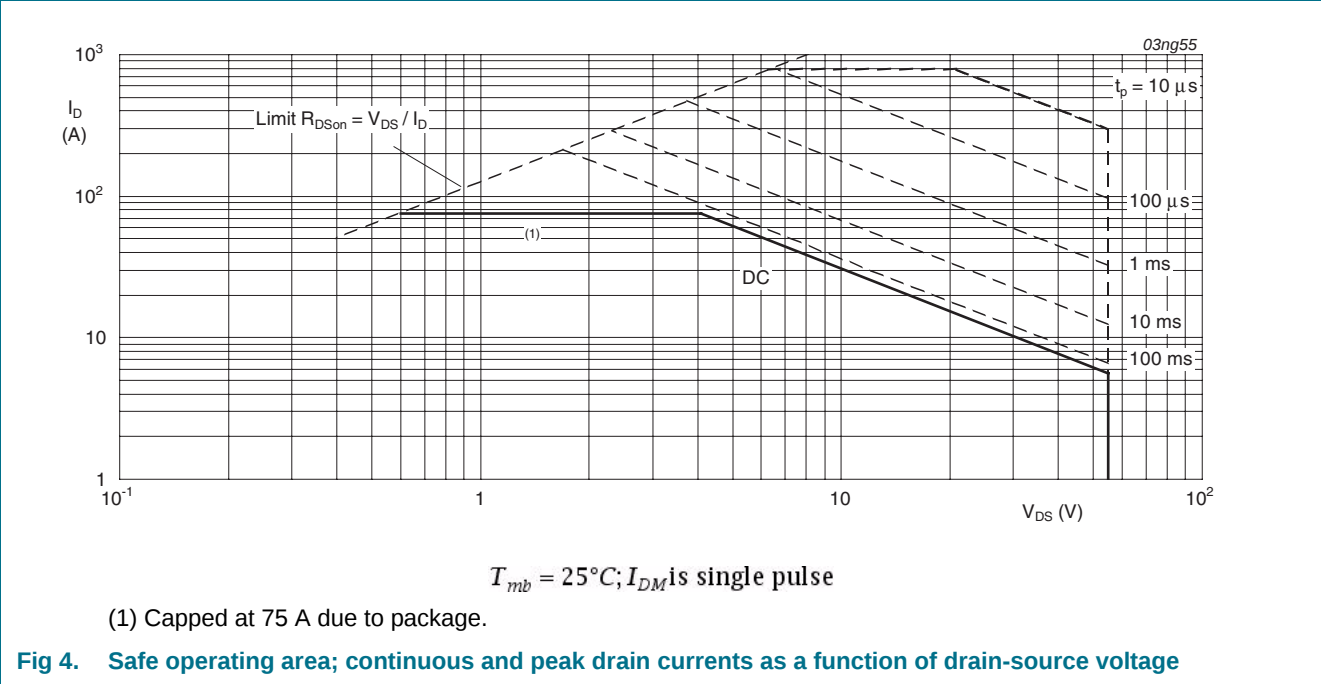
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig. 2. Normalized total power dissipation as a function of mounting base temperature



- (1) Single-pulse; $T_j = 25\text{ }^\circ\text{C}$.
- (2) Single-pulse; $T_j = 150\text{ }^\circ\text{C}$.
- (3) Repetitive

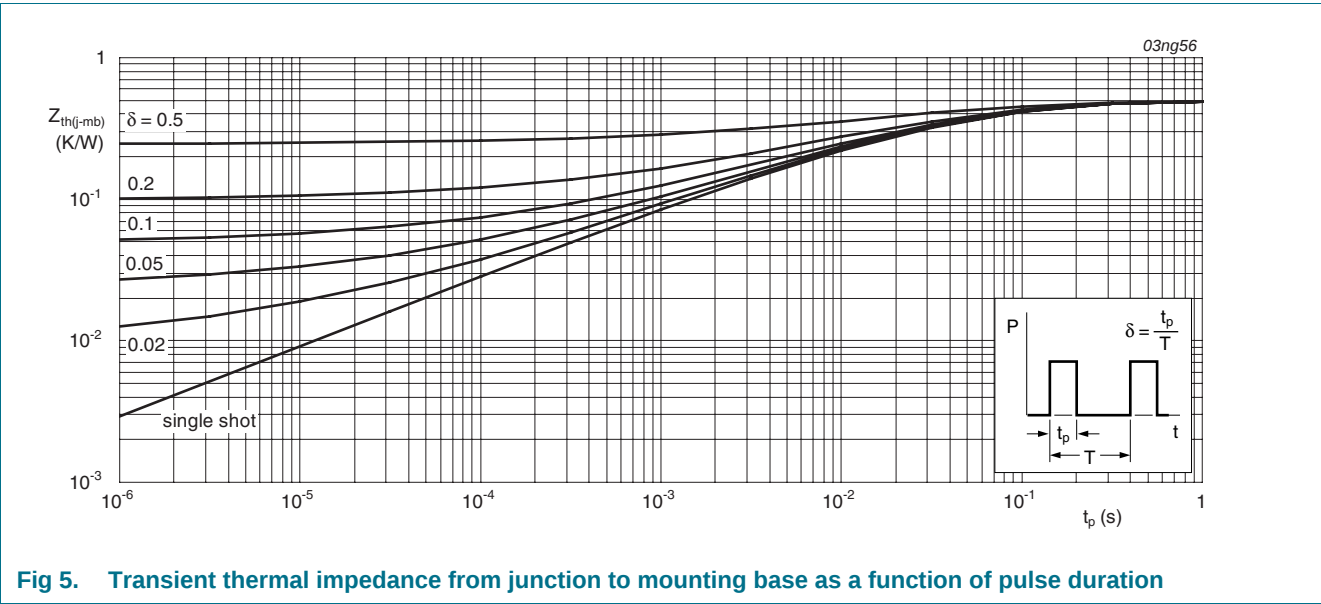
Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time.



5. Thermal characteristics

Table 5. Thermal characteristics

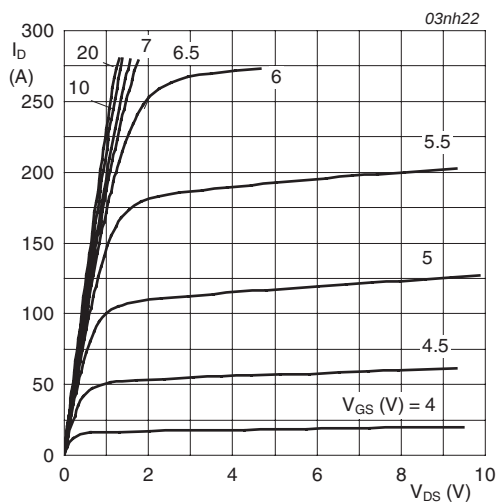
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W



6. Characteristics

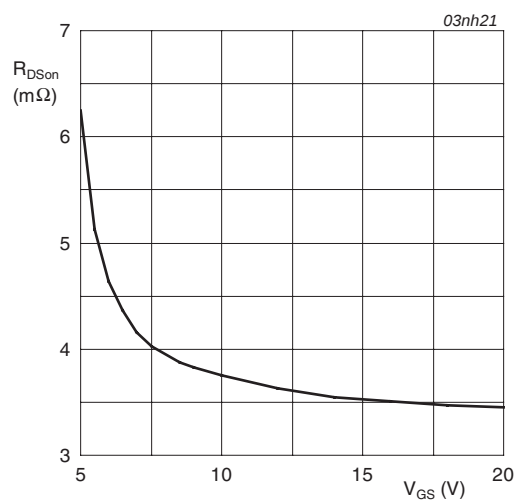
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _J = 25 °C	55	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _J = -55 °C	50	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; see Figure 11	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; see Figure 11	-	-	4.4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; see Figure 11	1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 55 V; V _{GS} = 0 V; T _J = 175 °C	-	-	500	µA
		V _{DS} = 55 V; V _{GS} = 0 V; T _J = 25 °C	-	0.02	1	µA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; see Figure 7 ; see Figure 12	-	-	8	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; see Figure 7 ; see Figure 12	-	3.4	4	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 44 V; V _{GS} = 10 V; T _J = 25 °C; see Figure 13	-	86	-	nC
Q _{GS}	gate-source charge		-	18	-	nC
Q _{GD}	gate-drain charge		-	25	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _J = 25 °C; see Figure 14	-	5082	6776	pF
C _{oss}	output capacitance		-	1054	1265	pF
C _{rss}	reverse transfer capacitance		-	450	617	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω; T _J = 25 °C	-	23	-	ns
t _r	rise time		-	51	-	ns
t _{d(off)}	turn-off delay time		-	71	-	ns
t _f	fall time		-	41	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to centre of die; T _J = 25 °C	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die; T _J = 25 °C	-	4.5	-	nH
L _S	internal source inductance	from source lead to source bond pad; T _J = 25 °C	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 40 A; V _{GS} = 0 V; T _J = 25 °C; see Figure 15	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/µs; V _{GS} = -10 V; V _{DS} = 30 V; T _J = 25 °C	-	95	-	ns
Q _r	recovered charge		-	251	-	nC



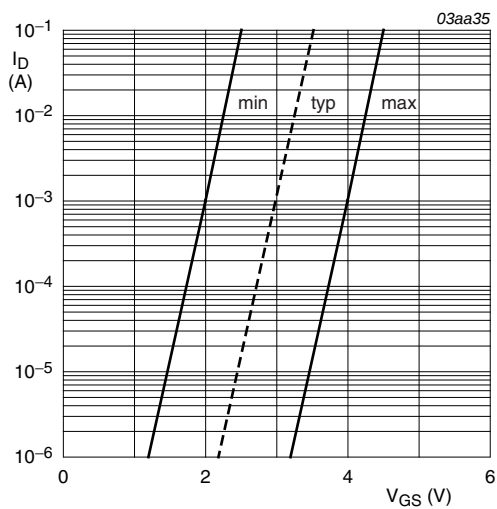
$T_j = 25^{\circ}\text{C}; t_p = 300\mu\text{s}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



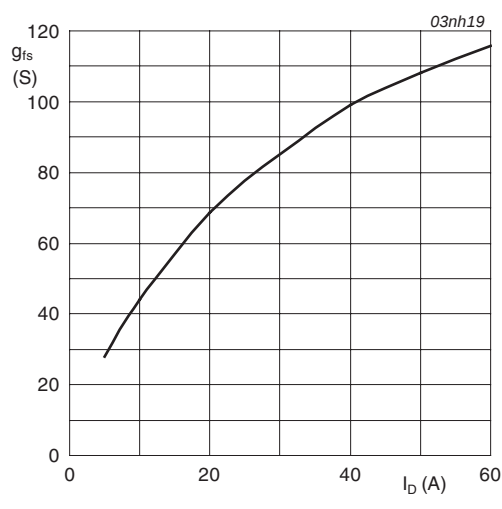
$T_j = 25^{\circ}\text{C}; I_D = 25\text{A}$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^{\circ}\text{C}; V_{DS} = 25\text{V}$

Fig 9. Forward transconductance as a function of drain current; typical values

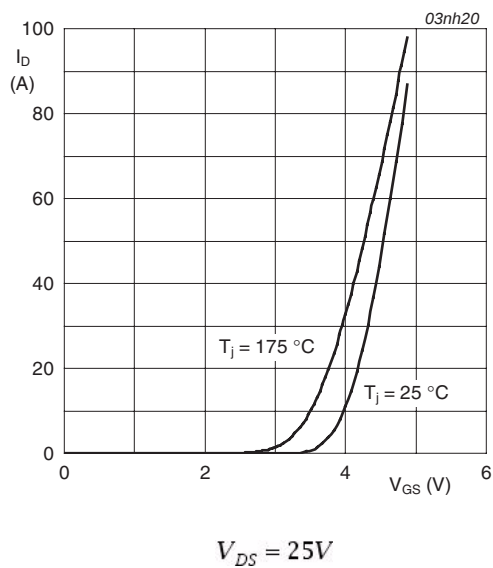


Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

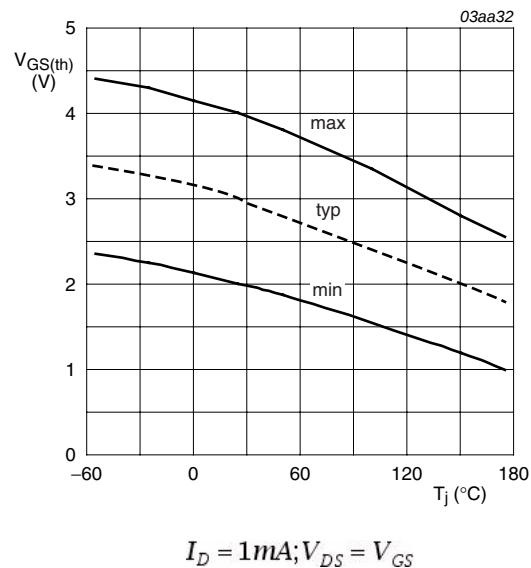


Fig 11. Gate-source threshold voltage as a function of junction temperature

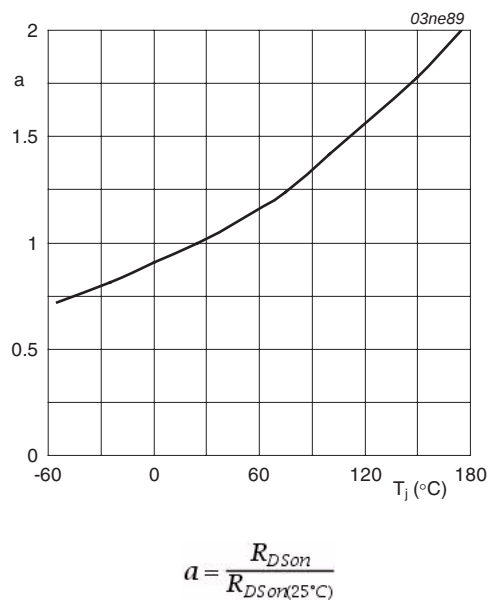


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

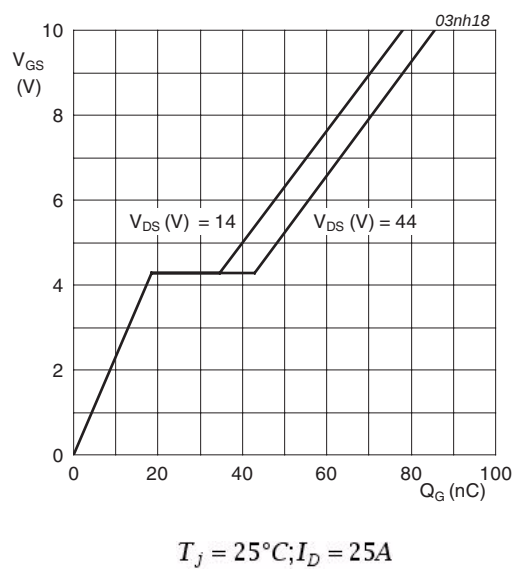
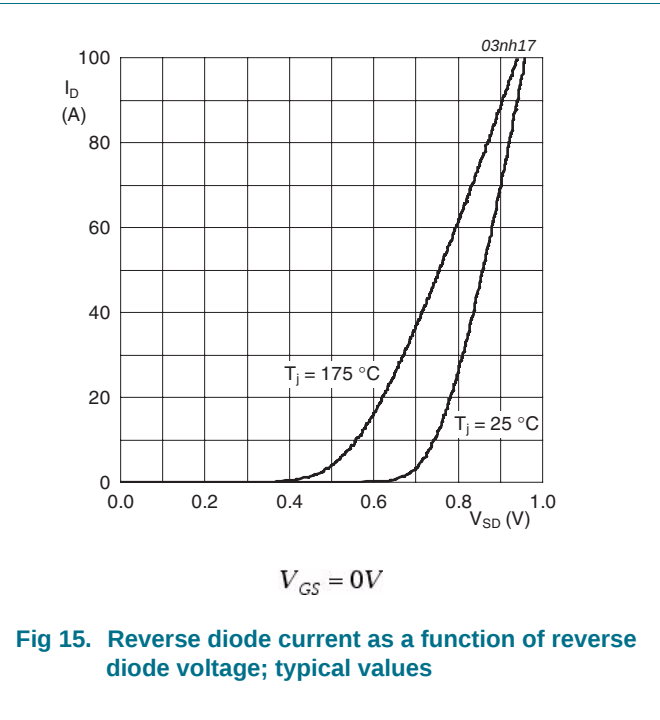
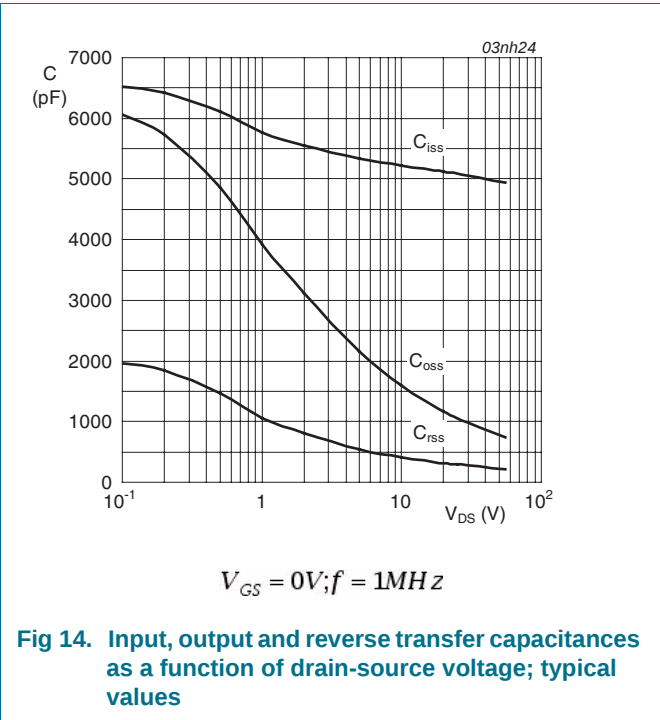


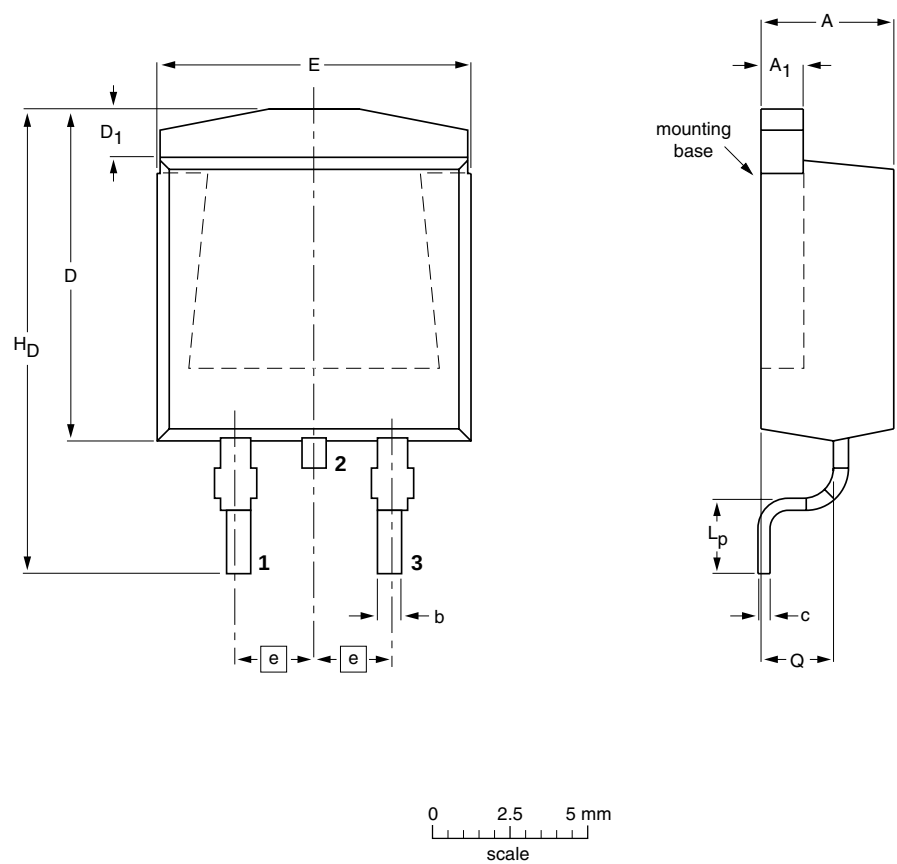
Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values



7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK764R0-55B v.5	20110422	Product data sheet	-	BUK75_764R0-55B_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number BUK764R0-55B separated from data sheet BUK75_764R0-55B_4.			
BUK75_764R0-55B_4	20071004	Product data sheet	-	BUK75_764R0-55B_3

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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