

28 V, P-channel Trench MOSFET

12 July 2023

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Trench MOSFET technology
- Very fast switching
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Table II dalen							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-28	V
V _{GS}	gate-source voltage			-12	-	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-	-4	А
Static characte	eristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -4 A; T _j = 25 °C		-	41	50	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².



5. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	3	D
2	S	source		
3	D	drain		G G S
			SOT23	017aaa094

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PMV41XPA	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23		

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PMV41XPA	%5H

[1] % = placeholder for manufacturing site code

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8. Limiting values

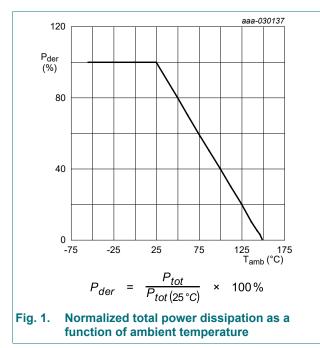
Table 5. Limiting values

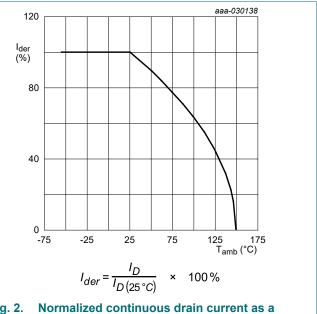
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-28	V
V _{GS}	gate-source voltage	_		-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-4	А
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-3	А
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \ \mu s$		-	-38	А
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	510	mW
			[1]	-	1.2	W
		T _{sp} = 25 °C		-	7	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	n diode					
ls	source current	T _{amb} = 25 °C	[1]	-	-1.2	А
Avalanche r	uggedness					
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	$T_{j(init)} = 25 \text{ °C; } I_D = -1.1 \text{ A; DUT in}$ (avalanche (unclamped)		-	17.5	mJ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

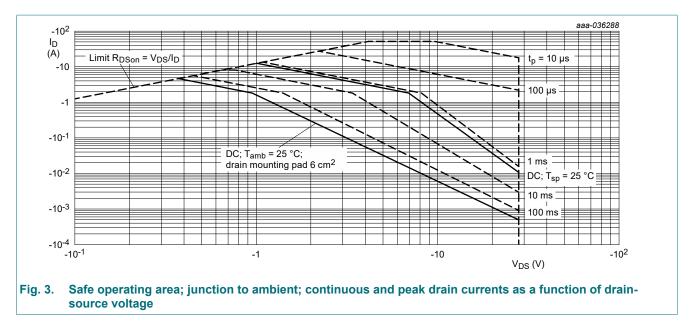
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.







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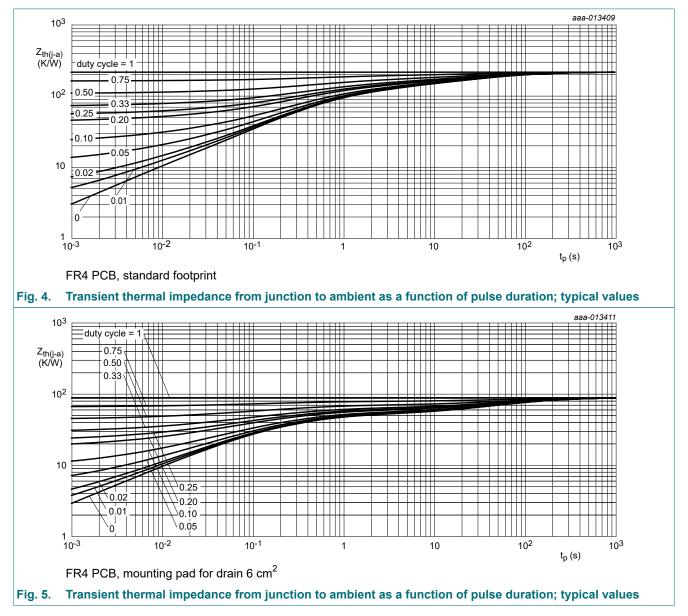
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9. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)} thermal resistance from	in free air	[1]	-	208	245	K/W	
	junction to ambient		[2]	-	88	104	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	13	18	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

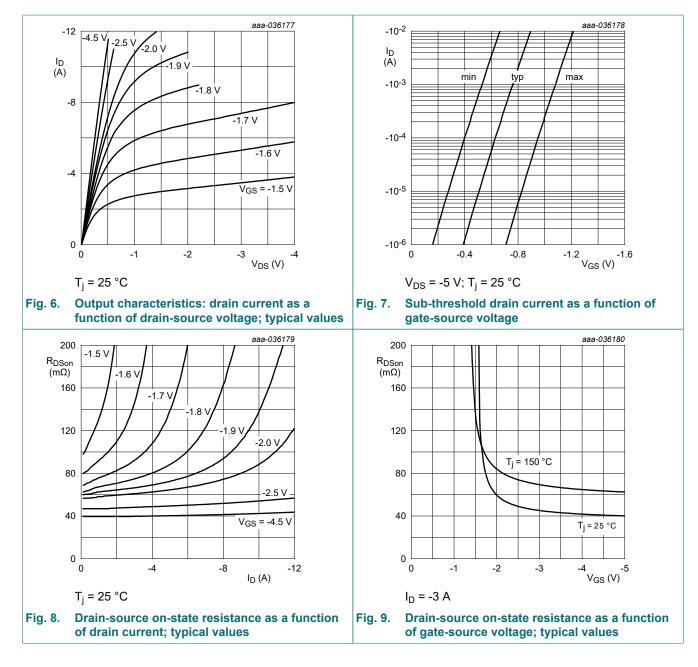
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².



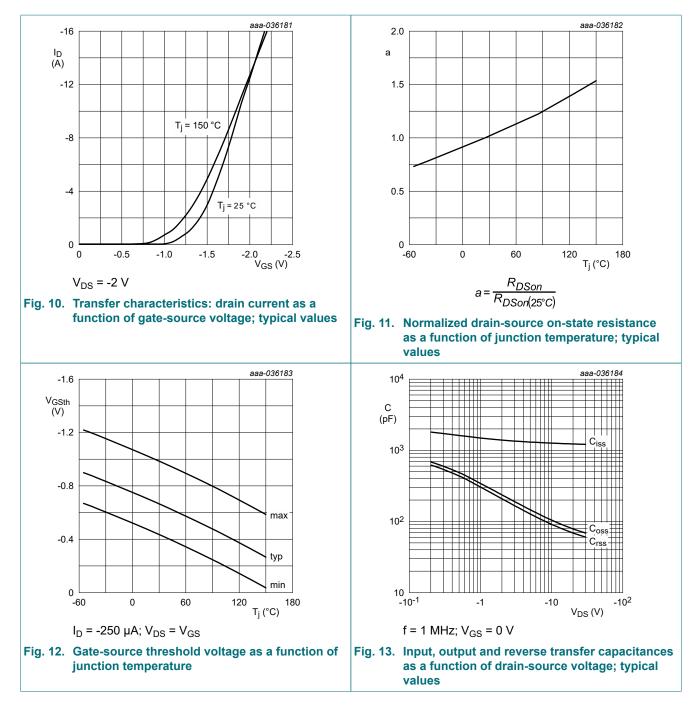
10. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C	-28	-	-	V
V _{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS} ; T_j = 25 °C	-0.45	-0.68	-1	V
I _{DSS}	drain leakage current	V _{DS} = -28 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μA
I _{GSS} gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA	
		V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state	V _{GS} = -4.5 V; I _D = -4 A; T _j = 25 °C	-	41	50	mΩ
	resistance	V _{GS} = -4.5 V; I _D = -4 A; T _j = 150 °C	-	63	80	mΩ
		V _{GS} = -2.5 V; I _D = -2.5 A; T _j = 25 °C	-	49	64	mΩ
		V _{GS} = -1.8 V; I _D = -0.5 A; T _j = 25 °C	-	67	105	mΩ
9 _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -4 A; T _j = 25 °C	-	12	-	S
R _G	gate resistance	f = 1 MHz	-	5.2	-	Ω
Dynamic ch	aracteristics	· · · ·				
Q _{G(tot)}	total gate charge	V _{DS} = -15 V; I _D = -4 A; V _{GS} = -4.5 V;	-	14	21	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	1.9	-	nC
Q _{GD}	gate-drain charge		-	3.7	-	nC
C _{iss}	input capacitance	V _{DS} = -15 V; f = 1 MHz; V _{GS} = 0 V;	-	1254	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	88	-	pF
C _{rss}	reverse transfer capacitance		-	77	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -15 V; I _D = -4 A; V _{GS} = -4.5 V;	-	4	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	10	-	ns
t _{d(off)}	turn-off delay time		-	42	-	ns
t _f	fall time		-	18	-	ns
Source-drai	n diode	· · ·	I			
V _{SD}	source-drain voltage	I _S = -1.9 A; V _{GS} = 0 V; T _j = 25 °C	-	-0.74	-1.2	V
t _{rr}	reverse recovery time	I _S = -1.9 A; dI _S /dt = 100 A/μs;	-	11.6	-	ns
Q _r	recovered charge	V _{GS} = -4.5 V; V _{DS} = -15 V; T _j = 25 °C	-	3.8	-	nC

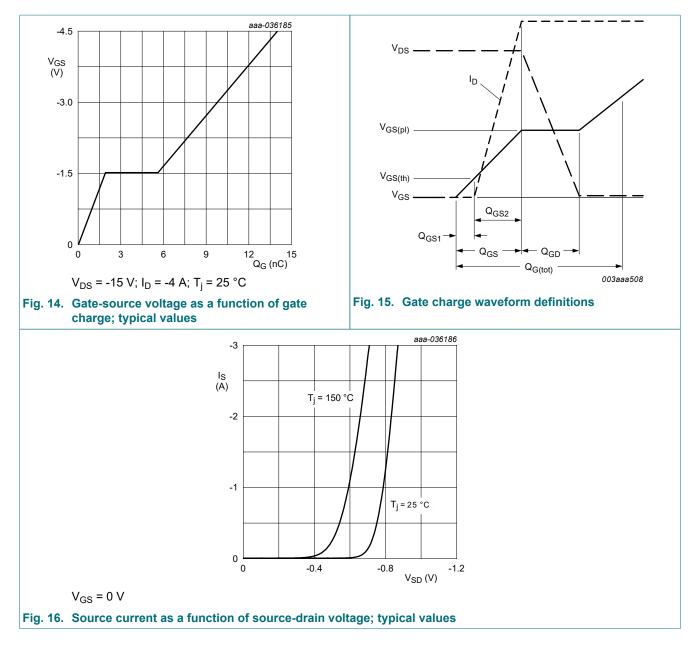
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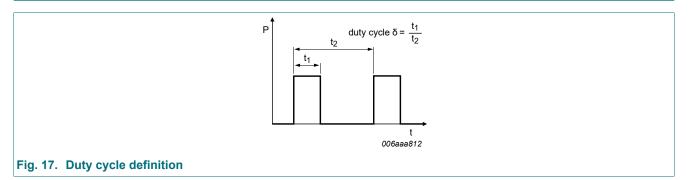
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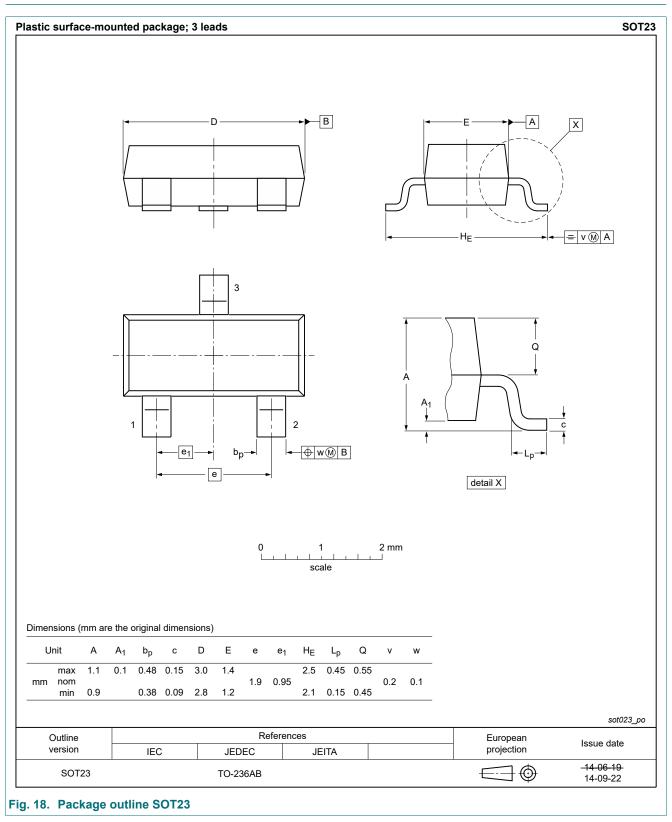
11. Test information



Quality information

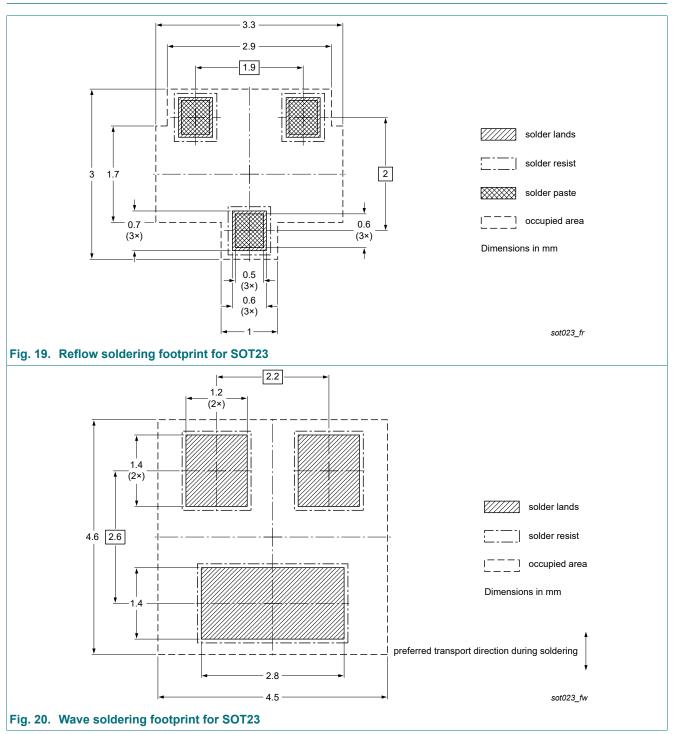
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101* - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



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13. Soldering



14. Revision history

Table 8. Revision history						
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes		
PMV41XPA v.2	20230712	Product data sheet	-	PMV41XPA v.1		
Modifications:	Change I _D condition	for one R _{DSon} parameter				
PMV41XPA v.1	20230306	Product data sheet	-	-		

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

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