

74LVT2244

3.3 V octal buffer/line driver with 30 Ω termination resistors;
3-state

Rev. 5 — 8 July 2024

Product data sheet

1. General description

The 74LVT2244 is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables (1 \overline{OE} and 2 \overline{OE}), each controlling four of the 3-state outputs. A HIGH on n \overline{OE} causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

The 74LVT2244 is designed with 30 Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

2. Features and benefits

- Octal bus interface
- 3-state buffers
- Wide supply voltage range from 2.7 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Output capability: +12 mA and -12 mA
- Direct interface with TTL levels
- No bus current loading when output is tied to 5 V bus
- Bus hold on data inputs
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Live insertion and extraction permitted
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT2244D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT2244PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

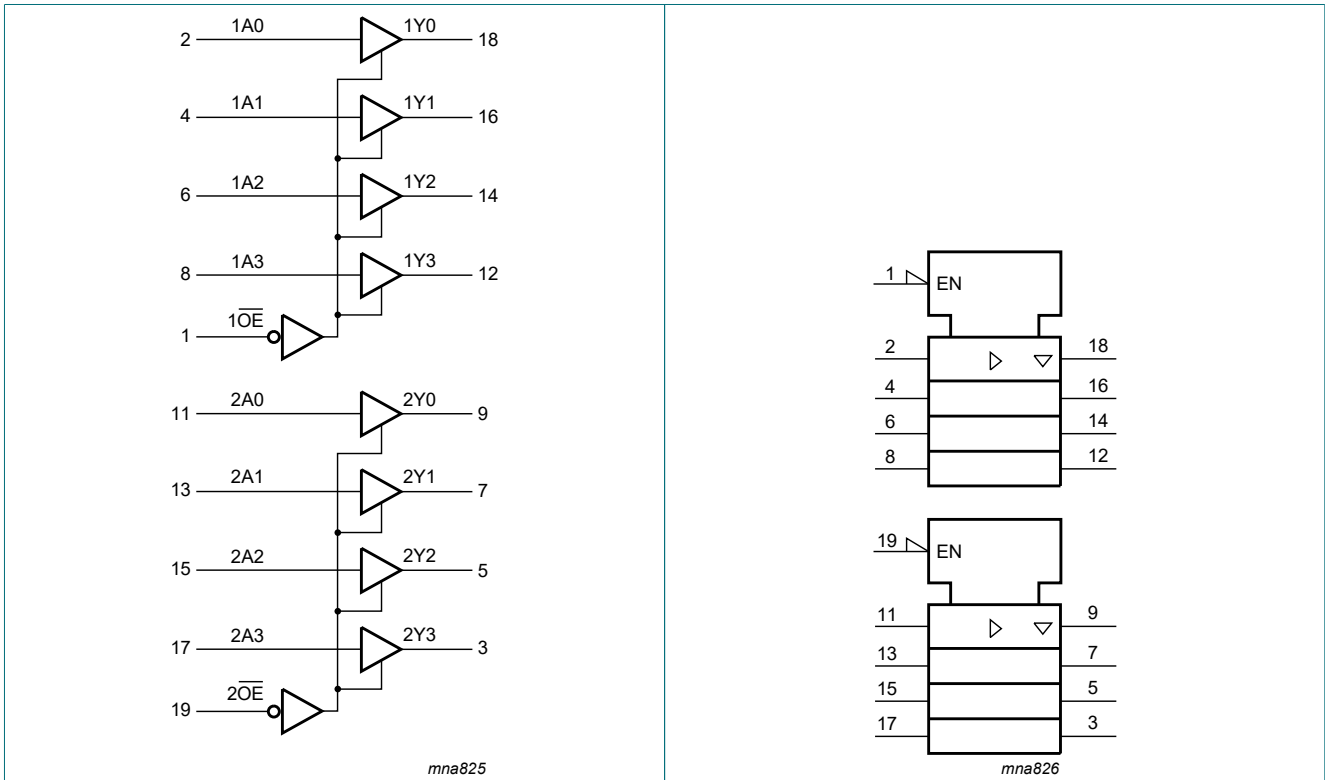


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

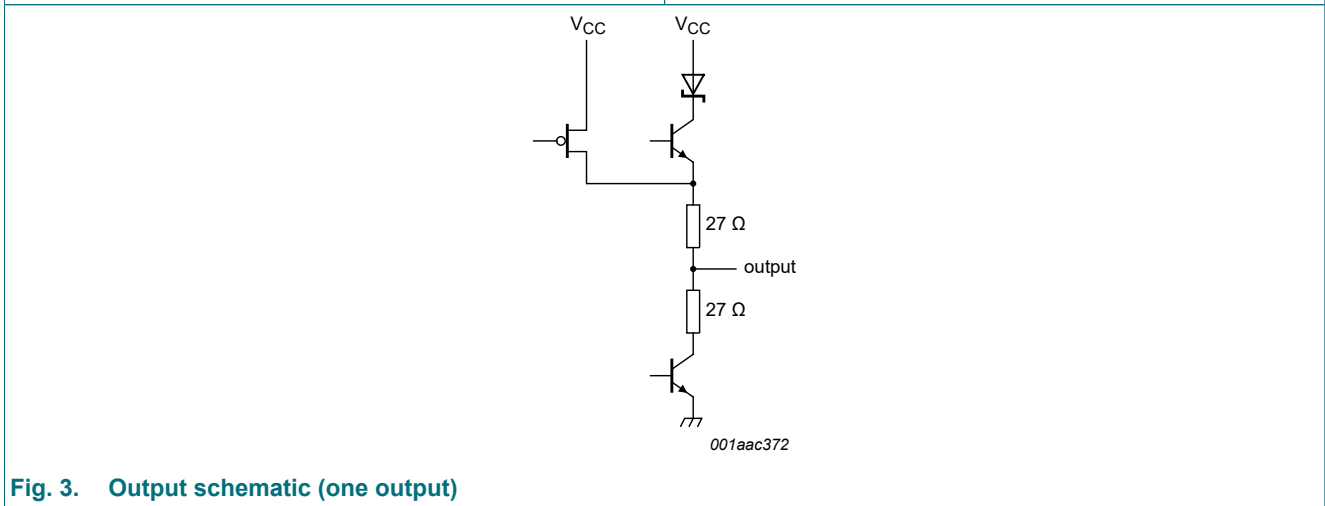
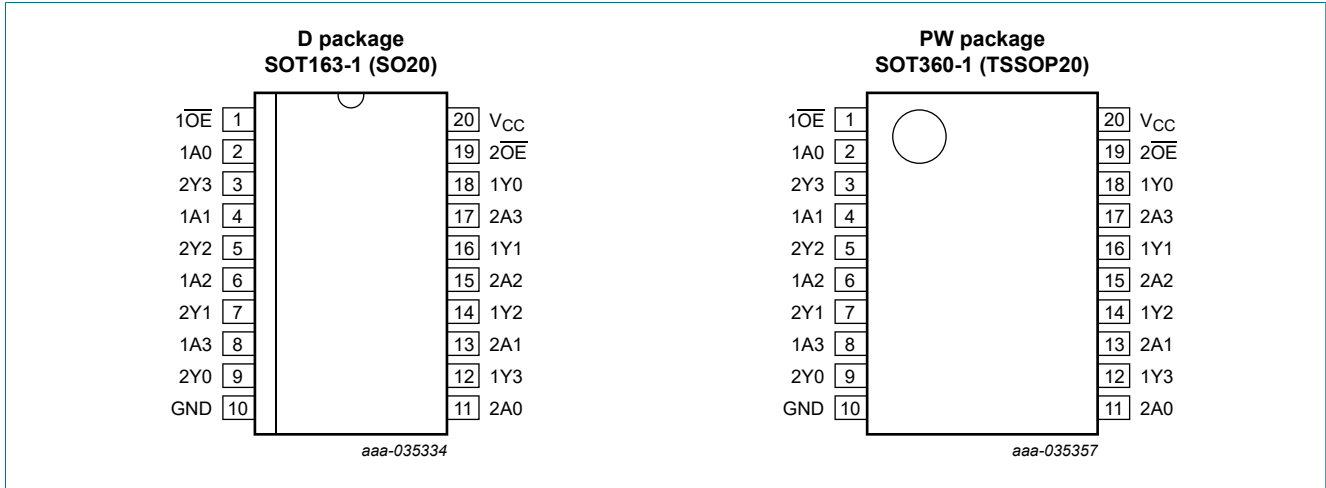


Fig. 3. Output schematic (one output)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3,	18, 16, 14, 12	data output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T_{stg}	storage temperature		-65	+150	$^{\circ}$ C
T_j	junction temperature	[2]	-	+150	$^{\circ}$ C
P_{tot}	total power dissipation	$T_{amb} = -40$ to $+85$ $^{\circ}$ C		500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 $^{\circ}$ C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-	-	-12	mA
I_{OL}	LOW-level output current		-	-	12	mA
T_{amb}	ambient temperature	in free-air	-40	-	+85	$^{\circ}$ C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-0.9	-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 3.0 V; I _{OH} = -12 mA	2.0	2.5	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 3.0 V; I _{OL} = 12 mA	-	-	0.8	V
I _I	input leakage current	all input pins				
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	1	10	μ A
		control pins				
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	\pm 0.1	\pm 1	μ A
		data pins [2]				
		V _{CC} = 3.6 V; V _I = V _{CC} V _{CC} = 3.6 V; V _I = 0 V	-	0.1	1	μ A
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	1	\pm 100	μ A
I _{BHL}	bus hold LOW current	V _{CC} = 3 V; V _I = 0.8 V [3]	75	150	-	μ A
I _{BHH}	bus hold HIGH current	V _{CC} = 3 V; V _I = 2.0 V	-	-150	-75	μ A
I _{BHLO}	bus hold LOW overdrive current	nAn input; V _{CC} = 0 V to 3.6 V; V _I = 3.6 V	500	-	-	μ A
I _{BHHO}	bus hold HIGH overdrive current	nAn input; V _{CC} = 0 V to 3.6 V; V _I = 3.6 V	-	-	-500	μ A
I _{EX}	external current	nYn output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	60	125	μ A
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} \leq 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; n \overline{OE} = don't care [4]	-	\pm 1	\pm 100	μ A
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL}				
		V _O = 3.0 V	-	1	5	μ A
		V _O = 0.5 V	-5	-1	-	μ A
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A				
		output HIGH	-	0.12	0.19	mA
		output LOW	-	3	12	mA
		outputs disabled [5]	-	0.12	0.19	mA
Δ I _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; one input at V _{CC} - 0.6 V and other inputs at V _{CC} or GND [6]	-	0.1	0.2	mA
C _I	input capacitance	V _I = 0 V or 3.0 V	-	4	-	pF
C _O	output capacitance	outputs disabled; V _O = 0 V or 3.0 V	-	7	-	pF

[1] All typical values are at T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V \pm 0.3 V a transition time of 100 μ s is permitted. This parameter is valid for T_{amb} = 25 °C only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

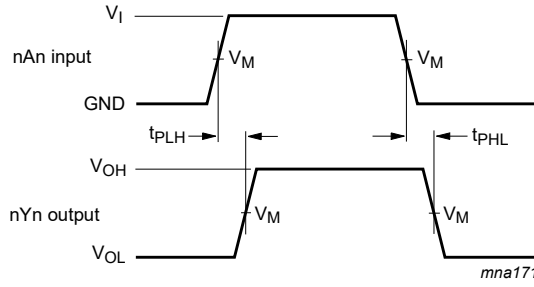
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$			Unit
			Min	Typ [1]	Max	
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn ; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	5.3	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1	2.9	4.4	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn ; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	4.4	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1	2.9	4.1	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nYn ; see Fig. 5				
		$V_{CC} = 2.7\text{ V}$	-	-	7.7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1	3.7	5.9	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nYn ; see Fig. 5				
		$V_{CC} = 2.7\text{ V}$	-	-	6.2	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.1	3.7	5.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nYn ; see Fig. 5				
		$V_{CC} = 2.7\text{ V}$	-	-	6.8	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.9	4.3	6.1	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nYn ; see Fig. 5				
		$V_{CC} = 2.7\text{ V}$	-	-	4.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.8	3.3	4.5	ns

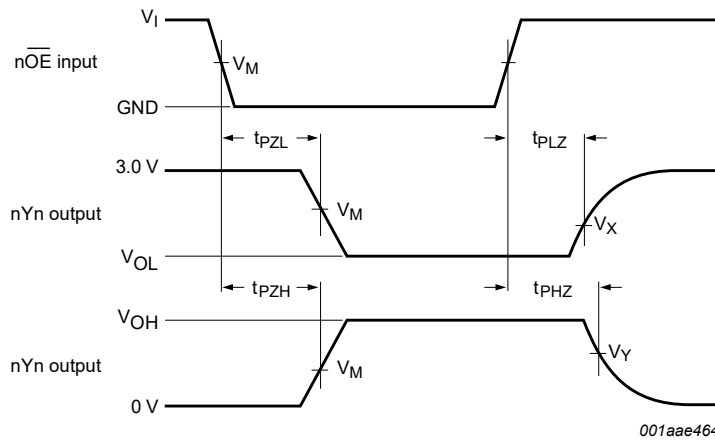
[1] All typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).
 VOL and VOH are typical voltage output levels that occur with the output load.

Fig. 4. Propagation delay input (nAn) to output (nYn) propagation delays



Measurement points are given in [Table 8](#).
 VOL and VOH are typical voltage output levels that occur with the output load.

Fig. 5. 3-state output enable and disable times

Table 8. Measurement points

Input	Output		
VM	VM	VX	VY
1.5 V	1.5 V	VOL + 0.3 V	VOH - 0.3 V

3.3 V octal buffer/line driver with 30 Ω termination resistors; 3-state

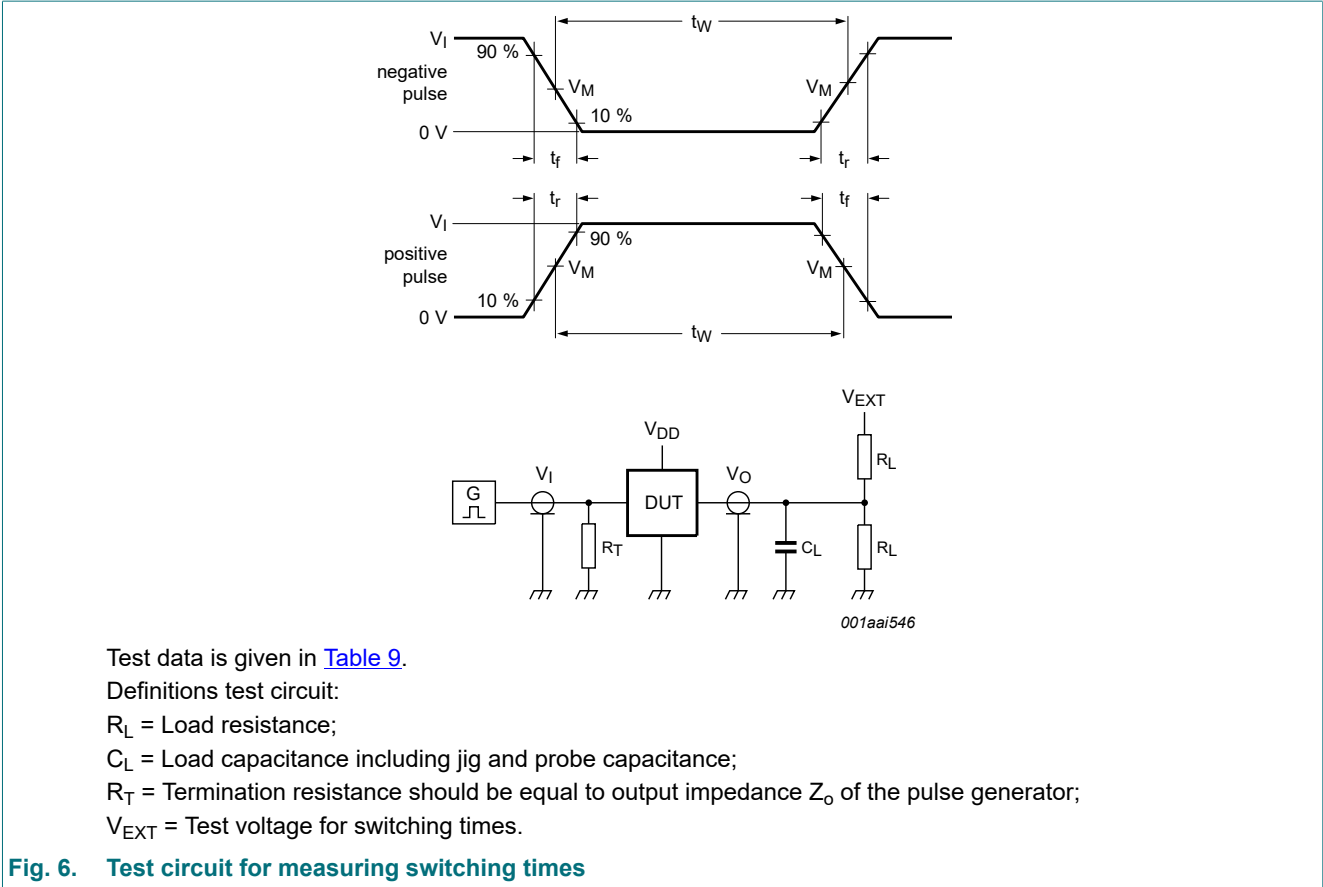


Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

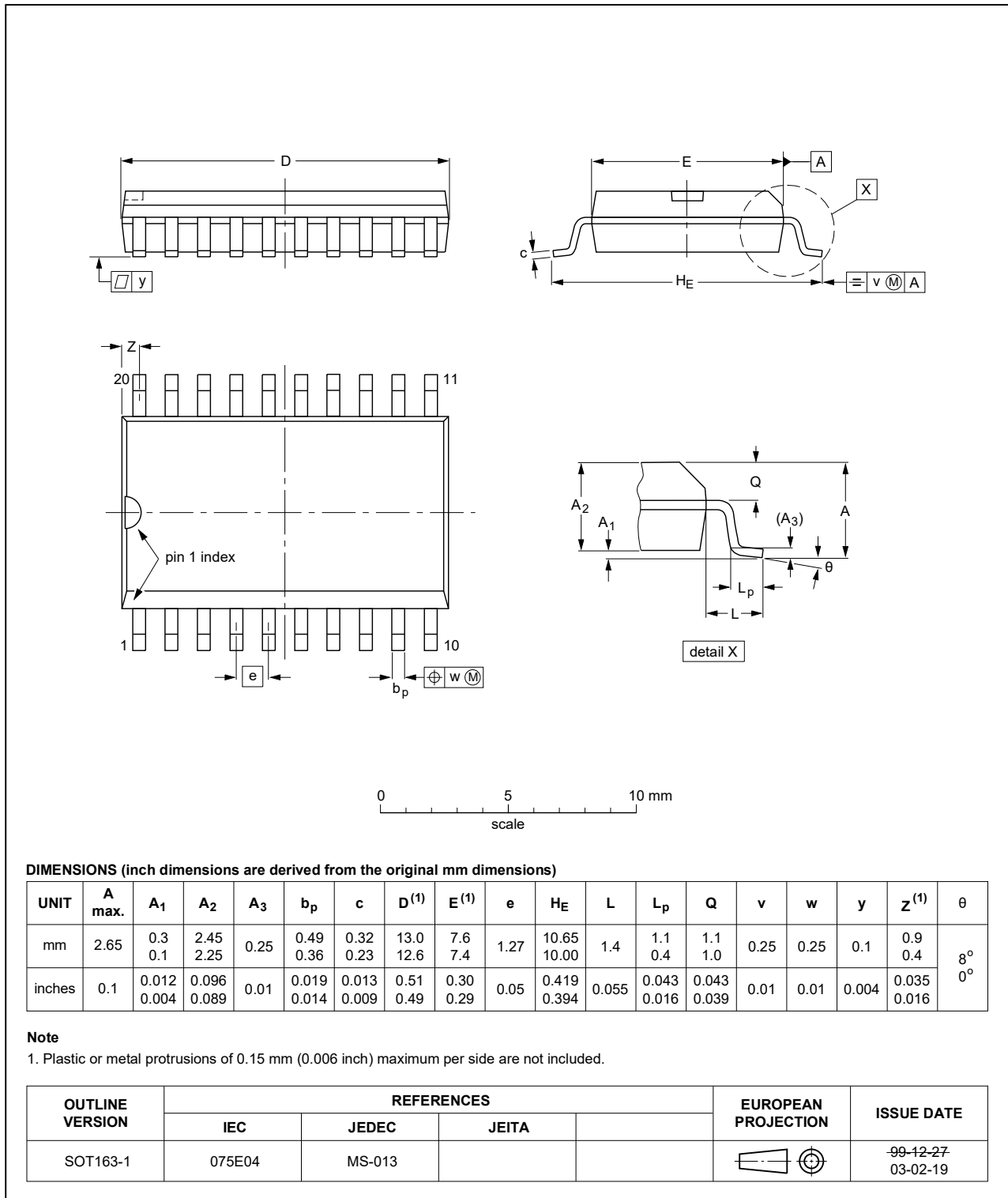


Fig. 7. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

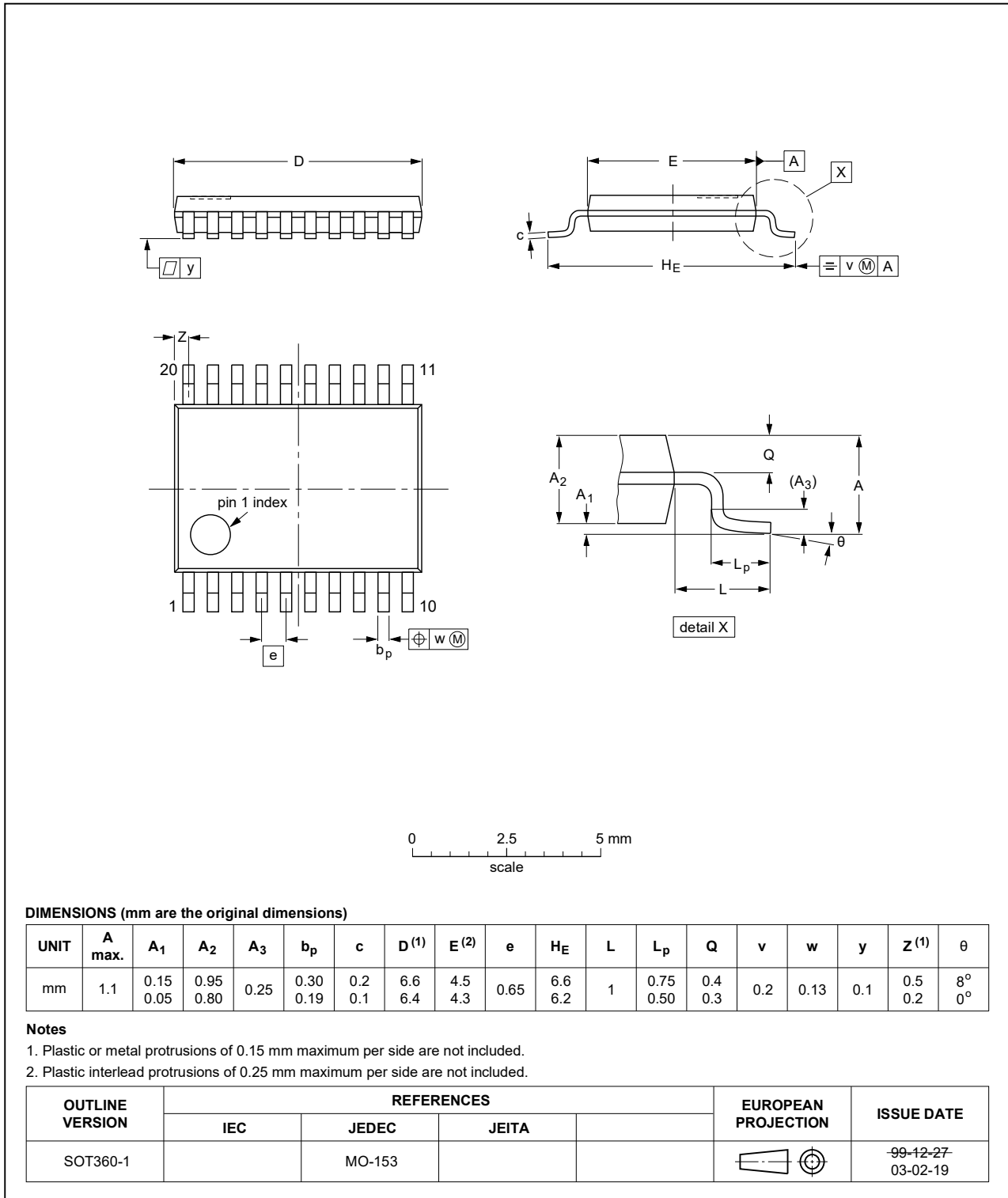


Fig. 8. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bi-polar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT2244 v.5	20240708	Product data sheet	-	74LVT2244 v.4
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVT2244 v.4	20210517	Product data sheet	-	74LVT2244 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74LVT2244DB (SOT339-1 / SSOP20) removed. Section 1 and Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation removed (errata). 			
74LVT2244 v.3	20160901	Product data sheet	-	74LVT2244 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 			
74LVT2244 v.2	19980219	Product specification	-	74LVT2244 v.1
74LVT2244 v.1	19960828	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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