Hex inverting Schmitt trigger Rev. 3 — 18 April 2024

1. General description

The 74VHC14; 74VHCT14 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74VHC14; 74VHCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features and benefits

- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - The 74VHC14 operates with CMOS input level
 - The 74VHCT14 operates with TTL input level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

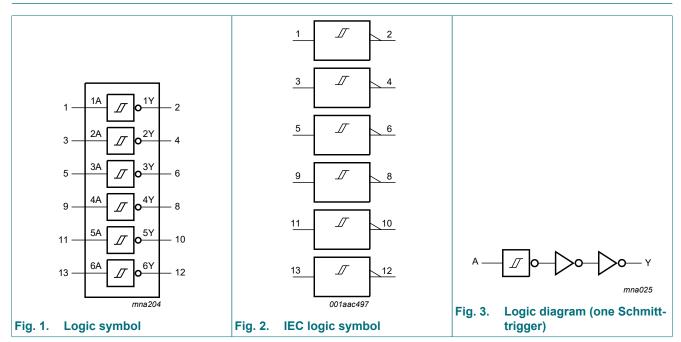
3. Ordering information

Table 1. Ordering information

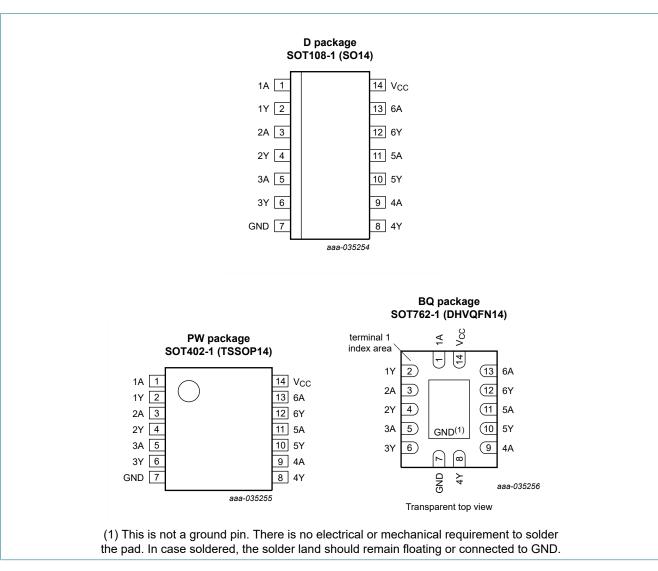
Type number	Package							
	Temperature range	ge Name Description						
74VHC14D 74VHCT14D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<u>SOT108-1</u>				
74VHC14PW 74VHCT14PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<u>SOT402-1</u>				
74VHC14BQ 74VHCT14BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	<u>SOT762-1</u>				

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4. Functional diagram



5. Pinning information



5.1. Pinning

5.2. Pin description

Table 2. Pin description							
Symbol	Pin	Description					
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input					
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output					
GND	7	ground (0 V)					
V _{CC}	14	supply voltage					

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	nY
L	Н
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
VI	input voltage			-0.5	+7.0	V
I _{IK}	input clamping current	V ₁ < -0.5 V	[1]	-20	-	mA
I _{ОК}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	[1]	-20	+20	mA
I _O	output current	V_{O} = -0.5 V to (V _{CC} + 0.5 V)		-25	+25	mA
I _{CC}	supply current			-	+75	mA
I _{GND}	ground current			-75	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
 For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Op	erating conditions					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74VHC14				•		
V _{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
74VHCT14			·			
V _{CC}	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Мах	Min	Max	1
74VHC1	4							1	1	
011	$V_{I} = V_{T+}$ or V_{T-}									
	output voltage	I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_{I} = V_{T+}$ or V_{T-}								
	output voltage	I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
CI	input capacitance		-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF
74VHCT	14			1					1	1
V _{OH}	HIGH-level	$V_{I} = V_{T+}$ or V_{T-}								
	output voltage	I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_{I} = V_{T+}$ or V_{T-}								
	output voltage	I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
ΔI _{CC}	additional supply current	per input pin; $V_1 = V_{CC} - 2.1 V$; other pins at V_{CC} or GND; $I_0 = 0 A$; $V_{CC} = 4.5 V$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
CI	input capacitance		-	3	10	-	10	-	10	pF
C _O	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Мах	Min	Max	
74VHC1	4	11			I		1	I		
t _{pd}	propagation	nA to nY; see Fig. 4 [2]								
	delay	V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.3	12.8	1.0	15.0	1.0	16.0	ns
		C _L = 50 pF	-	5.8	16.3	1.0	18.0	1.0	20.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.2	8.6	1.0	10.0	1.0	11.0	ns
		C _L = 50 pF	-	4.2	10.6	1.0	12.0	1.0	13.5	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_i = \text{GND to } V_{\text{CC}}$ [3]	-	10	-	-	-	-	-	pF
74VHCT	14								•	
t _{pd}	propagation	nA to nY; see Fig. 4 [2]								
	delay	V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.0	7.0	1.0	8.0	1.0	9.0	ns
		C _L = 50 pF	-	5.4	8.0	1.0	9.0	1.0	10.0	ns
C _{PD}	power dissipation	$f_i = 1 \text{ MHz}; V_1 = \text{GND to } V_{\text{CC}}$ [3]	-	12	-	-	-	-	-	pF

Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[1] [2]

capacitance

 t_{pd} is the same as t_{PLH} and t_{PHL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: [3]

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

 C_L = output load capacitance in pF;

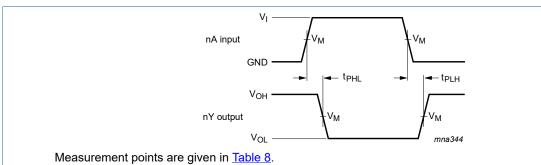
V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

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10.1. Waveforms and test circuit

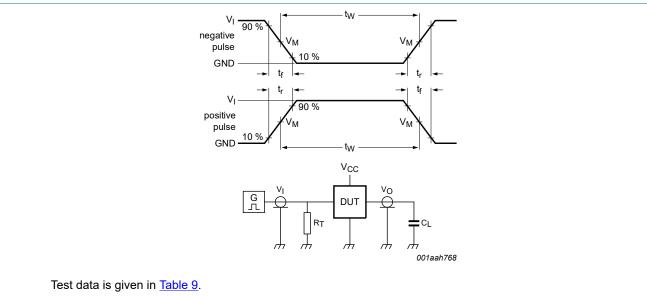


 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Input to output propagation delays

Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74VHC14	0.5 x V _{CC}	0.5 x V _{CC}
74VHCT14	1.5 V	0.5 x V _{CC}



Definitions test circuit:

- R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator
- C_L = Load capacitance including jig and probe capacitance

Fig. 5. Test circuit for measuring switching times

Table 9. Test data Type	Input		Load	Test
	VI	t _r , t _f	CL	
74VHC14	V _{CC}	≤ 3.0 ns	50 pF, 15 pF	t _{PLH} , t _{PHL}
74VHCT14	3.0 V	≤ 3.0 ns	50 pF, 15 pF	t _{PLH} , t _{PHL}

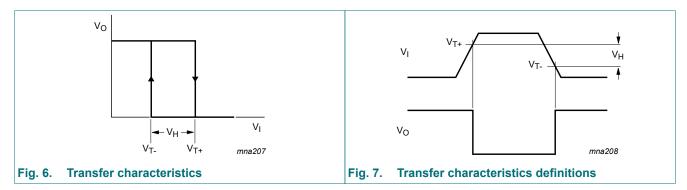
11. Transfer characteristics

Table 10. Transfer characteristics

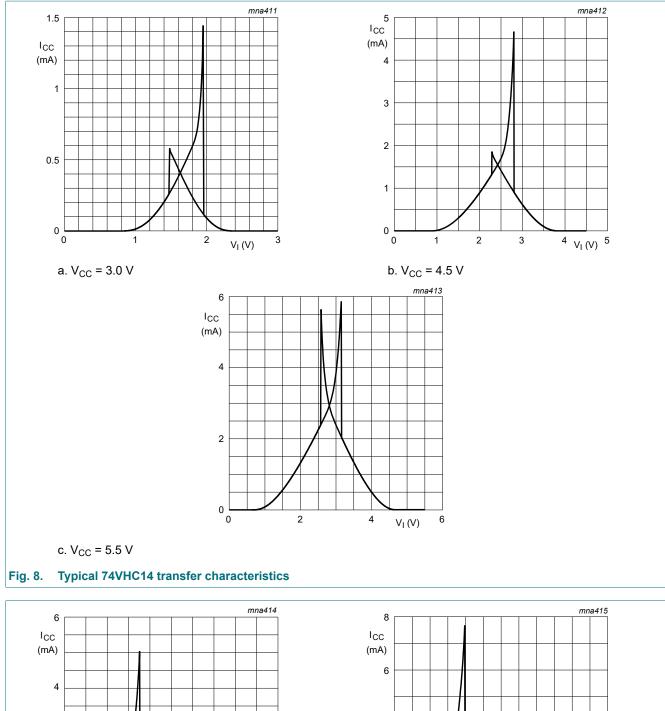
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Fig. 6 and Fig. 7.

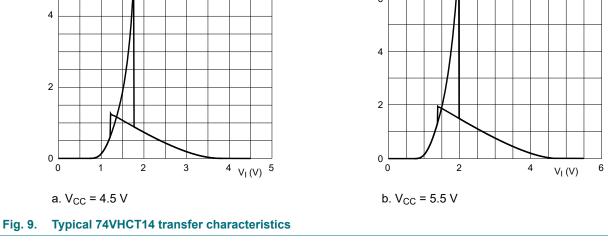
Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Мах	Min	Max	
74VHC1	4	1		I	1			1	1	
V _{T+}	positive-going	V _{CC} = 3.0 V	-	-	2.2	-	2.2	-	2.2	V
	threshold voltage	V _{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
	Voltage	V _{CC} = 5.5 V	-	-	3.85	-	3.85	-	3.85	V
V _{T-}	negative-going	V _{CC} = 3.0 V	0.9	-	-	0.9	-	0.9	-	V
	threshold voltage	V _{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
	voltage	V _{CC} = 5.5 V	1.65	-	-	1.65	-	1.65	-	V
V _H	hysteresis	V _{CC} = 3.0 V	0.3	-	1.2	0.3	1.2	0.25	1.2	V
	voltage	V _{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.35	1.4	V
		V _{CC} = 5.5 V	0.5	-	1.6	0.5	1.6	0.45	1.6	V
74VHCT	14							1		
V _{T+}	positive-going	V _{CC} = 4.5 V	-	-	1.9	-	1.9	-	1.9	V
	threshold voltage	V _{CC} = 5.5 V	-	-	2.1	-	2.1	-	2.1	V
V _{T-}	negative-going	V _{CC} = 4.5 V	0.5	-	-	0.5	-	0.5	-	V
	threshold voltage	V _{CC} = 5.5 V	0.6	-	-	0.6	-	0.6	-	V
V _H	hysteresis	V _{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.35	1.4	V
v	voltage	V _{CC} = 5.5 V	0.4	-	1.5	0.4	1.5	0.35	1.5	V

11.1. Transfer characteristics waveforms



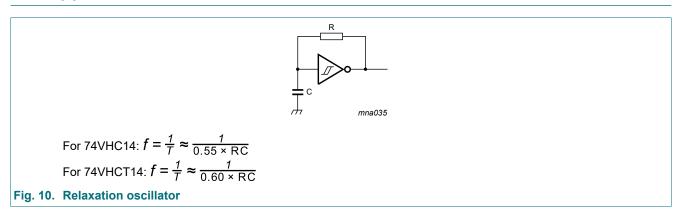
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12. Application information



74VHC_VHCT14

13. Package outline

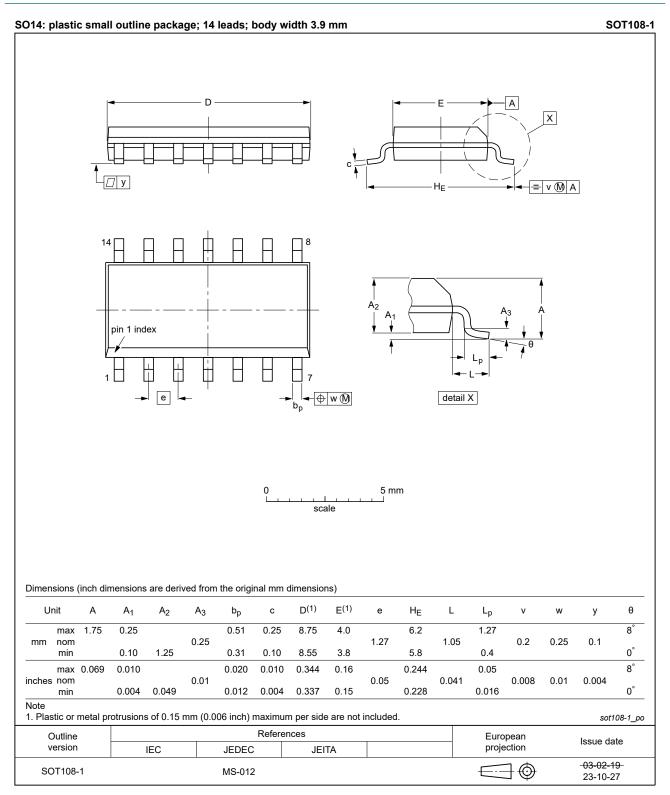


Fig. 11. Package outline SOT108-1 (SO14)

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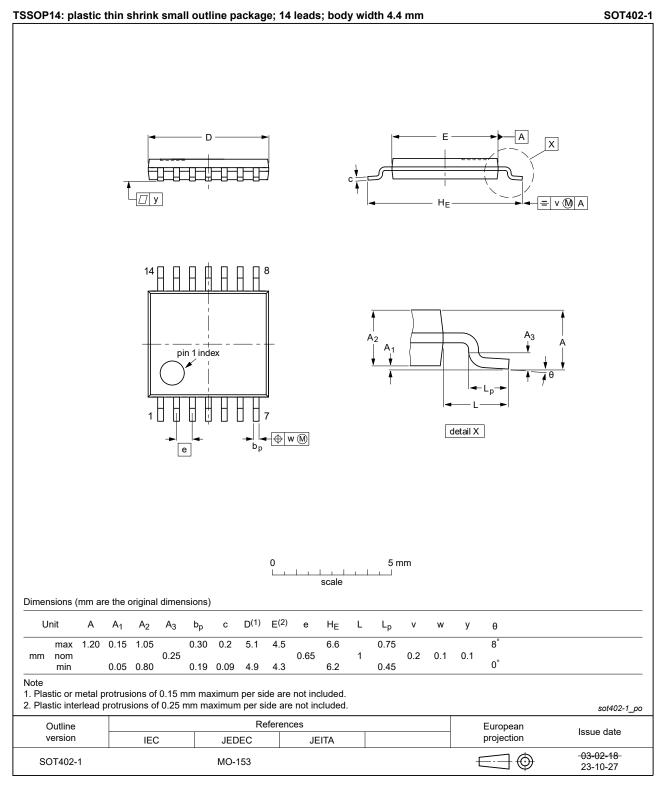


Fig. 12. Package outline SOT402-1 (TSSOP14)

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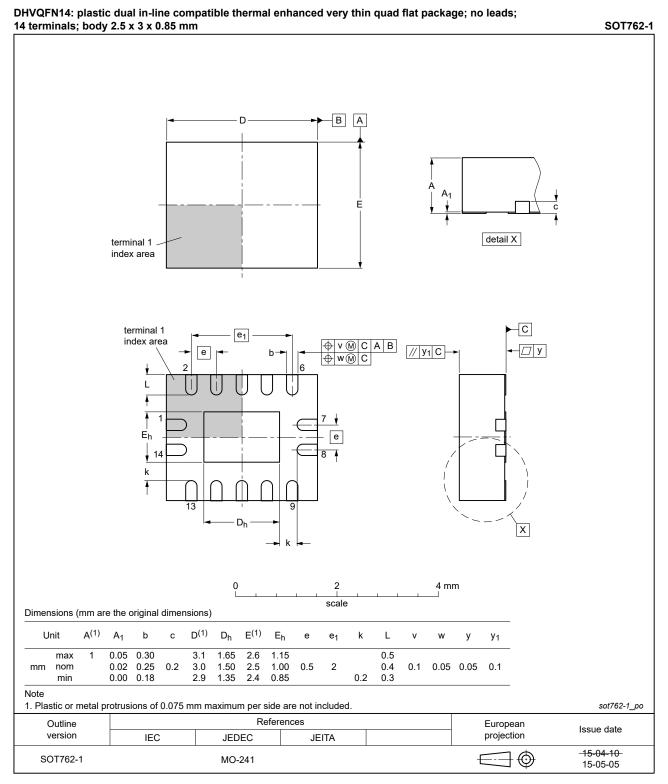


Fig. 13. Package outline SOT762-1 (DHVQFN14)

14. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74VHC_VHCT14 v.3	20240418	Product data sheet	-	74VHC_VHCT14 v.2				
Modifications:	and MO-153.	Fig. 11, Fig. 12: Aligned SO and TSSOP package outline drawings to JEDEC MS-012and MO-153.Section 2: ESD specification updated according to the latest JEDEC standard.						
74VHC_VHCT14 v.2	20221101	Product data sheet	-	74VHC_VHCT14 v.1				
Modifications:	of Nexperia. Legal texts have <u>Section 7</u>: Deray 	his data sheet has been n re been adapted to the ne ating values for P _{tot} total p ge outline drawing of SOT	ew company name	pdated.				
74VHC_VHCT14 v.1	20090817	Product data sheet	-	-				

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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