



PESD5V0U5BV

Ultra low capacitance bidirectional fivefold ESD protection array

28 December 2022

Product data sheet

1. General description

Ultra low capacitance bidirectional fivefold ElectroStatic Discharge (ESD) protection array in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package, designed to protect up to five signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of up to five lines
- ESD protection up to 10 kV
- Ultra low diode capacitance: $C_d = 2.9$ pF
- IEC 61000-4-2; level 4 (ESD)
- Ultra low leakage current: $I_{RM} = 5$ nA

3. Applications

- Computers and peripherals
- Portable electronics
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems

4. Quick reference data

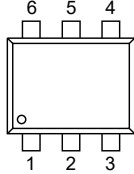
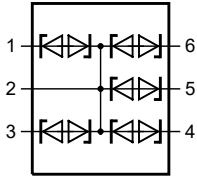
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25$ °C	-	-	5	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	[1]	2.9	3.5	pF

[1] Measured from pin 1, 3, 4, 5 or 6 to pin 2.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p style="text-align: center;">SOT666</p>	 <p style="text-align: right;"><small>006aab346</small></p>
2	CC	common cathode		
3	K2	cathode (diode 2)		
4	K3	cathode (diode 3)		
5	K4	cathode (diode 4)		
6	K5	cathode (diode 5)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0U5BV	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	SOT666

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0U5BV	G7

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[1] [2]	-	10	kV
		MIL-STD-883; human body model (HBM)	[1] [2]	-	8	V

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1, 3, 4, 5 or 6 to pin 2.

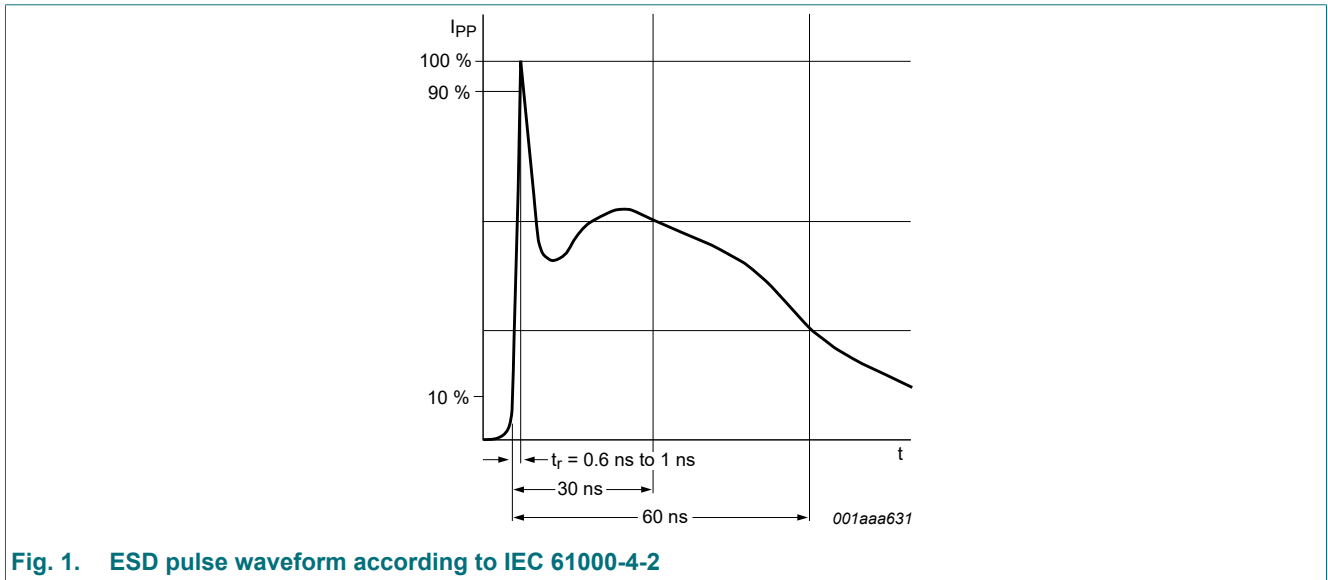


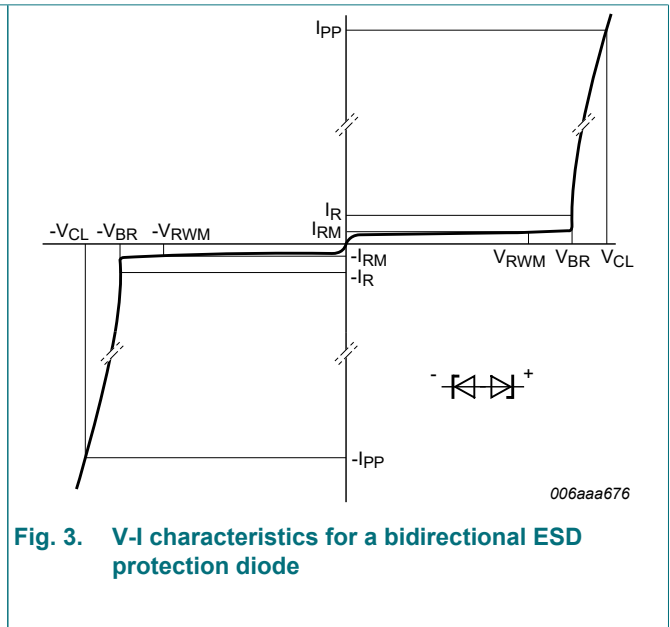
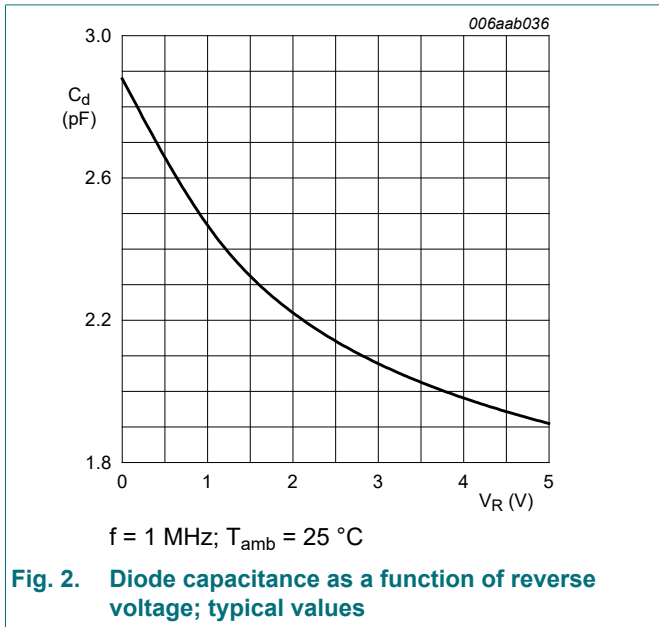
Fig. 1. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	5	V
V_{BR}	breakdown voltage	$I_R = 5\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	5.5	6.5	9.5	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	5	100	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	2.9	3.5	pF
		$f = 1\text{ MHz}; V_R = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.9	-	pF
R_{diff}	differential resistance	$I_R = 1\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	100	Ω

[1] Measured from pin 1, 3, 4, 5 or 6 to pin 2.



Ultra low capacitance bidirectional fivefold ESD protection array

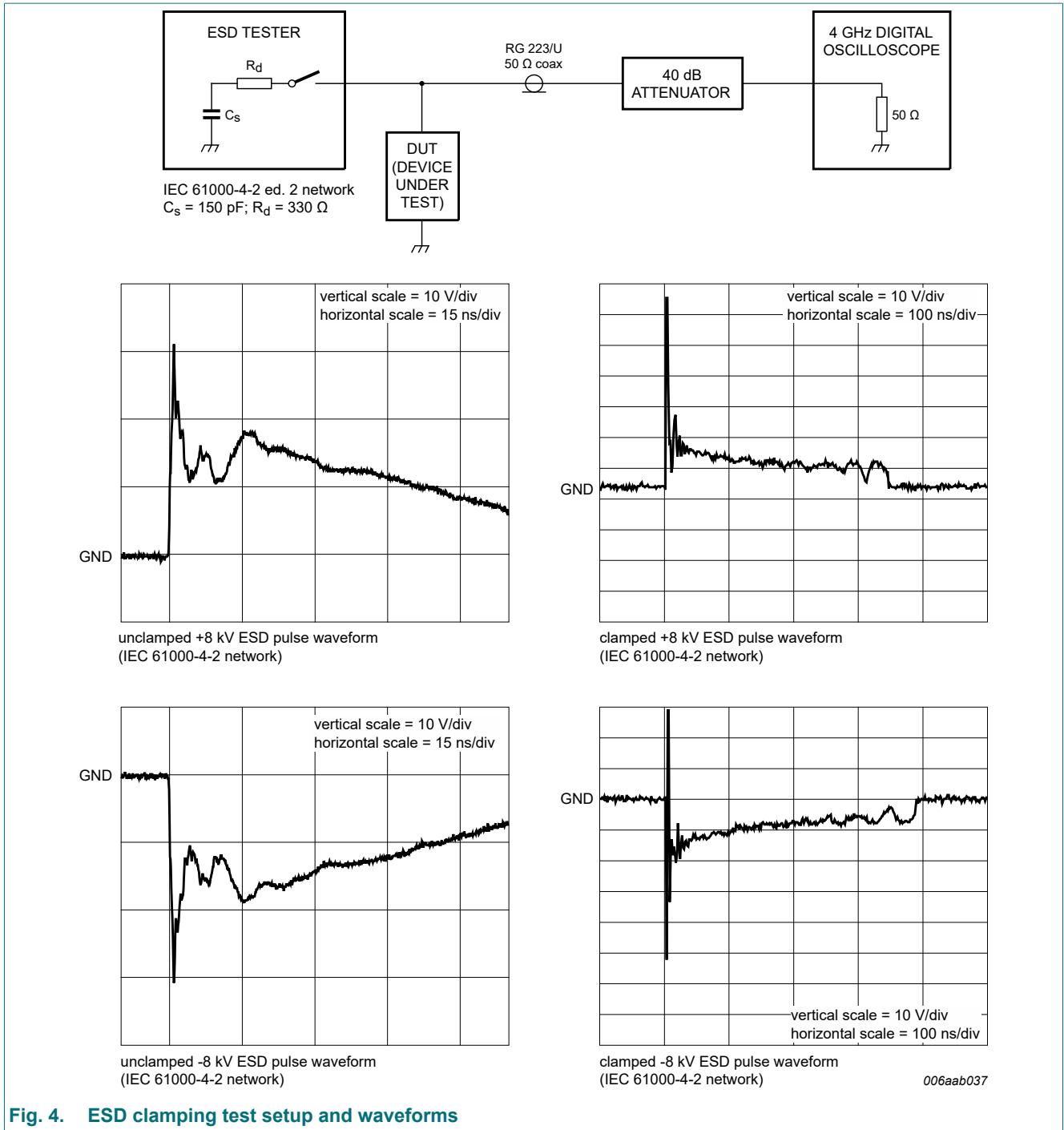


Fig. 4. ESD clamping test setup and waveforms

10. Application information

The device is designed for the protection of up to five bidirectional data or signal lines from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground.

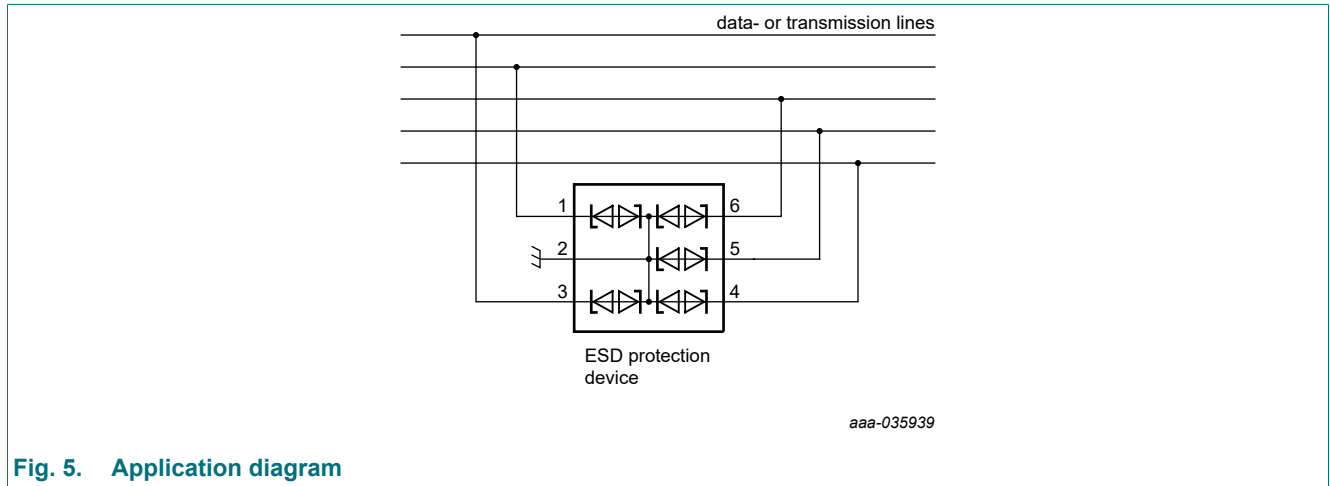


Fig. 5. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

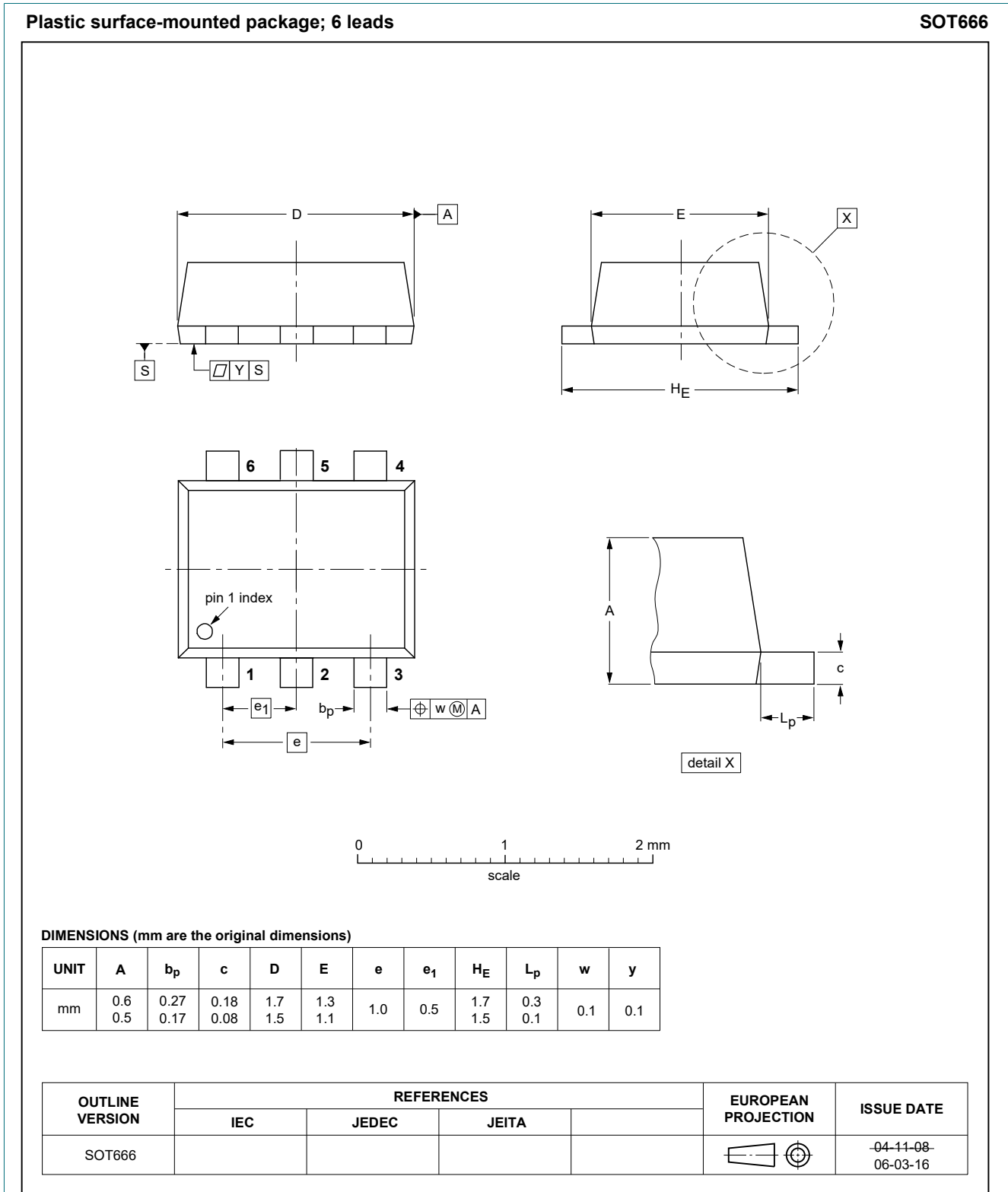


Fig. 6. Package outline SOT666

12. Soldering

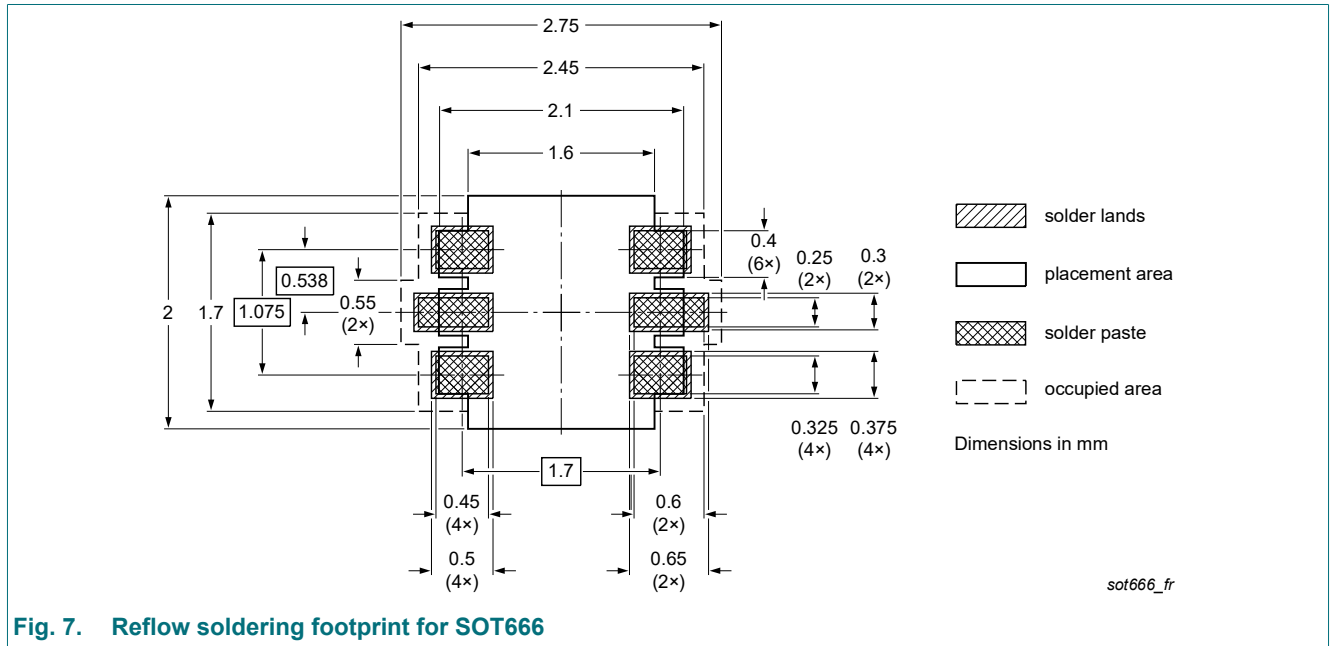


Fig. 7. Reflow soldering footprint for SOT666

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U5BV v.2	20221228	Product data sheet	-	PESD5V0U5BF_PESD5V0U5BV_1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia Legal texts have been adapted to the new company name where appropriate Family data sheet reduced to single type data sheet Product changed to non-automotive qualification 			
PESD5V0U5BF_PESD5V0U5BV_1	20080815	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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