



PUMH9-Q

50 V, 100 mA NPN/NPN resistor-equipped double transistor;
R1 = 10 kΩ, R2 = 47 kΩ

7 October 2021

Product data sheet

1. General description

NPN/NPN Resistor-Equipped double Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

PNP/PNP complement: PUMB9-Q

NPN/PNP complement: PUMD9-Q

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Digital application in automotive and industrial segments
- Cost-saving alternative for BC847-Q series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

Table 1. Quick reference data

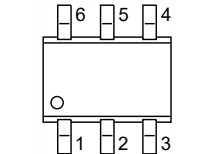
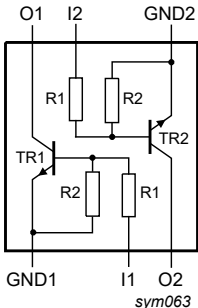
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
R1	bias resistor 1	[1]	7	10	13	kΩ
R2/R1	bias resistor ratio	[1]	3.7	4.7	5.7	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 TSSOP6 (SOT363)	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMH9-Q	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMH9-Q	H%9

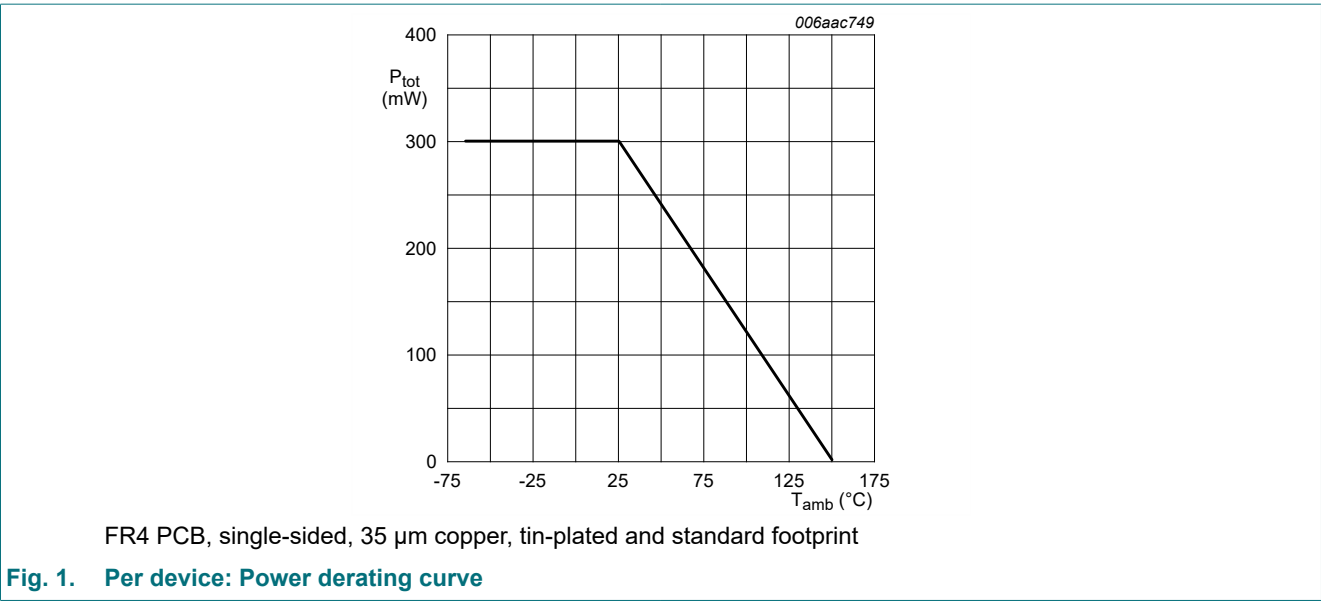
[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	6	V
V _I	input voltage	positive		-	40	V
		negative		-	-6	V
I _O	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	300	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.

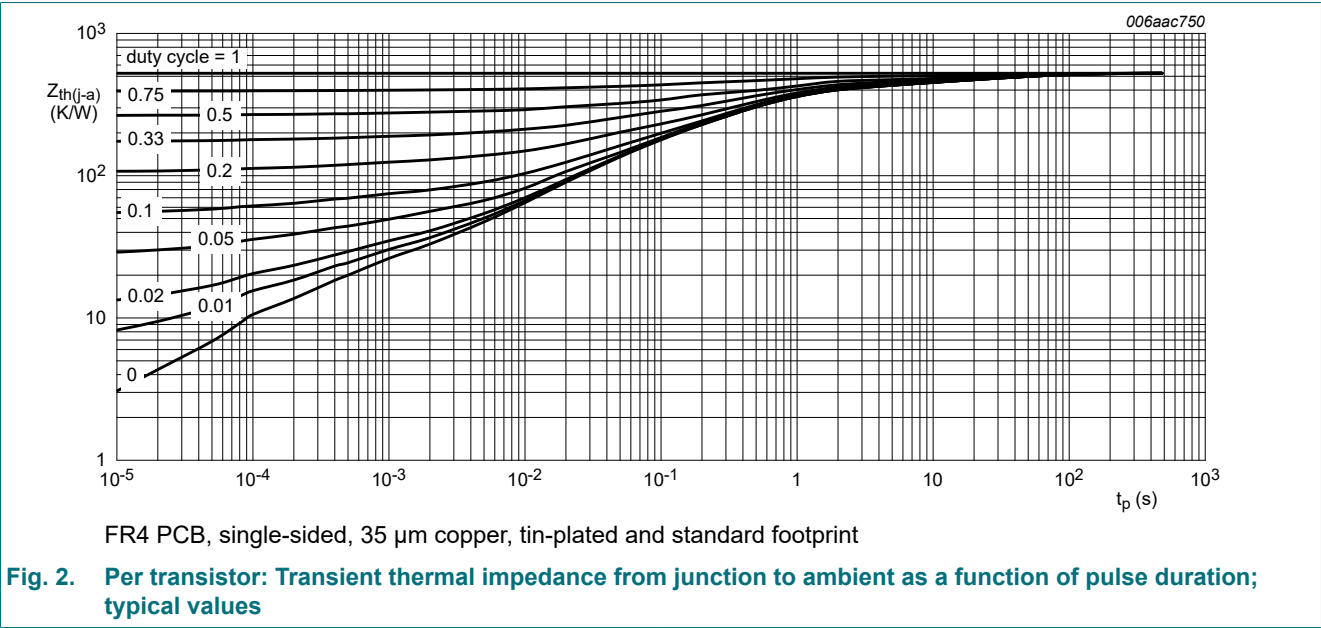


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.



10. Characteristics

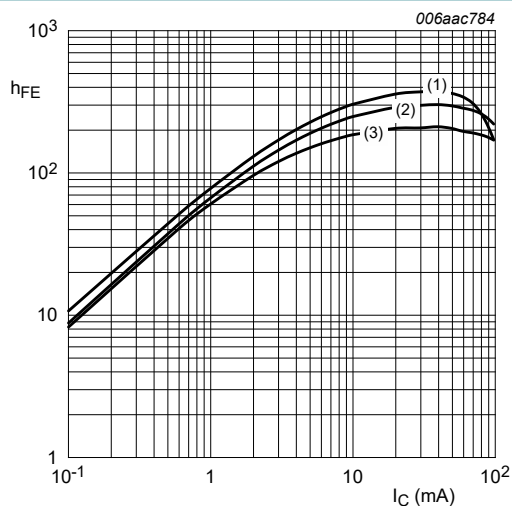
Table 7. Characteristics

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\text{ }\mu\text{A}$; $I_E = 0\text{ A}$	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2\text{ mA}$; $I_B = 0\text{ A}$	50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$	-	-	100	nA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_J = 150\text{ °C}$	-	-	5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$	-	-	150	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 5\text{ mA}$	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}$; $I_B = 0.25\text{ mA}$	-	-	100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 100\text{ }\mu\text{A}$	-	0.7	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 1\text{ mA}$	1.4	0.8	-	V
R1	bias resistor 1		[1]	7	10	kΩ
R2/R1	bias resistor ratio		[1]	3.7	4.7	
C_c	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$	-	-	2.5	pF
f_T	transition frequency	$V_{CE} = 5\text{ V}$; $I_C = 10\text{ mA}$; $f = 100\text{ MHz}$	[2]	-	230	MHz

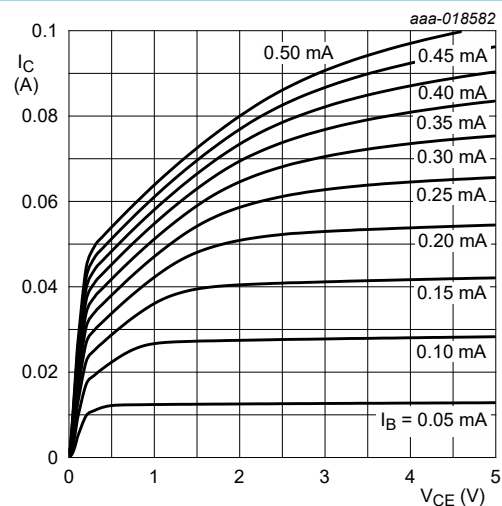
[1] See "Section 11: Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor



$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig. 3. DC current gain as a function of collector current; typical values



$T_{amb} = 25\text{ °C}$

Fig. 4. Collector current as a function of collector-emitter voltage; typical values

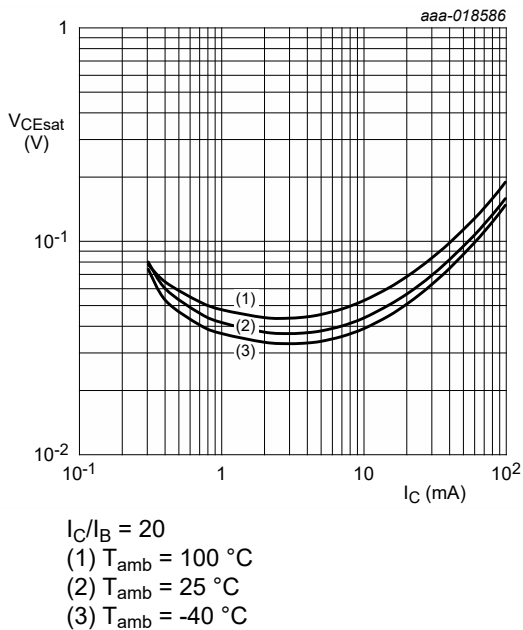


Fig. 5. Collector-emitter saturation voltage as a function of collector current; typical values

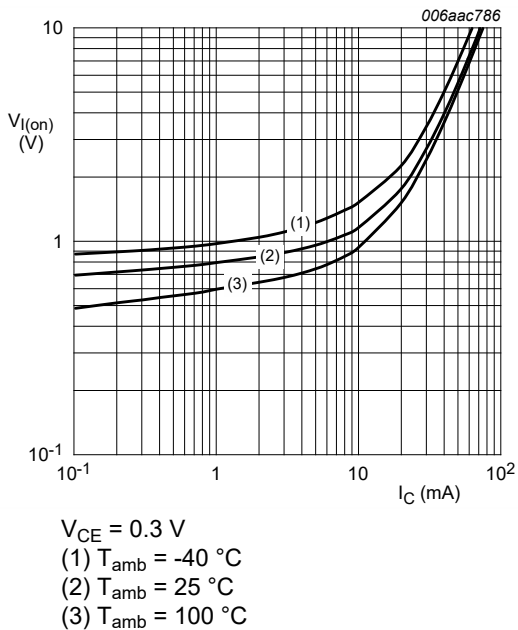


Fig. 6. On-state input voltage as a function of collector current; typical values

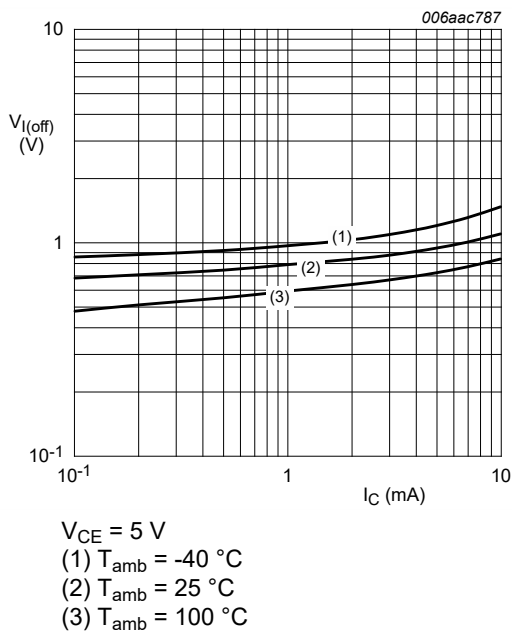


Fig. 7. Off-state input voltage as a function of collector current; typical values

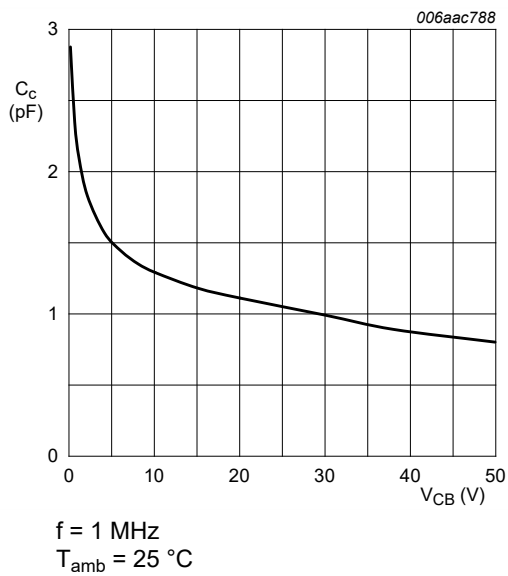
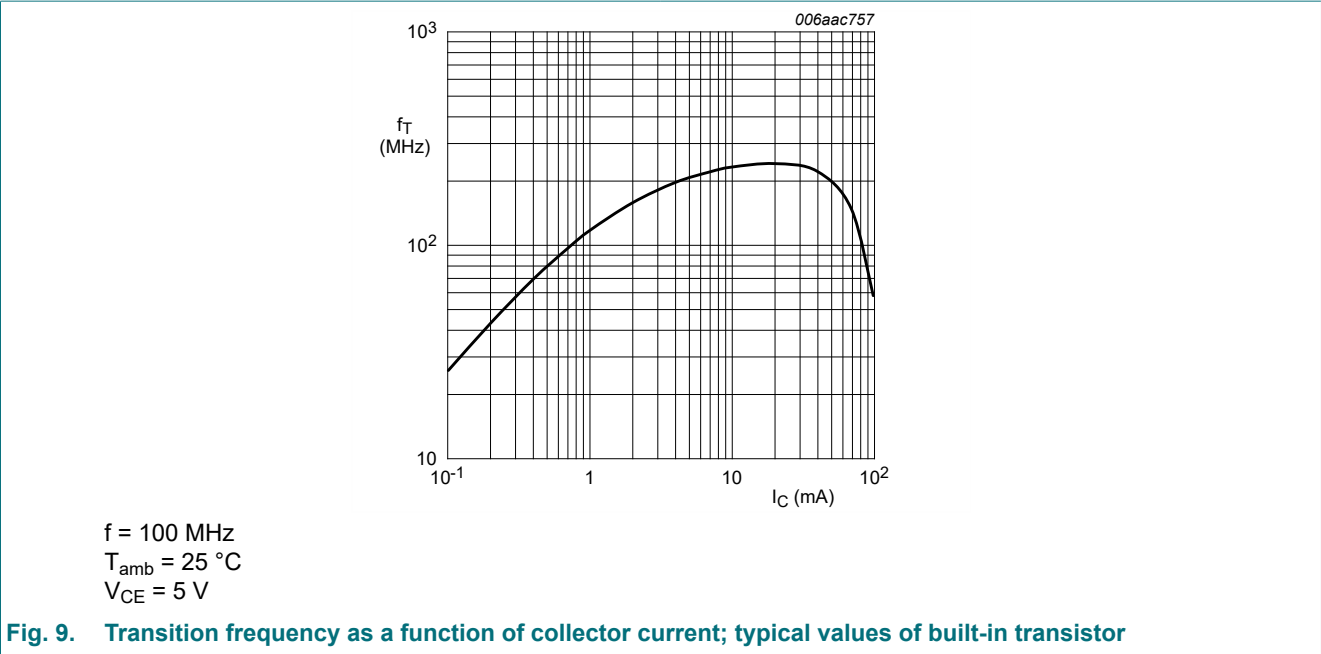


Fig. 8. Collector capacitance as a function of collector-base voltage; typical values

50 V, 100 mA NPN/NPN resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

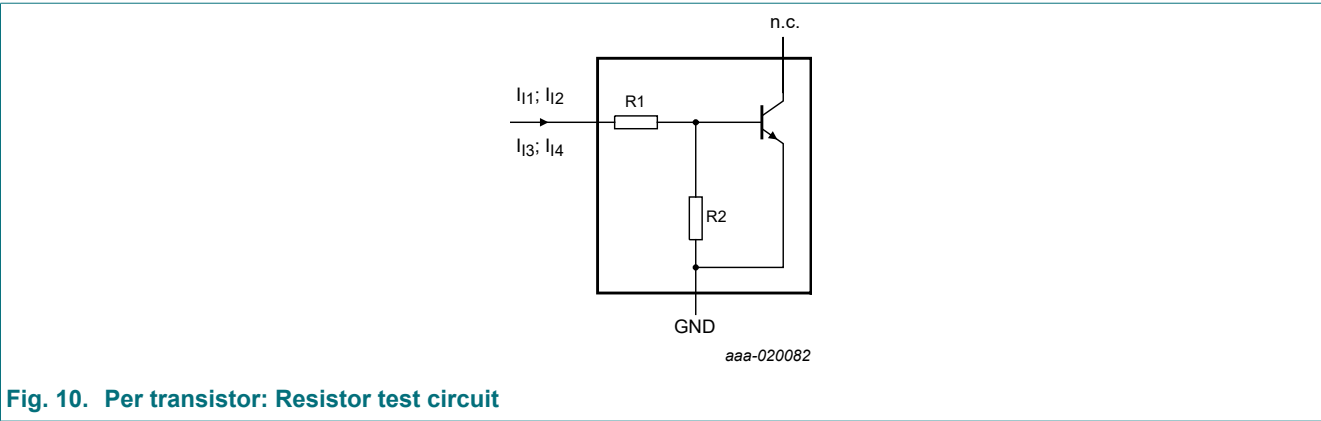
Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

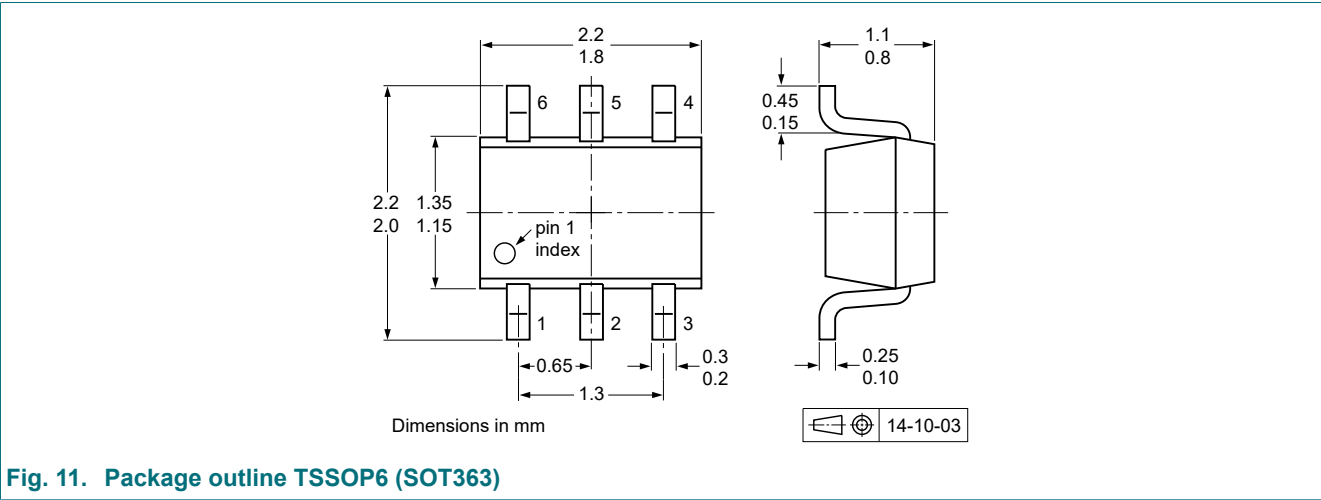


Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I _{I1}	I _{I2}	I _{I3}	I _{I4}
Per transistor						
PUMH9-Q	10	47	90 μA	140 μA	-55 μA	-105 μA

12. Package outline



13. Soldering

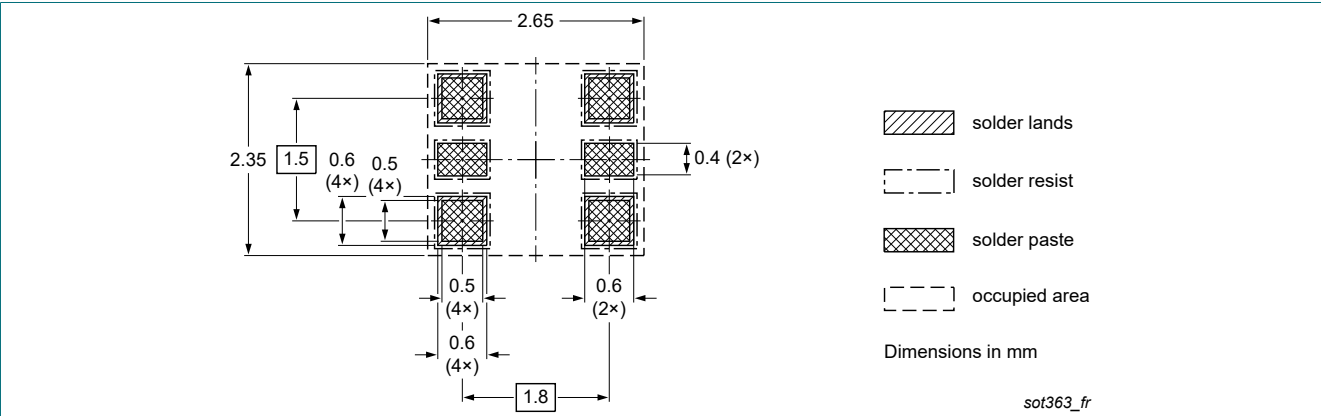


Fig. 12. Reflow soldering footprint for TSSOP6 (SOT363)

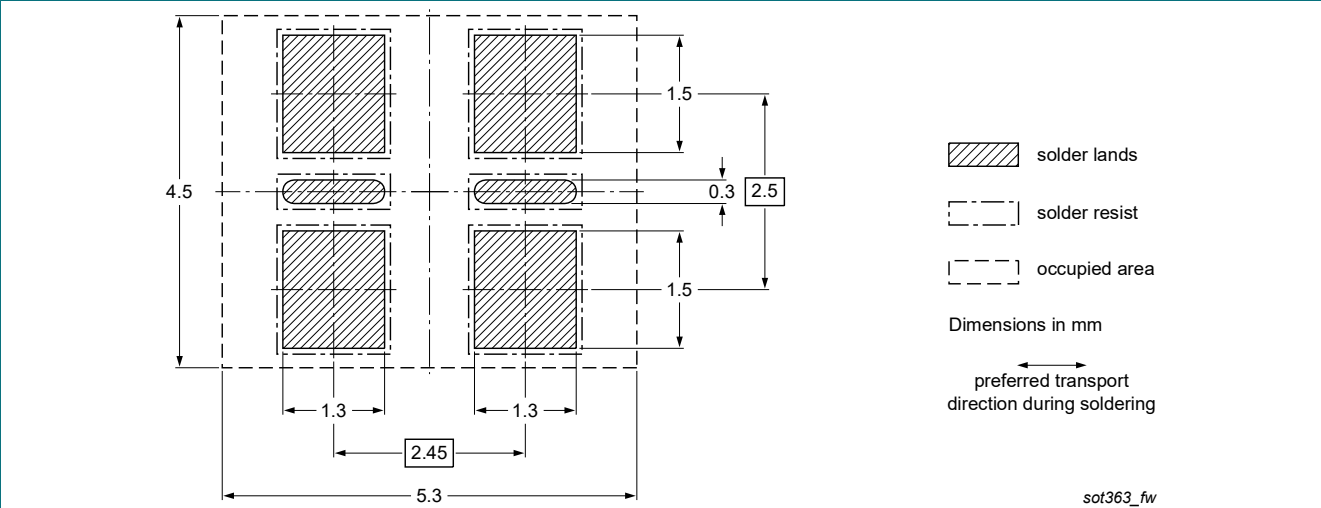


Fig. 13. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMH9-Q v.2	20211007	Product data sheet	-	PUMH9-Q v.1
Modification:	• Complete rework • General description: added new lines at the end • Pinning: Graphic symbol replaced • Limiting values: deleted parameter I_{CM} • Characteristics: I_{CEO} max limit is updated to 100 nA • Characteristics: added new graphics • Characteristics: replaced the figure 006aac785 with aaa-018586 • Characteristics: Updated the graphics conditions • Characteristics: $V_{(BR)EBO}$ values is removed • Test information: Included resistor calculation, resistor test circuit and resistor test condition			
PUMH9-Q v.1	20210625	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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