# HEF4014B

## 8-bit static shift register

Rev. 10 — 17 October 2018 Product data sheet

## 1. General description

The HEF4014B is a fully synchronous edge-triggered 8-bit static shift register with eight synchronous parallel inputs (D0 to D7), a synchronous serial data input (DS), a synchronous parallel enable input (PE), a LOW-to-HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages (Q5 to Q7).

Operation is synchronous and the device is edge-triggered on the LOW-to-HIGH transition of CP. Each register stage is of a D-type master-slave flip-flop type. When PE is HIGH, data is loaded into the register from D0 to D7 on the LOW-to-HIGH transition of CP. When PE is LOW, data is shifted to the first position from DS, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. The clock input's Schmitt trigger action makes it highly tolerant of slower clock rise and fall times.

It operates over a recommended $V_{DD}$ power supply range of 3 V to 15 V referenced to $V_{SS}$ (usually ground). Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input.

## 2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- Parallel-to-serial converter
- Serial data queueing
- General purpose register

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| HEF4014BT | -40 °C to +85 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

## 5. Functional diagram

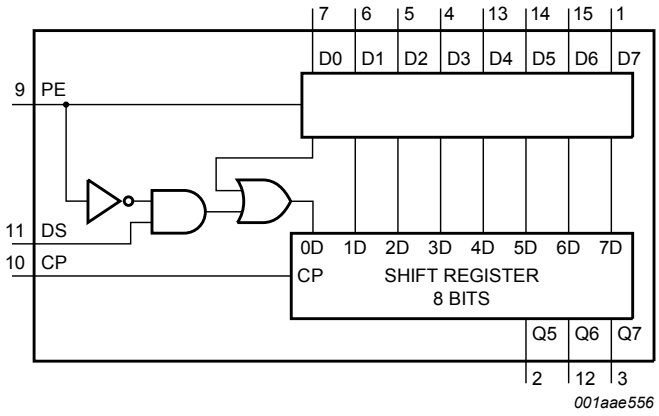



**Fig. 1. Functional diagram**

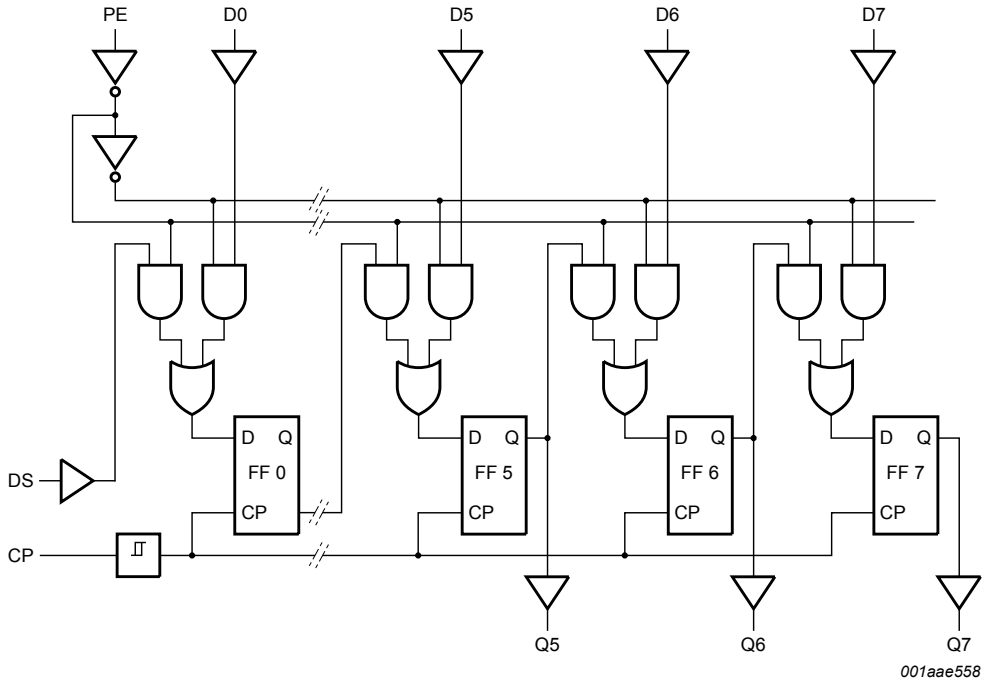



**Fig. 2. Logic diagram**

# 6. Pinning information

## 6.1. Pinning

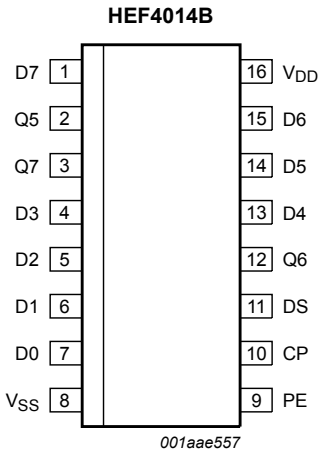



**Fig. 3. Pin configuration SOT109-1 (SO16)**

## 6.2. Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| Q5 to Q7 | 2, 12, 3 | output |
| D0 to D7 | 7, 6, 5, 4, 13, 14, 15, 1 | parallel data input |
| $V_{SS}$ | 8 | ground supply voltage |
| PE | 9 | parallel enable input |
| CP | 10 | clock input (LOW-to-HIGH edge-triggered) |
| DS | 11 | serial data input |
| $V_{DD}$ | 16 | supply voltage |

# 7. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; nD = HIGH or LOW;*
*↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition;*

| Number of clock transitions | Inputs | | | Outputs | | |
|---|---|---|---|---|---|---|
| | CP | DS | PE | Q5 | Q6 | Q7 |
| **Serial operation** | | | | | | |
| 1 | ↑ | 1D | L | X | X | X |
| 2 | ↑ | 2D | L | X | X | X |
| 3 | ↑ | 3D | L | X | X | X |
| 6 | ↑ | X | L | 1D | X | X |
| 7 | ↑ | X | L | 2D | 1D | X |
| 8 | ↑ | X | L | 3D | 2D | 1D |
| | ↓ | X | X | no change | no change | no change |
| **Parallel operation** | | | | | | |
| 1 | ↑ | X | H | D5 | D6 | D7 |
| | ↓ | X | X | no change | no change | no change |

# 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | -0.5 | +18 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V | - | ±10 | mA |
| $V_I$ | input voltage | | -0.5 | $V_{DD} + 0.5$ | V |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V | - | ±10 | mA |
| $I_{I/O}$ | input/output current | | - | ±10 | mA |
| $I_{DD}$ | supply current | | - | 50 | mA |
| $T_{stg}$ | storage temperature | | -65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | -40 | +85 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +85 °C [1] | - | 500 | mW |
| P | power dissipation | per output | - | 100 | mW |

[1] For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | 3 | - | 15 | V |
| $V_I$ | input voltage | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{DD}$ = 5 V | - | - | 3.75 | μs/V |
| | | $V_{DD}$ = 10 V | - | - | 0.5 | μs/V |
| | | $V_{DD}$ = 15 V | - | - | 0.08 | μs/V |

## 10. Static characteristics

**Table 6. Static characteristics**

*$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = -40 °C | | $T_{amb}$ = +25 °C | | $T_{amb}$ = +85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\|I_O\|$ < 1 μA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\|I_O\|$ < 1 μA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $V_{OH}$ | HIGH-level output voltage | $\|I_O\|$ < 1 μA | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| $V_{OL}$ | LOW-level output voltage | $\|I_O\|$ < 1 μA | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 2.5 V | 5 V | - | -1.7 | - | -1.4 | - | -1.1 | mA |
| | | $V_O$ = 4.6 V | 5 V | - | -0.52 | - | -0.44 | - | -0.36 | mA |
| | | $V_O$ = 9.5 V | 10 V | - | -1.3 | - | -1.1 | - | -0.9 | mA |
| | | $V_O$ = 13.5 V | 15 V | - | -3.6 | - | -3.0 | - | -2.4 | mA |
| $I_{OL}$ | LOW-level output current | $V_O$ = 0.4 V | 5 V | 0.52 | - | 0.44 | - | 0.36 | - | mA |
| | | $V_O$ = 0.5 V | 10 V | 1.3 | - | 1.1 | - | 0.9 | - | mA |
| | | $V_O$ = 1.5 V | 15 V | 3.6 | - | 3.0 | - | 2.4 | - | mA |
| $I_I$ | input leakage current | | 15 V | - | ±0.3 | - | ±0.3 | - | ±1.0 | μA |
| $I_{DD}$ | supply current | $I_O$ = 0 A | 5 V | - | 20 | - | 20 | - | 150 | μA |
| | | | 10 V | - | 40 | - | 40 | - | 300 | μA |
| | | | 15 V | - | 80 | - | 80 | - | 600 | μA |
| $C_I$ | input capacitance | | - | - | - | - | 7.5 | - | - | pF |

# 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

*$T_{amb}$ = 25 °C; $V_{SS}$ = 0 V.*

| Symbol | Parameter | Conditions | $V_{DD}$ | Extrapolation formula [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | CP to Qn; see Fig. 4 | 5 V | 103 ns + (0.55 ns/pF)$C_L$ | - | 130 | 260 | ns |
| | | | 10 V | 44 ns + (0.23 ns/pF)$C_L$ | - | 55 | 110 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)$C_L$ | - | 40 | 80 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | CP to Qn; see Fig. 4 | 5 V | 88 ns + (0.55 ns/pF)$C_L$ | - | 115 | 230 | ns |
| | | | 10 V | 39 ns + (0.23 ns/pF)$C_L$ | - | 50 | 100 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)$C_L$ | - | 40 | 80 | ns |
| $t_t$ | transition time | Qn output; see Fig. 4 | 5 V [2] | 10 ns + (1.00 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 10 V | 9 ns + (0.42 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | 6 ns + (0.28 ns/pF)$C_L$ | - | 20 | 40 | ns |
| $t_W$ | pulse width | CP input; minimum width; see Fig. 5 | 5 V | | 70 | 35 | - | ns |
| | | | 10 V | | 30 | 15 | - | ns |
| | | | 15 V | | 24 | 12 | - | ns |
| $t_{su}$ | set-up time | PE to CP; see Fig. 5 | 5 V | | 40 | 10 | - | ns |
| | | | 10 V | | 25 | 5 | - | ns |
| | | | 15 V | | 15 | 0 | - | ns |
| | | DS to CP; see Fig. 5 | 5 V | | +35 | -5 | - | ns |
| | | | 10 V | | +25 | -5 | - | ns |
| | | | 15 V | | 25 | 0 | - | ns |
| | | Dn to CP; see Fig. 5 | 5 V | | +35 | -5 | - | ns |
| | | | 10 V | | +25 | -5 | - | ns |
| | | | 15 V | | 25 | 0 | - | ns |
| $t_h$ | hold time | PE to CP; see Fig. 5 | 5 V | | +25 | -5 | - | ns |
| | | | 10 V | | 20 | 0 | - | ns |
| | | | 15 V | | 15 | 0 | - | ns |
| | | DS to CP; see Fig. 5 | 5 V | | 30 | 15 | - | ns |
| | | | 10 V | | 20 | 10 | - | ns |
| | | | 15 V | | 15 | 7 | - | ns |
| | | Dn to CP; see Fig. 5 | 5 V | | 30 | 15 | - | ns |
| | | | 10 V | | 20 | 10 | - | ns |
| | | | 15 V | | 15 | 7 | - | ns |
| $f_{clk(max)}$ | maximum clock frequency | see Fig. 5 | 5 V | | 6 | 13 | - | MHz |
| | | | 10 V | | 15 | 30 | - | MHz |
| | | | 15 V | | 20 | 40 | - | MHz |

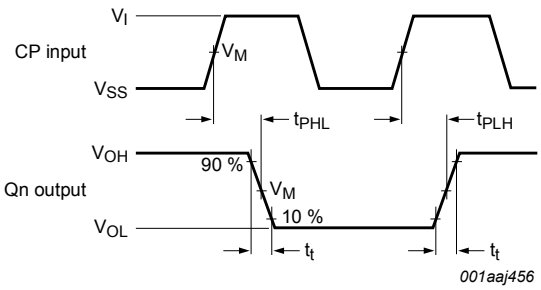
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ($C_L$ in pF).
[2] $t_t$ is the same as $t_{THL}$ and $t_{TLH}$.

**Table 8. Dynamic power dissipation $P_D$**

*$P_D$ can be calculated from the formulas shown. $V_{SS}$ = 0 V; $t_r = t_f \leq 20$ ns; $T_{amb}$ = 25 °C.*

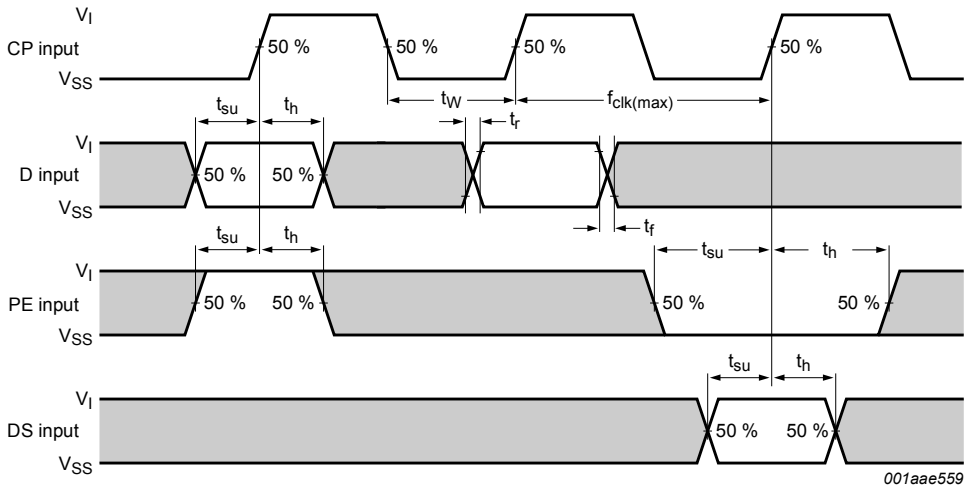
| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ (µW) | Where: |
|---|---|---|---|---|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 900 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz;<br>$f_o$ = output frequency in MHz;<br>$C_L$ = output load capacitance in pF;<br>$V_{DD}$ = supply voltage in V;<br>$\sum(C_L \times f_o)$ = sum of the outputs. |
| | | 10 V | $P_D = 4300 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$ | |
| | | 15 V | $P_D = 12000 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$ | |

## 11.1. Waveforms and test circuit




Measurement points are given in Table 9.

**Fig. 4. CP to Qn propagation delays and output transition times**

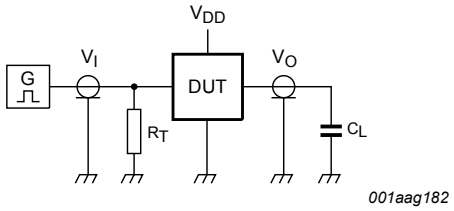



The shaded areas indicate where change is permitted for predictable output performance.
Set-up and hold times are shown as positive values but may be specified as negative values.
Measurement points are given in Table 9.

**Fig. 5. Minimum clock pulse width, and set-up and hold times for PE to CP, DS to CP, and D to CP**

**Table 9. Measurement points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{DD}$ | $V_M$ | $V_M$ |
| 5 V to 15 V | $0.5V_{DD}$ | $0.5V_{DD}$ |




Test data is given in Table 10;
Definitions for test circuit:
DUT = Device Under Test.
$C_L$ = load capacitance including jig and probe capacitance.
$R_T$ = termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

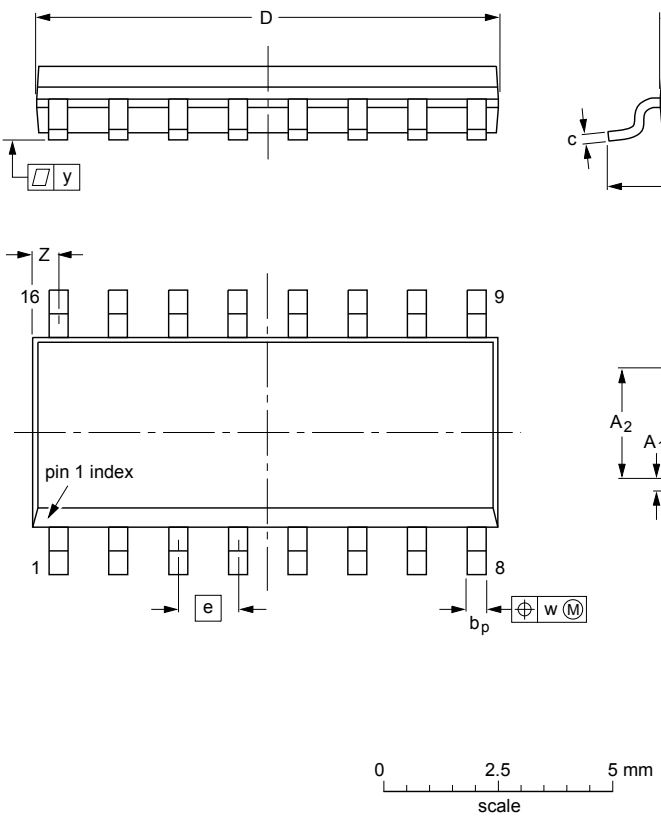
**Fig. 6. Test circuit for measuring switching times**

**Table 10. Test data**

| Supply voltage | Input | | Load |
|---|---|---|---|
| $V_{DD}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ |
| 5 V to 15 V | $V_{SS}$ or $V_{DD}$ | ≤ 20 ns | 50 pF |

## 12. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 7. Package outline SOT109-1 (SO16)**

## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4014B v.10 | 20181017 | Product data sheet | - | HEF4014B v.9 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| HEF4014B v.9 | 20160321 | Product data sheet | - | HEF4014B v.8 |
| Modifications: | • Type number HEF4014BP (SOT38-4) removed. | | | |
| HEF4014B v.8 | 20111121 | Product data sheet | - | HEF4014B v.7 |
| Modifications: | • Legal pages updated.<br>• Changes in "General description" and "Features and benefits". | | | |
| HEF4014B v.7 | 20110914 | Product data sheet | - | HEF4014B v.6 |
| HEF4014B v.6 | 20091102 | Product data sheet | - | HEF4014B v.5 |
| HEF4014B v.5 | 20090624 | Product data sheet | - | HEF4014B v.4 |
| HEF4014B v.4 | 20090122 | Product data sheet | - | HEF4014B_CNV v.3 |
| HEF4014B_CNV v.3 | 19950101 | Product specification | - | HEF4014B_CNV v.2 |
| HEF4014B_CNV v.2 | 19950101 | Product specification | - | - |

# 14. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
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