HEF4016B

Quad single-pole single-throw analog switch

Rev. 4 — 24 October 2016 Product data sheet

1. General description

The HEF4016B provides four single-pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4016BT	–40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

5. Functional diagram

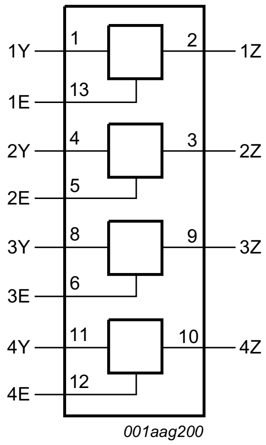


Fig 1. Functional diagram

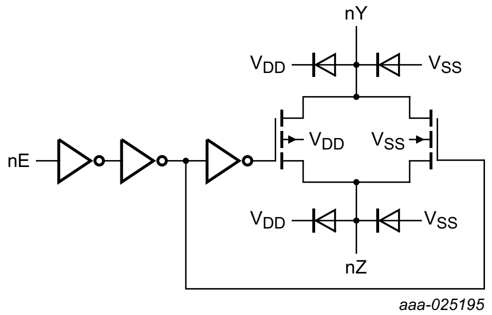


Fig 2. Logic diagram (one switch)

6. Pinning information

6.1 Pinning

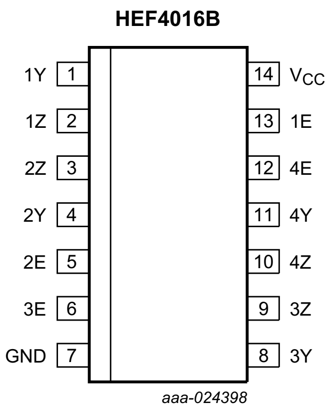


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 8, 11	independent input or output
1Z, 2Z, 3Z, 4Z	2, 3, 9, 10	independent input or output
1E, 2E, 3E, 4E	13, 5, 6, 12	enable input (active HIGH)
V_{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

7. Functional description

Table 3. Function table[1]

Input nE	Switch
H	ON
L	OFF

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+18	V
I_{IK}	input clamping current	V_I < –0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		–0.5	V_{DD} + 0.5	V
$I_{I/O}$	input/output current	[1]	-	±10	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C			
		SO14 [2]	-	500	mW
P	power dissipation	per switch	-	100	mW

[1] To avoid drawing V_{DD} current out of terminal nZ, when switch current flows into terminals nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{DD} current will flow out of terminals nY, in this case there is no limit for the voltage drop across the switch, but the voltages at nY and nZ may not exceed V_{DD} or V_{SS}.

[2] For SO14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics
V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
I_I	input leakage current		15 V	-	-	-	±0.3	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	per channel; see Figure 4	15 V	-	-	-	200	-	-	nA
I_{DD}	supply current	all valid input combinations	5 V	-	1.0	-	1.0	-	7.5	μA
			10 V	-	2.0	-	2.0	-	15.0	μA
			15 V	-	4.0	-	4.0	-	30.0	μA
C_I	input capacitance	nE input	-	-	-	-	7.5	-	-	pF

10.1 Test circuit

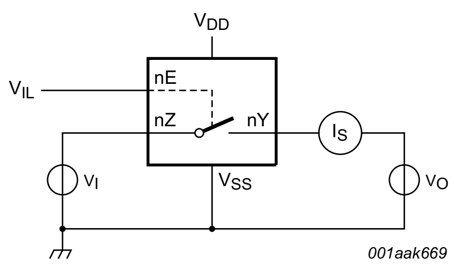


Fig 4. Test circuit for measuring OFF-state leakage current

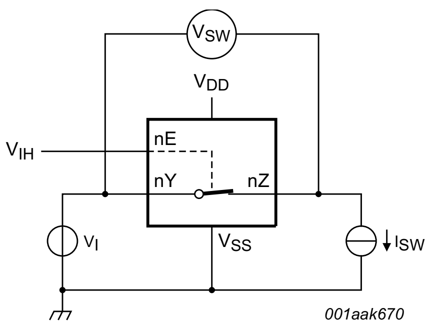
10.2 ON resistance

Table 7. ON resistance

T_{amb} = 25 °C; I_{SW} = 100 μA; V_{SS} = 0 V.

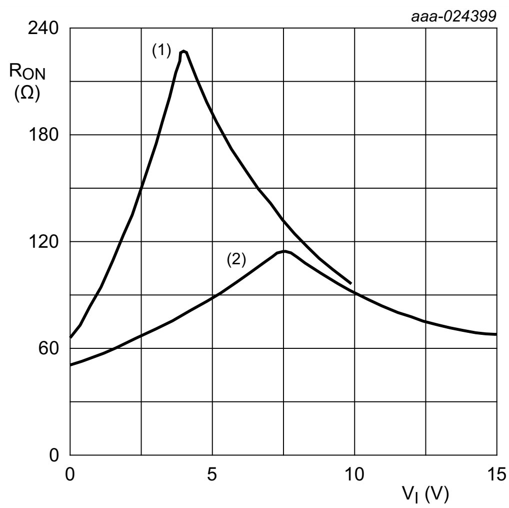
Symbol	Parameter	Conditions	V_{DD}	Typ	Max	Unit
$R_{ON(peak)}$	ON resistance (peak)	V_I = 0 V to V_{DD}; see Figure 5 and Figure 6	5 V	8000	-	Ω
			10 V	230	690	Ω
			15 V	115	350	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = 0 V; see Figure 5 and Figure 6	5 V	140	425	Ω
			10 V	65	195	Ω
			15 V	50	145	Ω
		V_I = V_{DD}; see Figure 5 and Figure 6	5 V	170	515	Ω
			10 V	95	285	Ω
			15 V	75	220	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0 V to V_{DD}; see Figure 5	5 V	200	-	Ω
			10 V	15	-	Ω
			15 V	10	-	Ω

10.2.1 ON resistance waveform and test circuit



$R_{ON} = V_{SW} / I_{SW}$.

Fig 5. Test circuit for measuring R_{ON}



I_{SW} = 100 μA.

(1) V_{DD} = 10 V

(2) V_{DD} = 15 V

Fig 6. Typical R_{ON} as a function of input voltage

11. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = 25 °C; V_{SS} = 0 V; for test circuit see Figure 9.

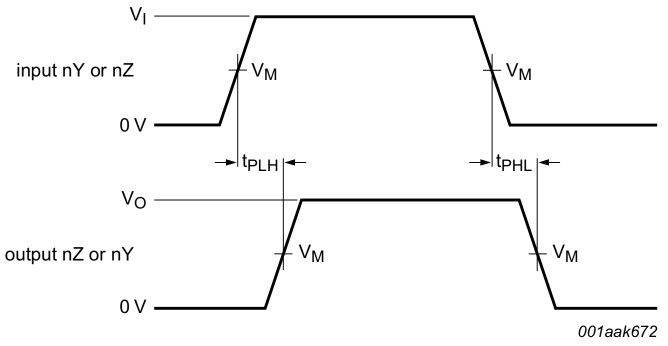
Symbol	Parameter	Conditions	V_{DD}	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nY, nZ to nZ, nY; see Figure 7	5 V	25	50	ns
			10 V	10	20	ns
			15 V	5	10	ns
t_{PLH}	LOW to HIGH propagation delay	nY, nZ to nZ, nY; see Figure 7	5 V	20	40	ns
			10 V	10	20	ns
			15 V	5	10	ns
t_{PHZ}	HIGH to OFF-state propagation delay	nE to nY, nZ; see Figure 8	5 V	90	130	ns
			10 V	80	110	ns
			15 V	75	100	ns
t_{PLZ}	LOW to OFF-state propagation delay	nE to nY, nZ; see Figure 8	5 V	85	120	ns
			10 V	75	100	ns
			15 V	75	100	ns
t_{PZH}	OFF-state to HIGH propagation delay	nE to nY, nZ; see Figure 8	5 V	40	80	ns
			10 V	20	40	ns
			15 V	15	30	ns
t_{PZL}	OFF-state to LOW propagation delay	nE to nY, nZ; see Figure 8	5 V	40	80	ns
			10 V	20	40	ns
			15 V	15	30	ns

Table 9. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown; V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

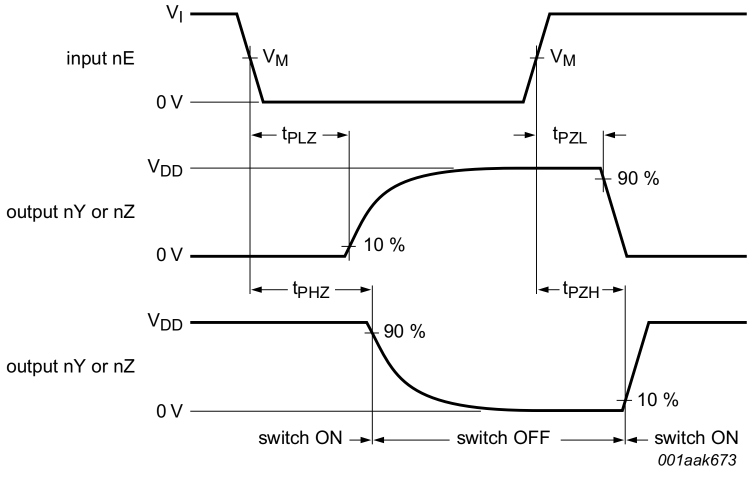
Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 550 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 2600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 6500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF;
				V_{DD} = supply voltage in V;
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

11.1 Waveforms and test circuit



Measurement points are given in Table 10.

Fig 7. nY or nZ to nZ or nY propagation delays

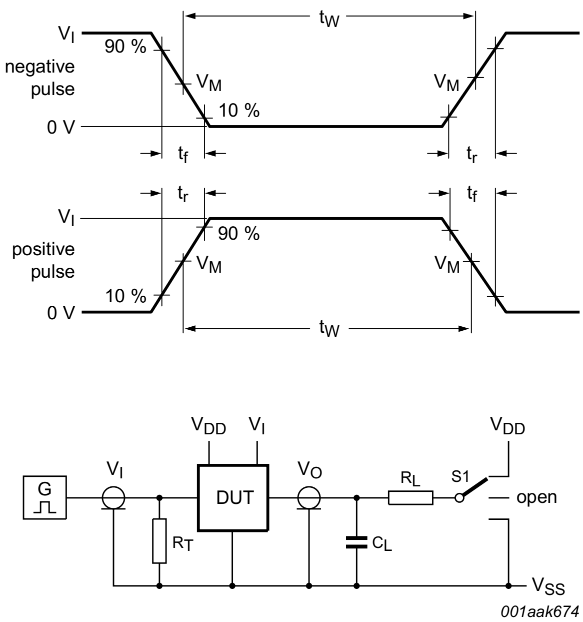


Measurement points are given in Table 10.

Fig 8. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in Table 11.

Definitions:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including test jig and probe.

R_L = Load resistance.

Fig 9. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		S1 position		
V_{DD}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
5 V to 15 V	0 V or V_{DD}	≤ 20 ns	50 pF	10 kΩ	V_{SS}	V_{SS}	V_{DD}

11.2 Additional dynamic parameters

Table 12. Additional dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	V_{DD}		Typ	Max	Unit
THD	total harmonic distortion	see Figure 10; R_L = 10 kΩ; C_L = 15 pF; channel ON; V_I = 0.5V_{DD} (p-p); f_i = 1 kHz	5 V	[1]	-	-	%
			10 V	[1]	0.08	-	%
			15 V	[1]	0.04	-	%
V_{ct}	crosstalk voltage	nE input to switch; see Figure 11; R_L = 10 kΩ; C_L = 15 pF; nE = V_{DD} (square-wave)	10 V		50	-	mV

Table 12. Additional dynamic characteristics *...continued*
V_{SS} = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	V_{DD}		Typ	Max	Unit
Xtalk	crosstalk	between switches; see Figure 12; f_i = 1 MHz; R_L = 1 kΩ; V_I = 0.5V_{DD} (p-p)	10 V	[1]	–50	-	dB
α_{iso}	isolation (OFF-state)	see Figure 13; f_i = 1 MHz; R_L = 1 kΩ; C_L = 5 pF; V_I = 0.5V_{DD} (p-p)	10 V	[1]	–50	-	dB
$f_{(-3dB)}$	–3 dB frequency response	see Figure 14; R_L = 1 kΩ; C_L = 5 pF; V_I = 0.5V_{DD} (p-p)	10 V	[1]	90	-	MHz

[1] f_i is biased at 0.5V_{DD}.

11.2.1 Test circuits

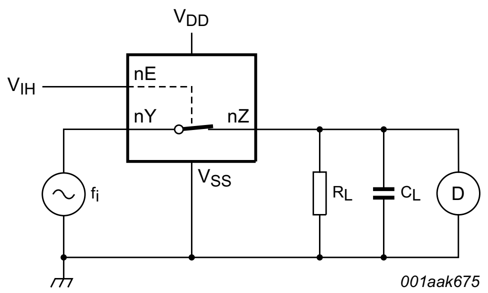
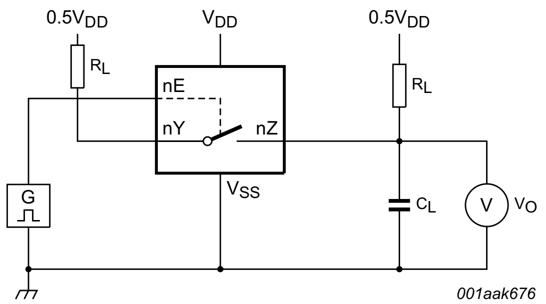
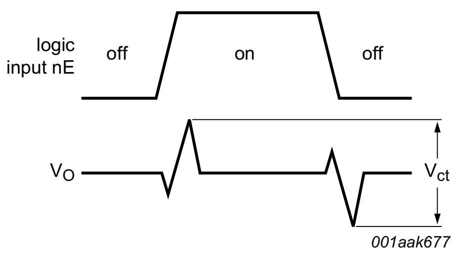


Fig 10. Test circuit for measuring total harmonic distortion

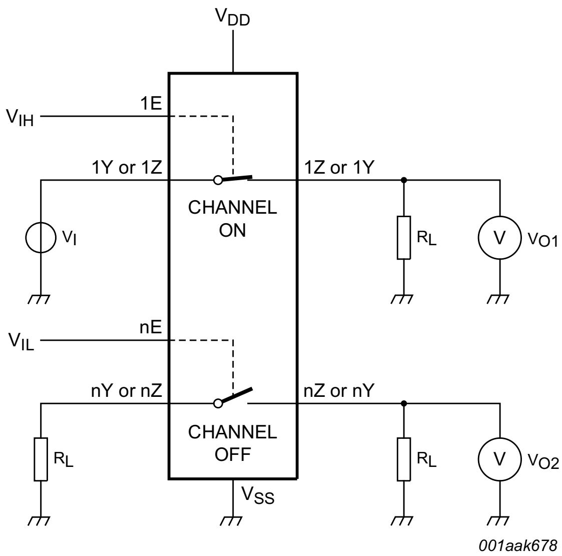


a. Test circuit



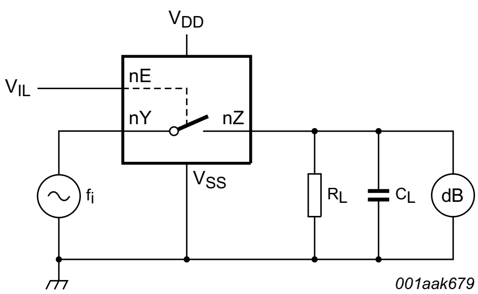
b. Input and output pulse definitions

Fig 11. Test circuit for measuring crosstalk voltage between digital input and switch



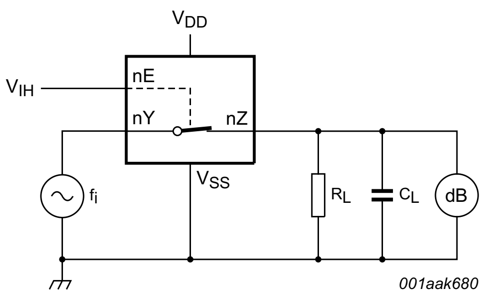
20 $\log_{10}$ (V_{O2} / V_{O1}) or 20 $\log_{10}$ (V_{O1} / V_{O2}).

Fig 12. Test circuit for measuring crosstalk between switches



Adjust f_i voltage to obtain 0 dBm level at input.

Fig 13. Test circuit for measuring isolation (OFF-state)

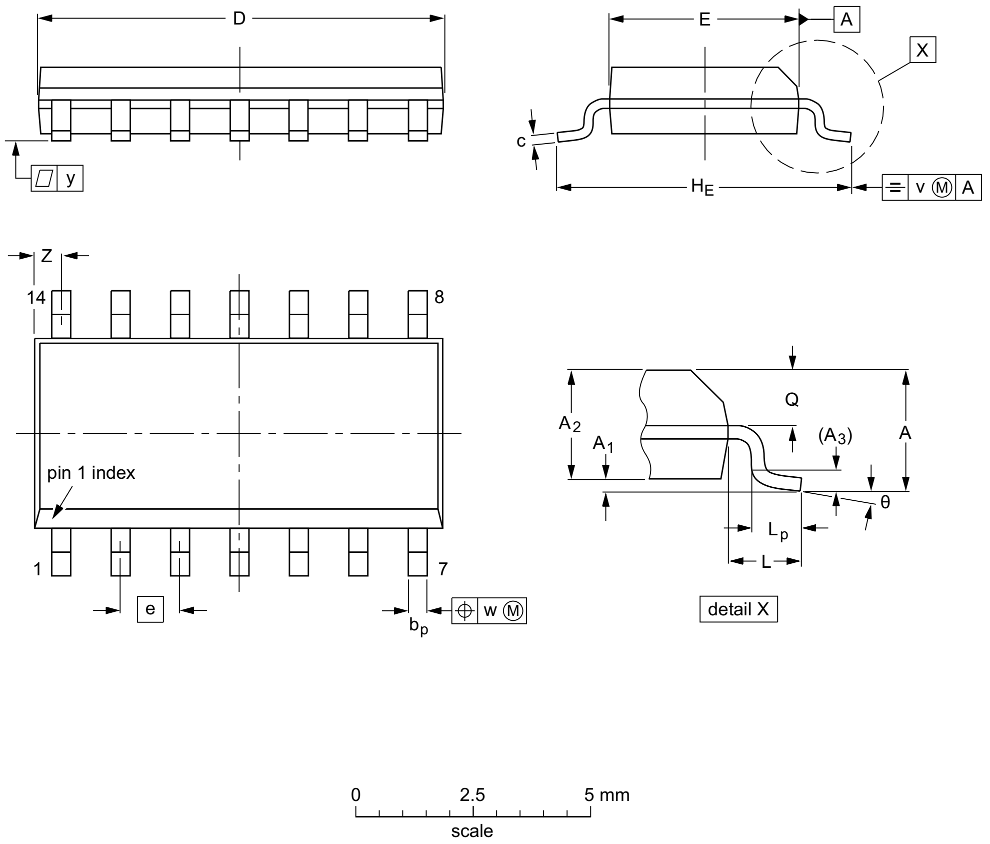


Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads −3 dB.

Fig 14. Test circuit for measuring frequency response

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
DUT	Device Under Test

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4016B v.4	20161024	Product data sheet	-	HEF4016B_CNV v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
HEF4016B_CNV v.3	19950101	Product specification	-	HEF4016B_CNV v.2
HEF4016B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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17. Contents

Date of release: 24 October 2016

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