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Kind regards,

Team Nexperia



PBL2001D

20 V PNP BISS loadswitch

Rev. 02 — 27 August 2009

Product data sheet

1. Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough in Small Signal (BISS) transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface Mounted Device (SMD) plastic package.

1.2 Features

- Low V_{CEsat} (BISS) and resistor-equipped transistor in one package
- Low threshold voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

1.4 Quick reference data

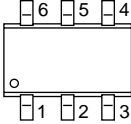
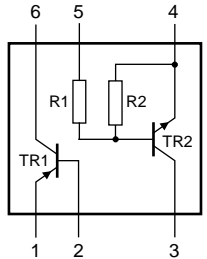
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|----------------------------------|------|-----|------|------------|
| TR1; PNP low V_{CEsat} transistor | | | | | | |
| V_{CEO} | collector-emitter voltage | open base | - | - | -20 | V |
| I_C | collector current (DC) | | - | - | -1 | A |
| R_{CEsat} | collector-emitter saturation resistance | $I_C = -1$ A; $I_B = -100$ mA | [1] | 185 | 280 | m Ω |
| TR2; NPN resistor-equipped transistor | | | | | | |
| V_{CEO} | collector-emitter voltage | open base | - | - | 50 | V |
| I_O | output current | | - | - | 100 | mA |
| R1 | bias resistor 1 (input) | | 1.54 | 2.2 | 2.86 | k Ω |
| R2/R1 | bias resistor ratio | | 0.8 | 1 | 1.2 | |

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$

2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline | Symbol |
|-----|------------------------|--|---|
| 1 | emitter TR1 |  |  |
| 2 | base TR1 | | |
| 3 | output (collector) TR2 | | |
| 4 | GND (emitter) TR2 | | |
| 5 | input (base) TR2 | | |
| 6 | collector TR1 | | |

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3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| PBLS2001D | SC-74 | plastic surface mounted package; 6 leads | SOT457 |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PBLS2001D | F6 |

5. Limiting values

Table 5. Limiting values

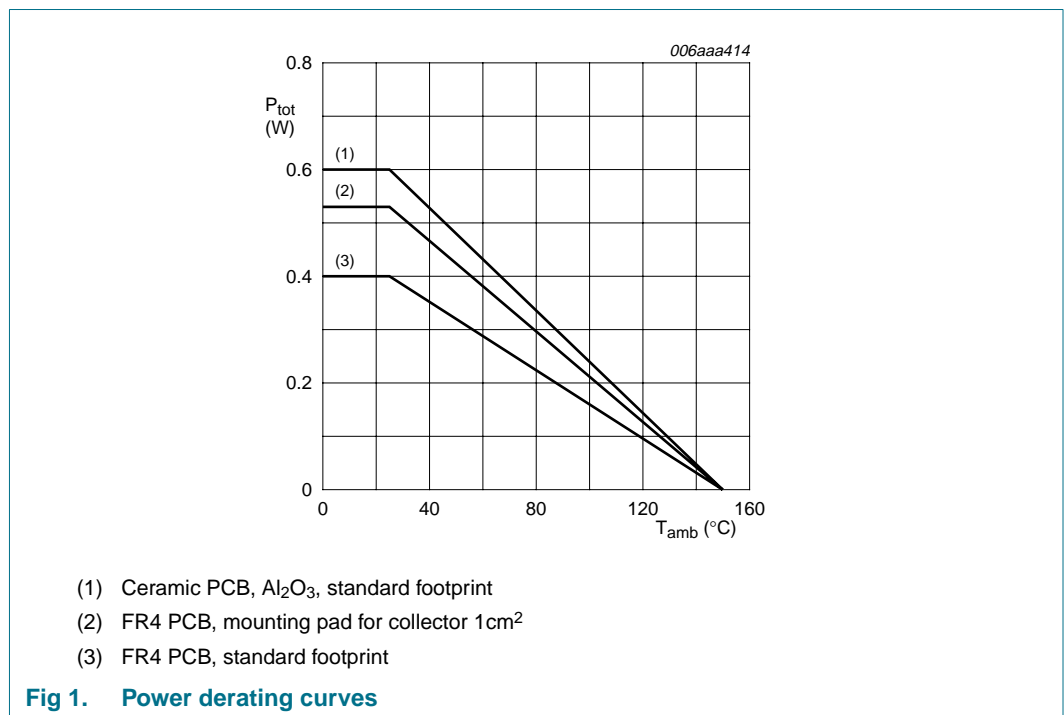
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|---|---------------------------|--|-----|------|------|----|
| TR1; PNP low V_{CEsat} transistor | | | | | | |
| V_{CBO} | collector-base voltage | open emitter | - | -20 | V | |
| V_{CEO} | collector-emitter voltage | open base | - | -20 | V | |
| V_{EBO} | emitter-base voltage | open collector | - | -5 | V | |
| I_C | collector current (DC) | | - | -1 | A | |
| I_{CM} | peak collector current | $t_p \leq 300 \mu s$ | - | -2 | A | |
| I_B | base current (DC) | | - | -0.3 | A | |
| I_{BM} | peak base current | $t_p \leq 300 \mu s$ | - | -0.6 | A | |
| P_{tot} | total power dissipation | $T_{amb} \leq 25 \text{ }^\circ\text{C}$ | [1] | - | 250 | mW |
| | | | [2] | - | 350 | mW |
| | | | [3] | - | 400 | mW |

Table 5. Limiting values ...continued
 In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|---------------------------|------------------------------------|-----|------|------------|
| TR2; NPN resistor-equipped transistor | | | | | |
| V_{CBO} | collector-base voltage | open emitter | - | 50 | V |
| V_{CEO} | collector-emitter voltage | open base | - | 50 | V |
| V_{EBO} | emitter-base voltage | open collector | - | 10 | V |
| V_I | input voltage | | | | |
| | positive | | - | +12 | V |
| | negative | | - | -10 | V |
| I_O | output current | | - | 100 | mA |
| I_{CM} | peak collector current | $t_p \leq 300 \mu s$ | - | 100 | mA |
| P_{tot} | total power dissipation | $T_{amb} \leq 25 \text{ }^\circ C$ | [1] | - | 200 mW |
| Per device | | | | | |
| P_{tot} | total power dissipation | | [1] | - | 400 mW |
| | | | [2] | - | 530 mW |
| | | | [3] | - | 600 mW |
| T_{stg} | storage temperature | | -65 | +150 | $^\circ C$ |
| T_j | junction temperature | | - | 150 | $^\circ C$ |
| T_{amb} | ambient temperature | | -65 | +150 | $^\circ C$ |

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



6. Thermal characteristics

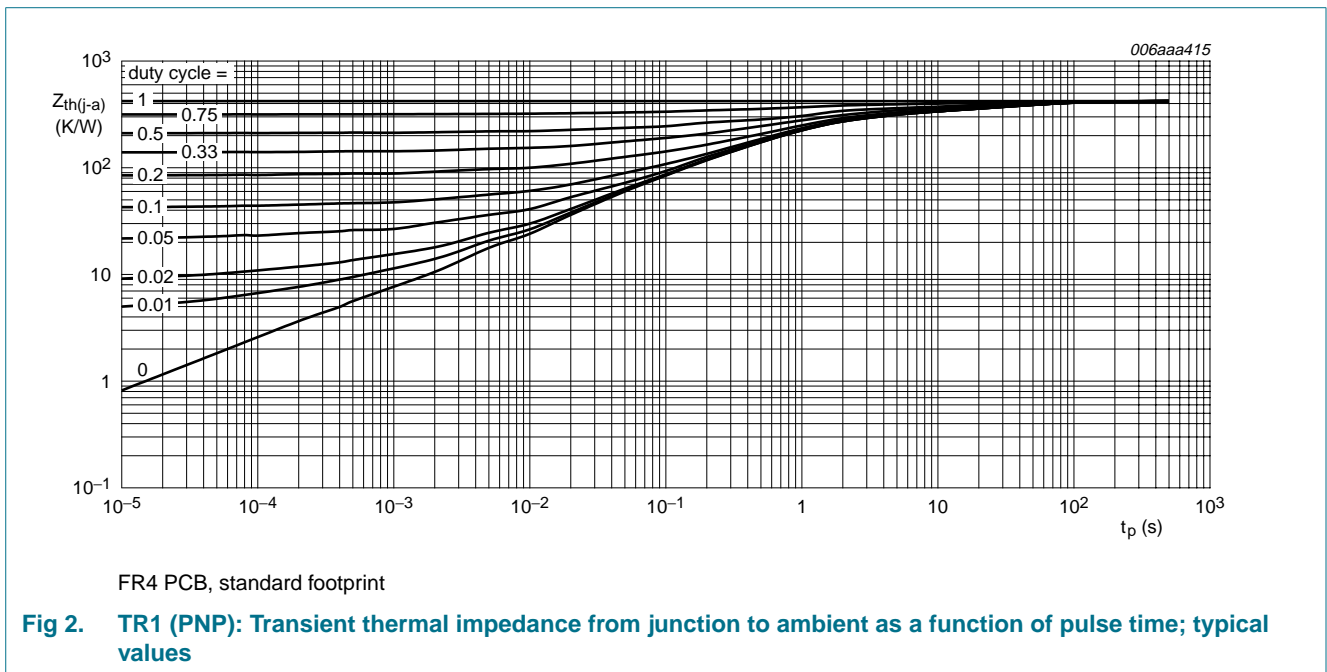
Table 6. Thermal characteristics

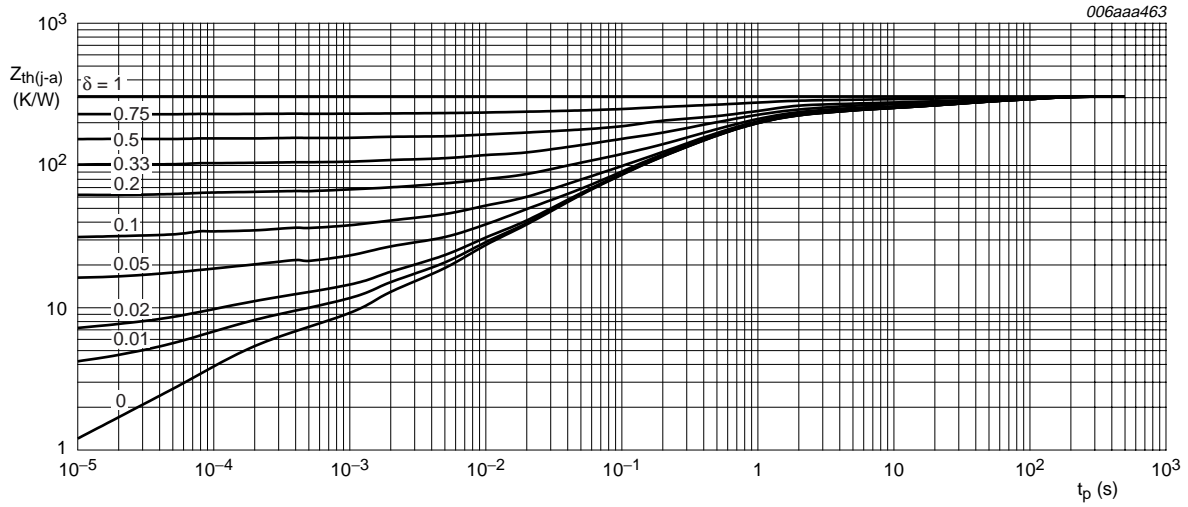
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-------------------|---|-------------|-----|-----|-----|------|-----|
| Per device | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 315 | K/W |
| | | | [2] | - | - | 236 | K/W |
| | | | [3] | - | - | 210 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

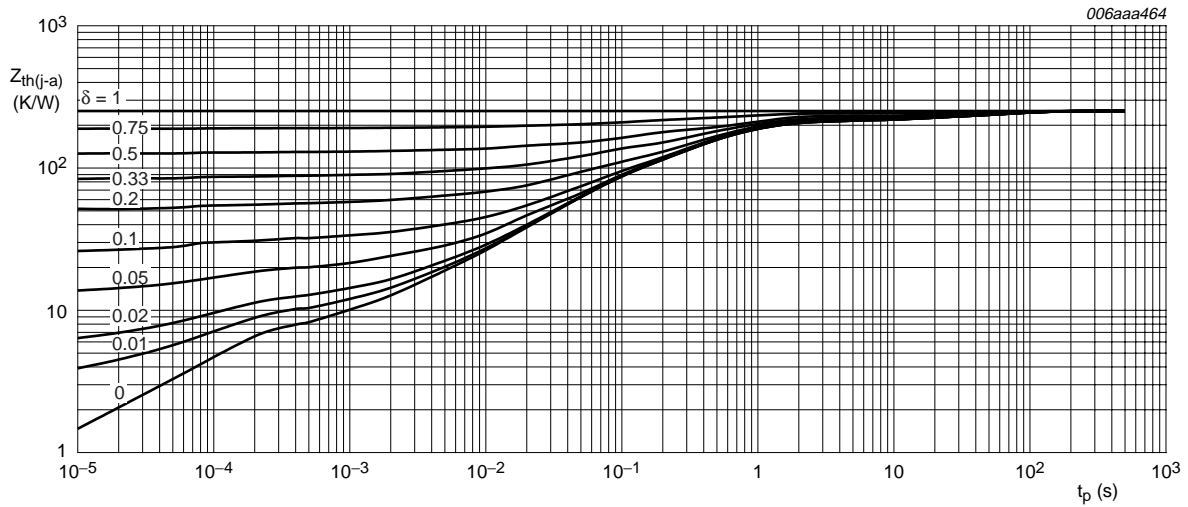
[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.





FR4 PCB, mounting pad for collector 1cm²

Fig 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values



Ceramic PCB, Al₂O₃, standard footprint

Fig 4. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values

7. Characteristics

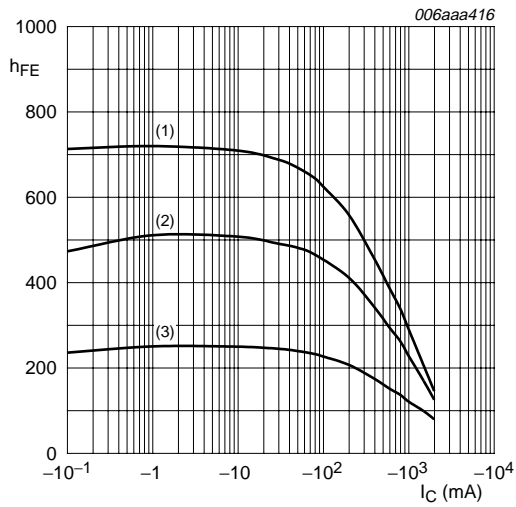
Table 7. Characteristics
T_{amb} = 25 °C unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--|---|--|-----|-----|-------|------|----|
| TR1; PNP low V_{CEsat} transistor | | | | | | | |
| I _{CBO} | collector-base cut-off current | V _{CB} = -20 V; I _E = 0 A | - | - | -0.1 | μA | |
| | | V _{CB} = -20 V; I _E = 0 A; T _j = 150 °C | - | - | -50 | μA | |
| I _{CES} | collector-emitter cut-off current | V _{CE} = -20 V; V _{BE} = 0 V | - | - | -0.1 | μA | |
| I _{EBO} | emitter-base cut-off current | V _{EB} = -5 V; I _C = 0 A | - | - | -0.1 | μA | |
| h _{FE} | DC current gain | V _{CE} = -2 V; I _C = -1 mA | 220 | 495 | - | | |
| | | V _{CE} = -2 V; I _C = -100 mA | 220 | 440 | - | | |
| | | V _{CE} = -2 V; I _C = -500 mA | [1] | 220 | 310 | - | |
| | | V _{CE} = -2 V; I _C = -1 A | [1] | 155 | 220 | - | |
| | | V _{CE} = -2 V; I _C = -2 A | [1] | 60 | 120 | - | |
| V _{CEsat} | collector-emitter saturation voltage | I _C = -100 mA; I _B = -1 mA | - | -55 | -90 | mV | |
| | | I _C = -500 mA; I _B = -50 mA | [1] | - | -100 | -150 | mV |
| | | I _C = -1 A; I _B = -50 mA | [1] | - | -200 | -300 | mV |
| | | I _C = -1 A; I _B = -100 mA | [1] | - | -185 | -280 | mV |
| R _{CEsat} | collector-emitter saturation resistance | I _C = -1 A; I _B = -100 mA | [1] | - | 185 | 280 | mΩ |
| V _{BEsat} | base-emitter saturation voltage | I _C = -1 A; I _B = -50 mA | [1] | - | -0.95 | -1.1 | V |
| | | I _C = -1 A; I _B = -100 mA | [1] | - | -1 | -1.1 | V |
| V _{BEon} | base-emitter turn-on voltage | V _{CE} = -5 V; I _C = -1 A | [1] | - | -0.85 | -1.1 | V |
| t _d | delay time | I _C = -1 A; I _{Bon} = -50 mA; | - | 8 | - | ns | |
| t _r | rise time | I _{Boff} = 50 mA | - | 34 | - | ns | |
| t _{on} | turn-on time | | - | 42 | - | ns | |
| t _s | storage time | | - | 140 | - | ns | |
| t _f | fall time | | - | 45 | - | ns | |
| t _{off} | turn-off time | | - | 185 | - | ns | |
| f _T | transition frequency | I _C = -50 mA; V _{CE} = -10 V; f = 100 MHz | 150 | 185 | - | MHz | |
| C _c | collector capacitance | V _{CB} = -10 V; I _E = I _e = 0 A; f = 1 MHz | - | 15 | 20 | pF | |

Table 7. Characteristics ...continued*T_{amb} = 25 °C unless otherwise specified*

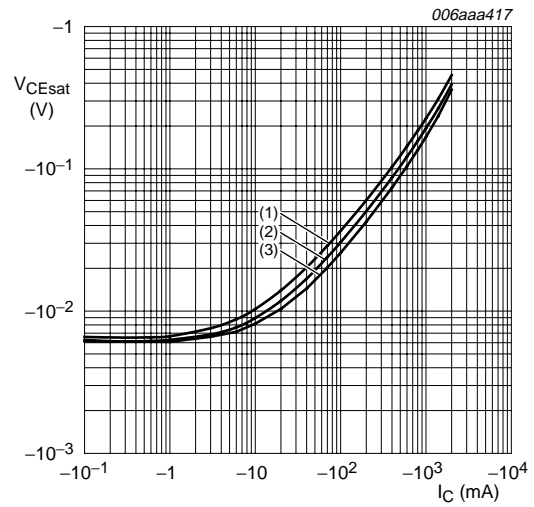
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--------------------------------------|---|------|-----|------|------|
| TR2; NPN resistor-equipped transistor | | | | | | |
| I _{CBO} | collector-base cut-off current | V _{CB} = 50 V; I _E = 0 A | - | - | 100 | nA |
| I _{CEO} | collector-emitter cut-off current | V _{CE} = 30 V; I _B = 0 A | - | - | 1 | μA |
| | | V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C | - | - | 50 | μA |
| I _{EBO} | emitter-base cut-off current | V _{EB} = 5 V; I _C = 0 A | - | - | 2 | mA |
| h _{FE} | DC current gain | V _{CE} = 5 V; I _C = 20 mA | 30 | - | - | |
| V _{CEsat} | collector-emitter saturation voltage | I _C = 10 mA; I _B = 0.5 mA | - | - | 150 | mV |
| V _{I(off)} | off-state input voltage | V _{CE} = 5 V; I _C = 1 mA | - | 1.2 | 0.5 | V |
| V _{I(on)} | on-state input voltage | V _{CE} = 0.3 V; I _C = 20 mA | 2 | 1.6 | - | V |
| R1 | bias resistor 1 (input) | | 1.54 | 2.2 | 2.86 | kΩ |
| R2/R1 | bias resistor ratio | | 0.8 | 1 | 1.2 | |
| C _c | collector capacitance | V _{CB} = 10 V; I _E = i _e = 0 A; f = 1 MHz | - | - | 2.5 | pF |

[1] Pulse test: t_p ≤ 300 μs; δ ≤ 0.02



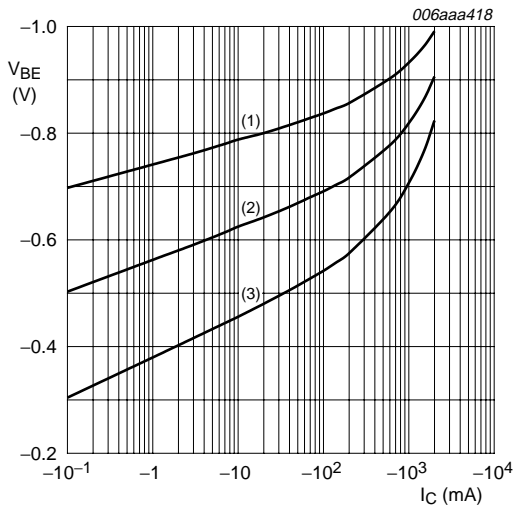
$V_{CE} = -2 \text{ V}$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -55 \text{ }^\circ\text{C}$

Fig 5. TR1 (PNP): DC current gain as a function of collector current; typical values



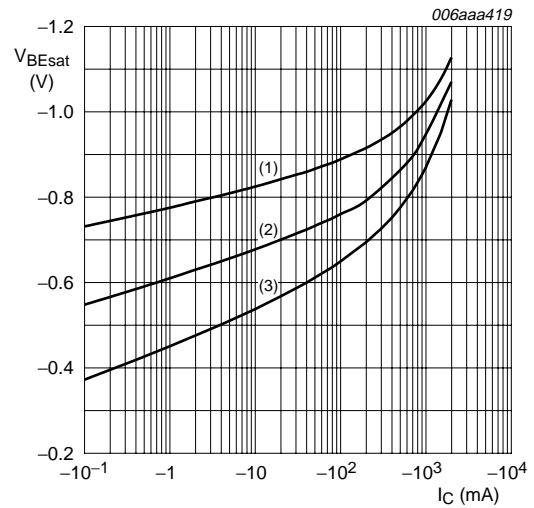
$I_C/I_B = 20$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -55 \text{ }^\circ\text{C}$

Fig 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -55 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = -55 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

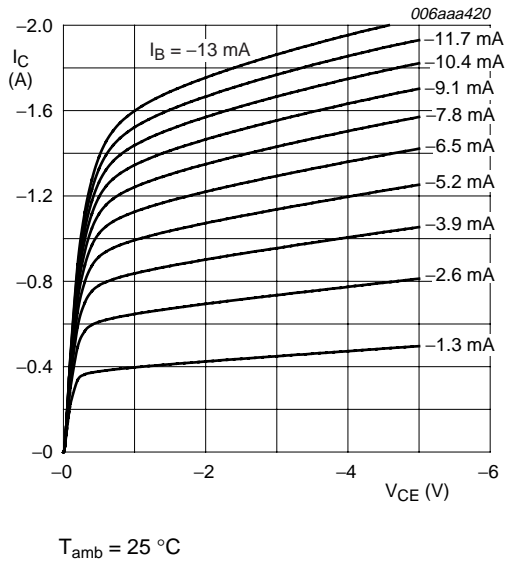


Fig 9. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values

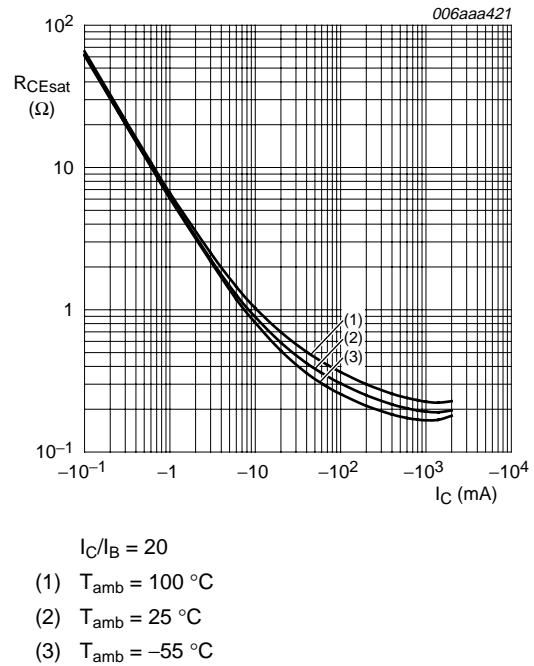


Fig 10. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

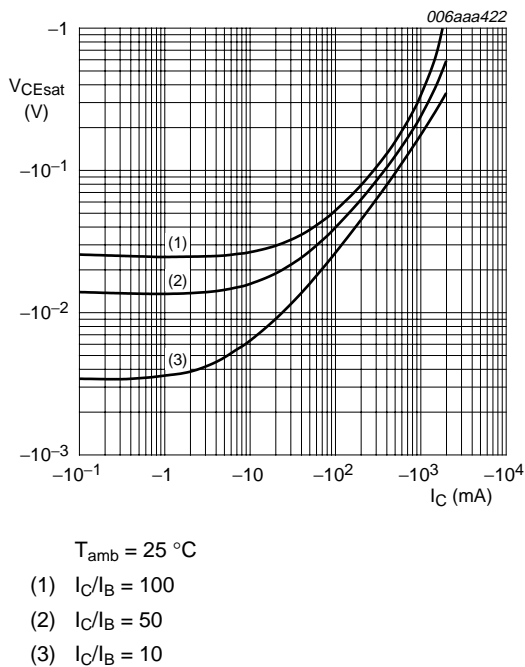


Fig 11. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

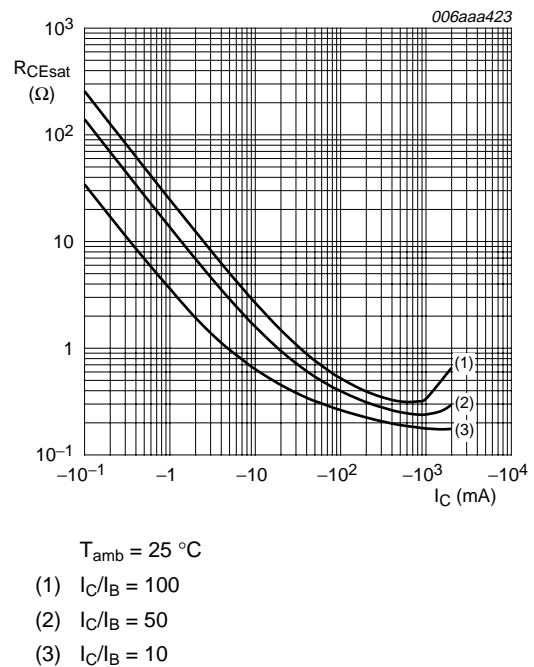
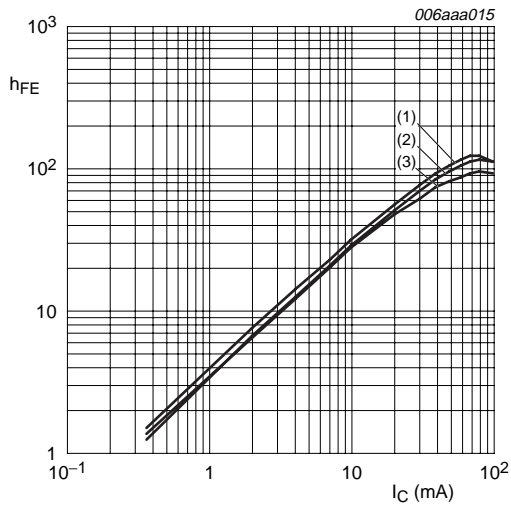
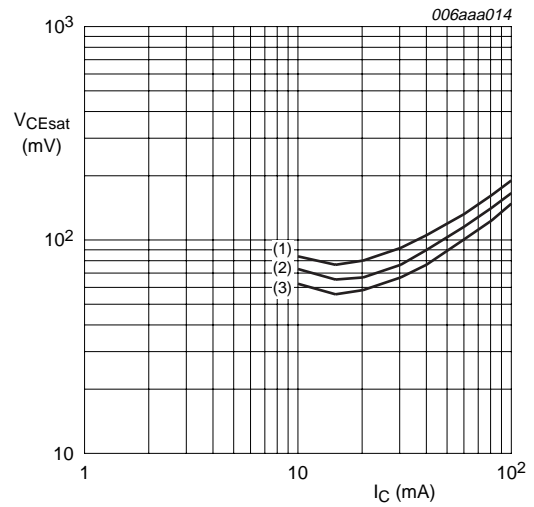


Fig 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



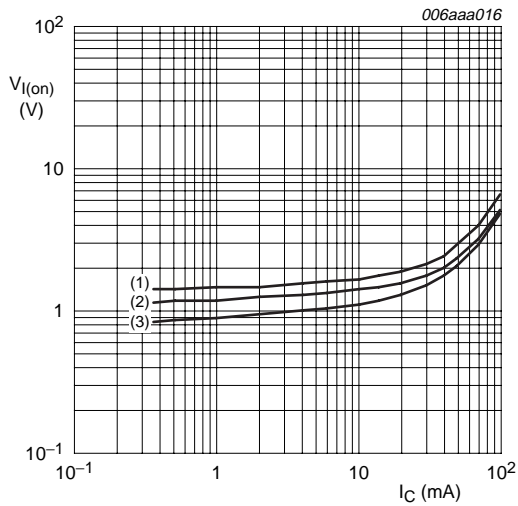
- $V_{CE} = 5 \text{ V}$
- (1) $T_{amb} = 150 \text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 - (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 13. TR2 (NPN): DC current gain as a function of collector current; typical values



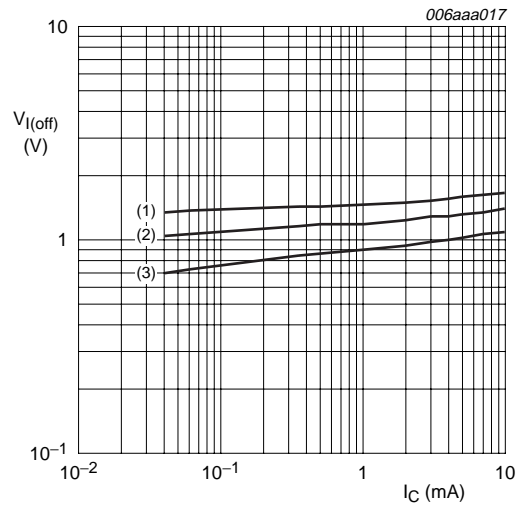
- $I_C/I_B = 20$
- (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 - (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 14. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



- $V_{CE} = 0.3 \text{ V}$
- (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 - (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 15. TR2 (NPN): On-state input voltage as a function of collector current; typical values



- $V_{CE} = 5 \text{ V}$
- (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 - (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 16. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

8. Test information

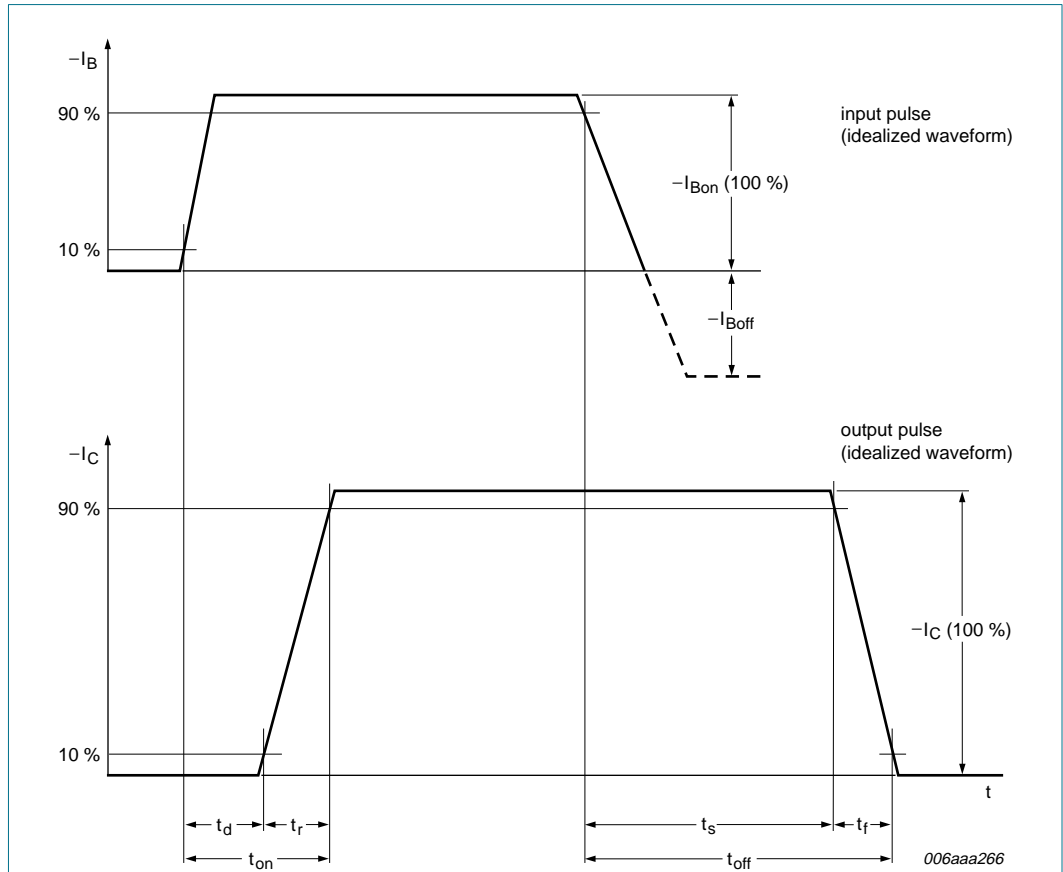


Fig 17. BISS transistor switching time definition

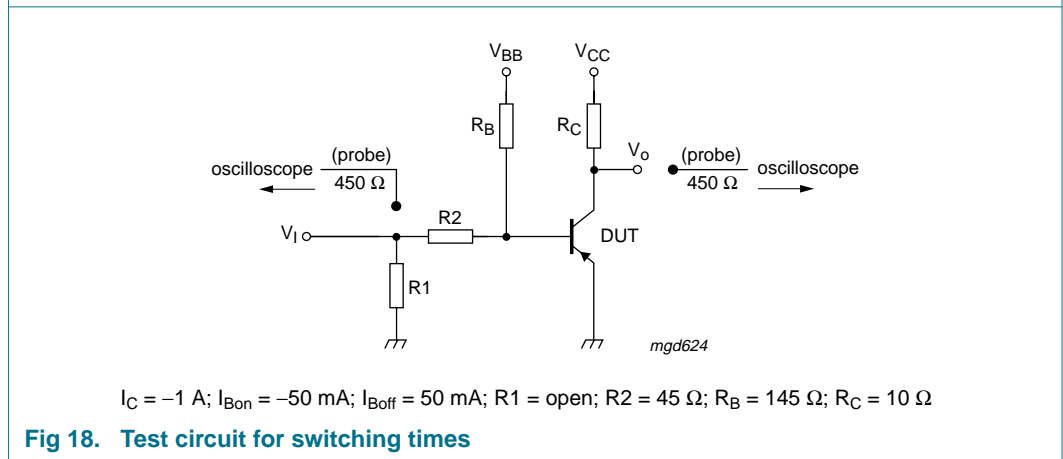
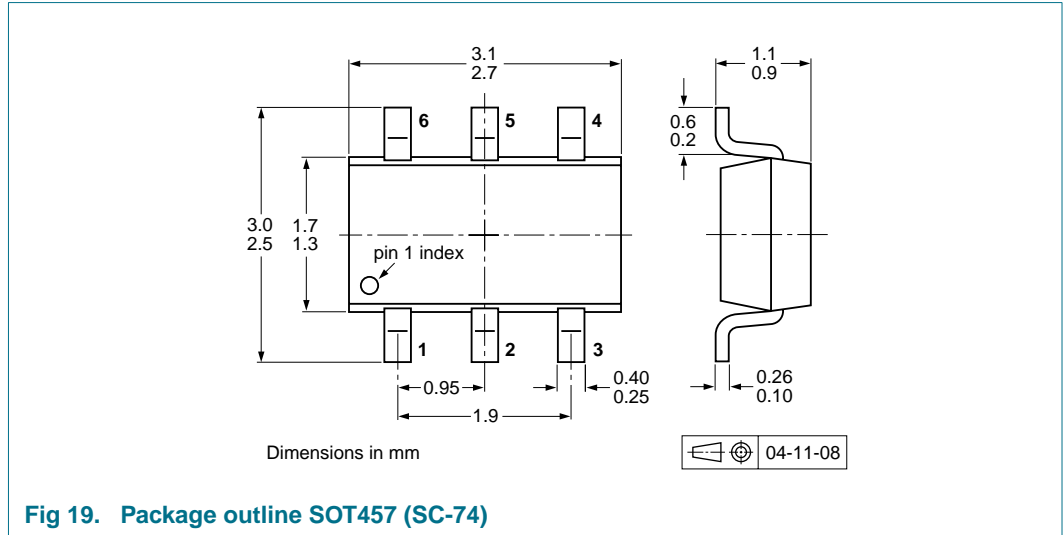


Fig 18. Test circuit for switching times

9. Package outline



10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

| Type number | Package | Description | Packing quantity | |
|-------------|---------|------------------------------------|---------------------|-------|
| | | | 3000 | 10000 |
| PBLS2001D | SOT457 | 4 mm pitch, 8 mm tape and reel; T1 | ^[2] -115 | -135 |
| | | 4 mm pitch, 8 mm tape and reel; T2 | ^[3] -125 | -165 |

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering

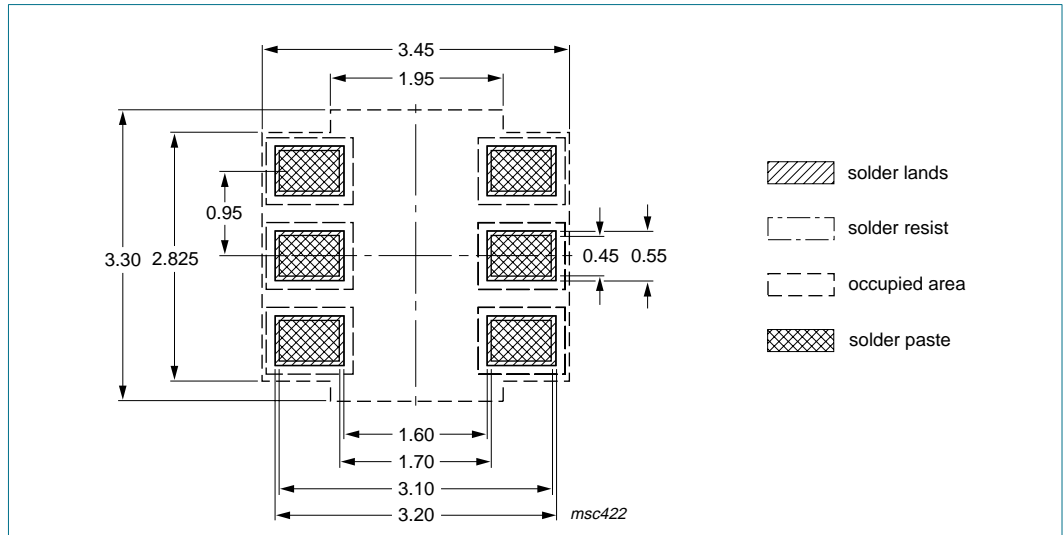


Fig 20. Reflow soldering footprint

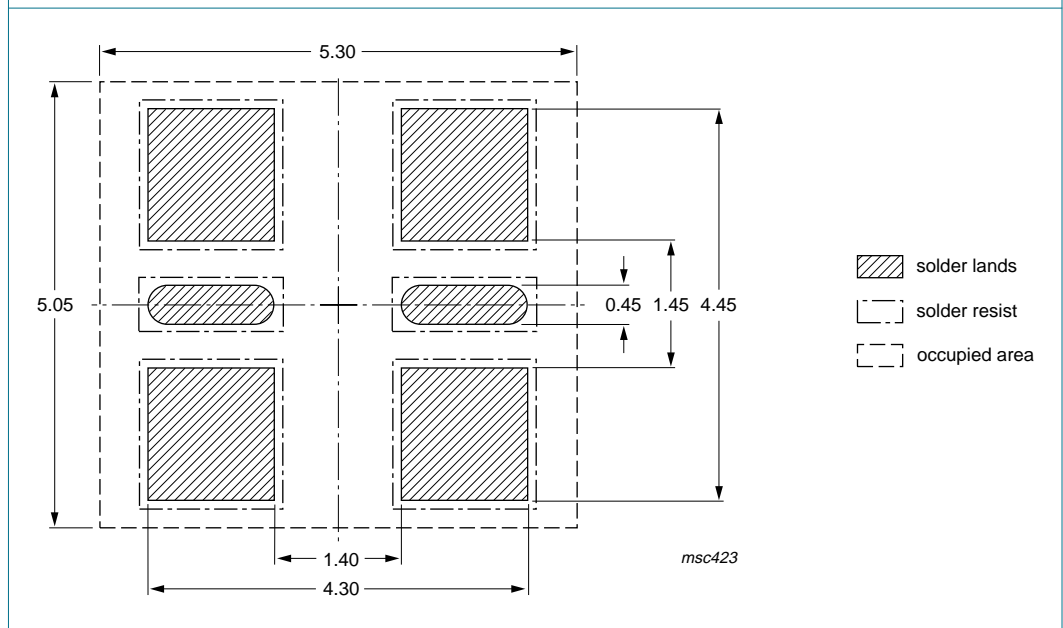


Fig 21. Wave soldering footprint

12. Revision history

Table 9. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|------------|
| PBL2001D_2 | 20090827 | Product data sheet | - | PBL2001D_1 |
| Modifications: | <ul style="list-style-type: none">• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.• Figure 21 "Wave soldering footprint": updated | | | |
| PBL2001D_1 | 20050705 | Product data sheet | - | - |

13. Legal information

13.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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