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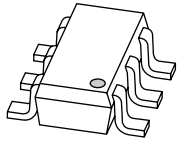
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Kind regards,

Team Nexperia



# PBSS4032PD

30 V, 2.7 A PNP low  $V_{CEsat}$  (BISS) transistor

Rev. 01 — 27 January 2010

Product data sheet

## 1. Product profile

### 1.1 General description

PNP low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) transistor in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

NPN complement: PBSS4032ND.

### 1.2 Features

- Low collector-emitter saturation voltage  $V_{CEsat}$
- Optimized switching time
- High collector current capability  $I_C$  and  $I_{CM}$
- High collector current gain ( $h_{FE}$ ) at high  $I_C$
- High energy efficiency due to less heat generation
- AEC-Q101 qualified
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

### 1.3 Applications

- DC-to-DC conversion
- Battery-driven devices
- Power management
- Charging circuits

### 1.4 Quick reference data

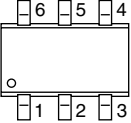
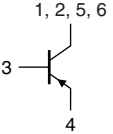
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CEO}$	collector-emitter voltage	open base	-	-	-30	V
$I_C$	collector current		-	-	-2.7	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-5	A
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = -3$ A; $I_B = -300$ mA	[1] -	88	130	m $\Omega$

[1] Pulse test:  $t_p \leq 300$   $\mu$ s;  $\delta \leq 0.02$ .

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	collector		
2	collector		
3	base		
4	emitter		
5	collector		
6	collector		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4032PD	SC-74	plastic surface-mounted package; 6 leads	SOT457

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4032PD	ZG

## 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

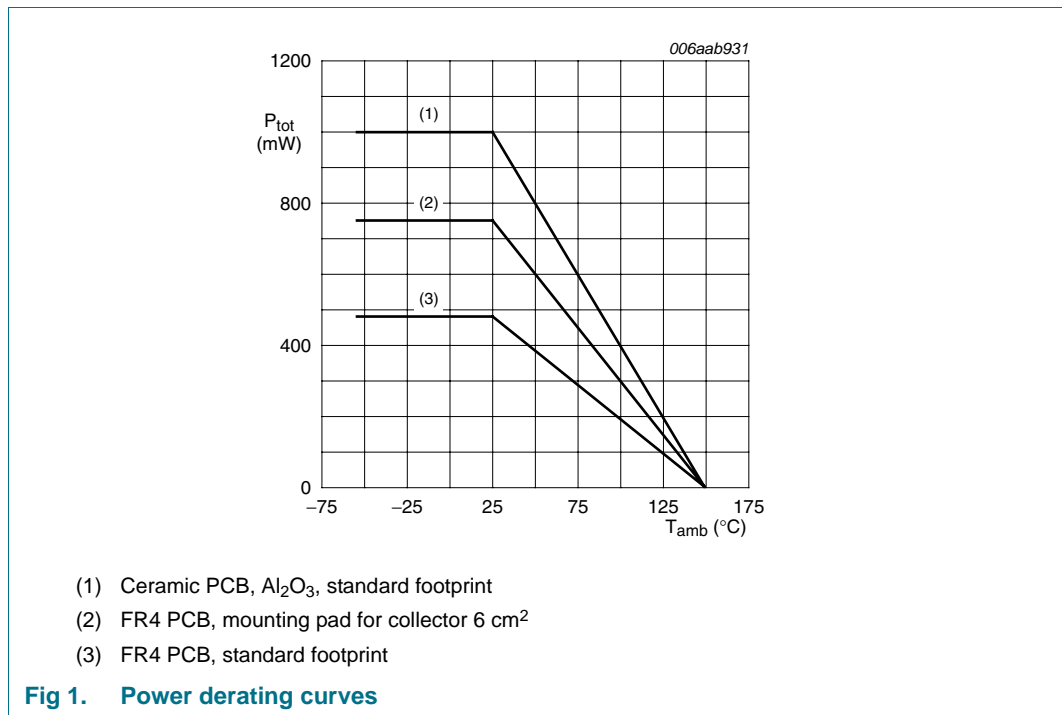
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter	-	-30	V
$V_{CEO}$	collector-emitter voltage	open base	-	-30	V
$V_{EBO}$	emitter-base voltage	open collector	-	-5	V
$I_C$	collector current		-	-2.7	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-5	A
$I_B$	base current		-	-0.5	A

**Table 5. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1] -	480	mW
			[2] -	750	mW
			[3] -	1	W
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-55	+150	°C
$T_{stg}$	storage temperature		-65	+150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

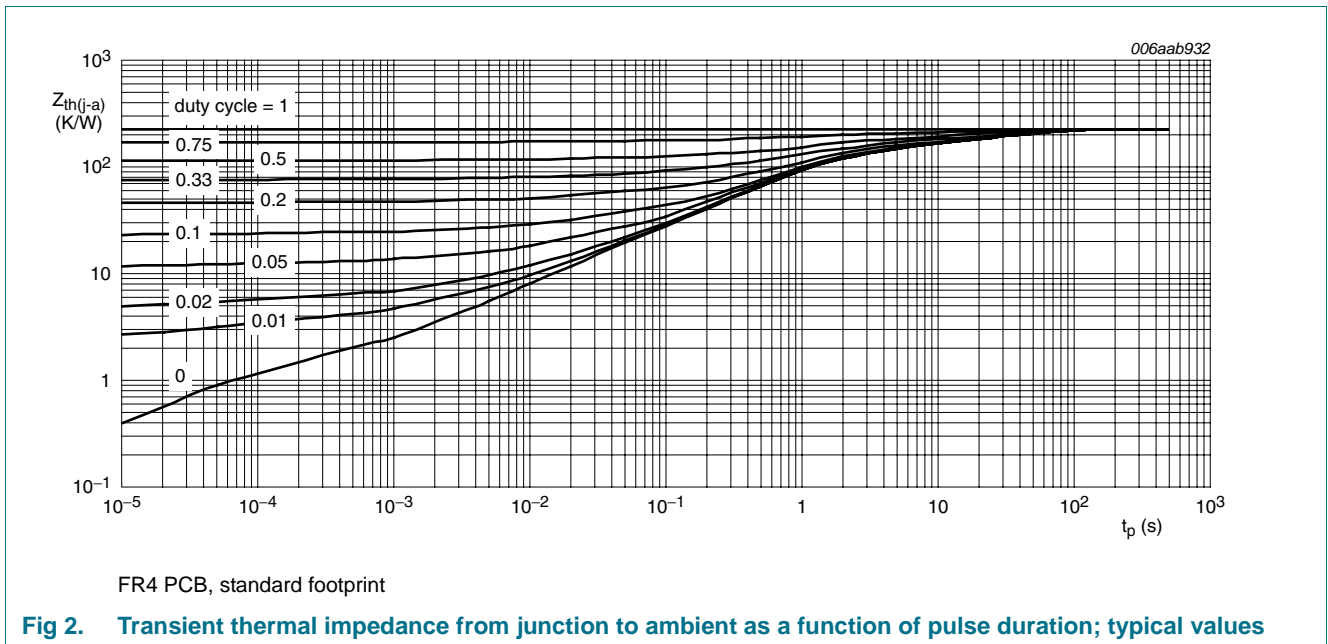


**6. Thermal characteristics**

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	260	K/W
			[2]	-	-	160	K/W
			[3]	-	-	125	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	45	K/W	

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.



**Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

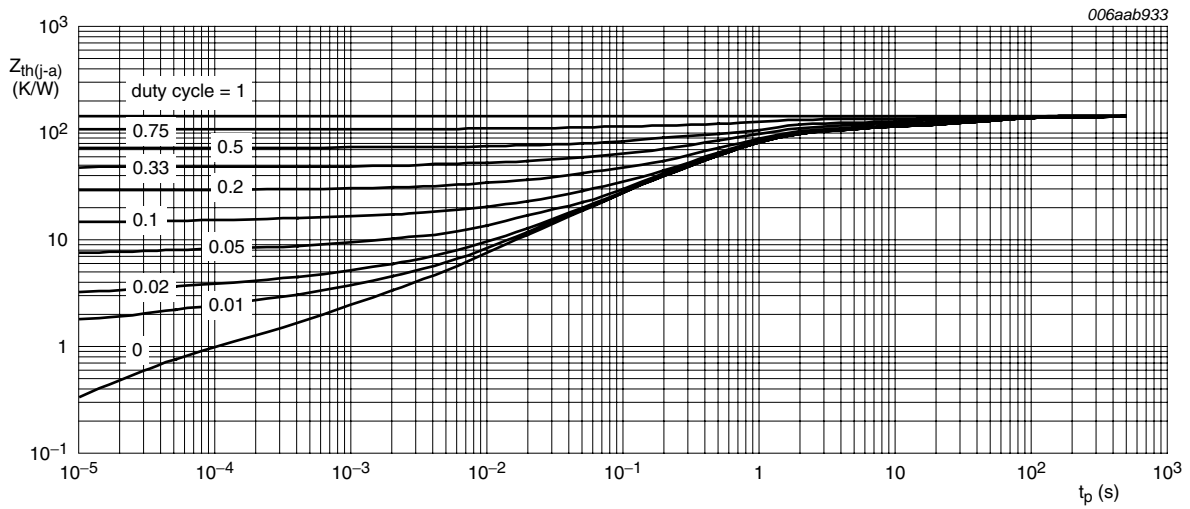


Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

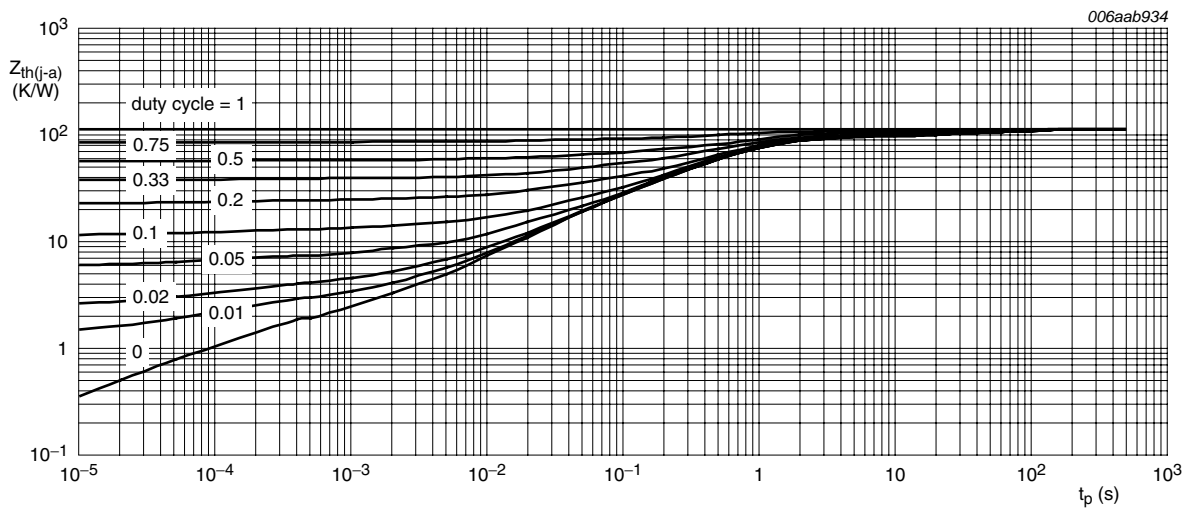


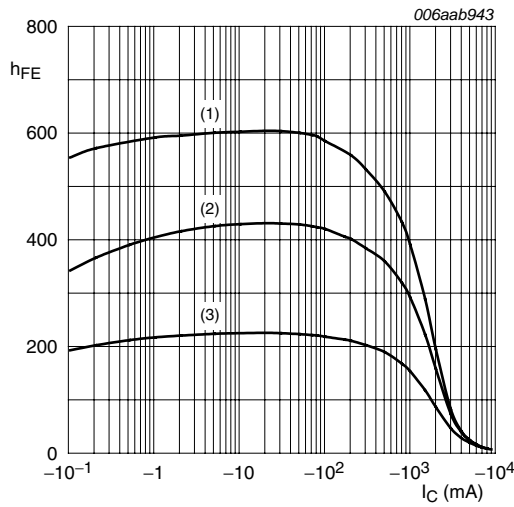
Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 7. Characteristics

**Table 7. Characteristics**
 $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

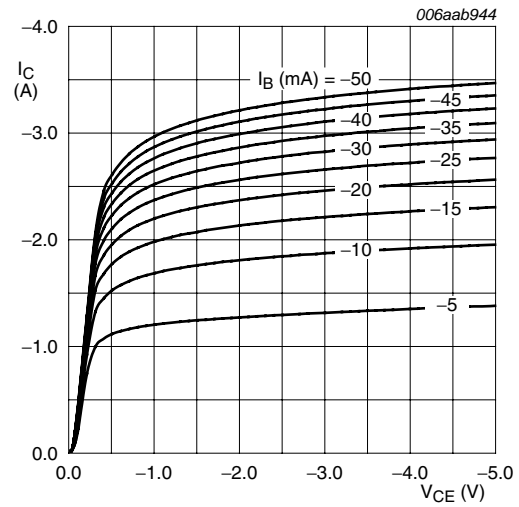
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA	
		$V_{CB} = -30\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	-55	$\mu\text{A}$	
$I_{CES}$	collector-emitter cut-off current	$V_{CE} = -24\text{ V}; V_{BE} = 0\text{ V}$	-	-	-100	nA	
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-100	nA	
$h_{FE}$	DC current gain	$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	[1]	200	350	-	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}$	[1]	200	300	-	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	[1]	100	160	-	
		$V_{CE} = -2\text{ V}; I_C = -4\text{ A}$	[1]	25	40	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	-	-87	-130	mV	
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	[1]	-	-140	-210	mV
		$I_C = -1\text{ A}; I_B = -10\text{ mA}$	[1]	-	-205	-300	mV
		$I_C = -2\text{ A}; I_B = -40\text{ mA}$	[1]	-	-280	-420	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	[1]	-	-170	-255	mV
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = -3\text{ A}; I_B = -300\text{ mA}$	[1]	-	88	130	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -1\text{ A}; I_B = -100\text{ mA}$	[1]	-	-0.83	-0.9	V
		$I_C = -3\text{ A}; I_B = -300\text{ mA}$	[1]	-	-1.11	-1.2	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	-	-0.85	-0.95	V	
$t_d$	delay time	$V_{CC} = -12.5\text{ V}; I_C = -1\text{ A}; I_{Bon} = -0.05\text{ A}; I_{Boff} = 0.05\text{ A}$	-	20	-	ns	
$t_r$	rise time		-	55	-	ns	
$t_{on}$	turn-on time		-	75	-	ns	
$t_s$	storage time		-	130	-	ns	
$t_f$	fall time		-	80	-	ns	
$t_{off}$	turn-off time		-	210	-	ns	
$f_T$	transition frequency	$V_{CE} = -10\text{ V}; I_C = -100\text{ mA}; f = 100\text{ MHz}$	-	104	-	MHz	
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$	-	59	-	pF	

[1] Pulse test:  $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$ .



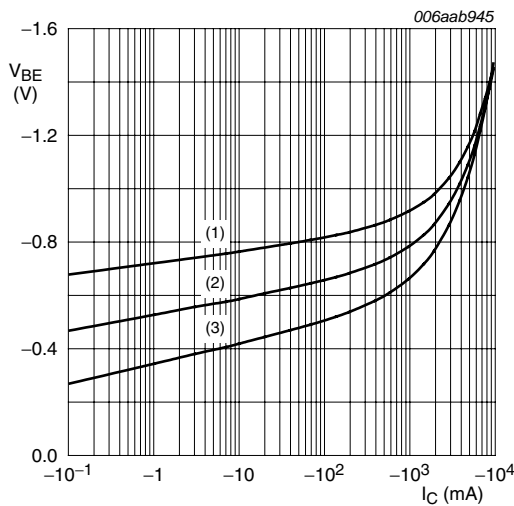
$V_{CE} = -2\text{ V}$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -55\text{ }^\circ\text{C}$

**Fig 5. DC current gain as a function of collector current; typical values**



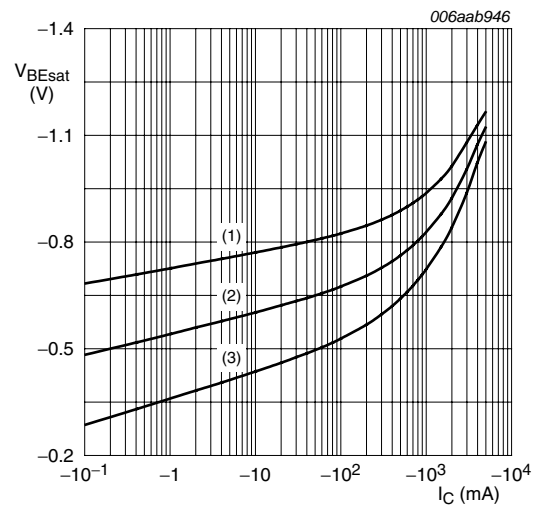
$T_{amb} = 25\text{ }^\circ\text{C}$

**Fig 6. Collector current as a function of collector-emitter voltage; typical values**



$V_{CE} = -2\text{ V}$   
 (1)  $T_{amb} = -55\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

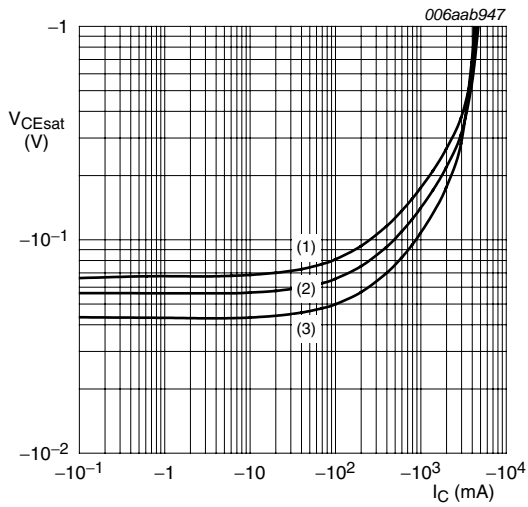
**Fig 7. Base-emitter voltage as a function of collector current; typical values**



$I_C/I_B = 20$   
 (1)  $T_{amb} = -55\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

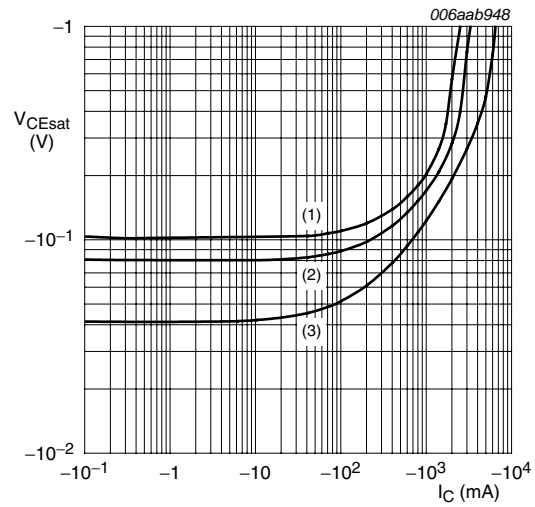
**Fig 8. Base-emitter saturation voltage as a function of collector current; typical values**





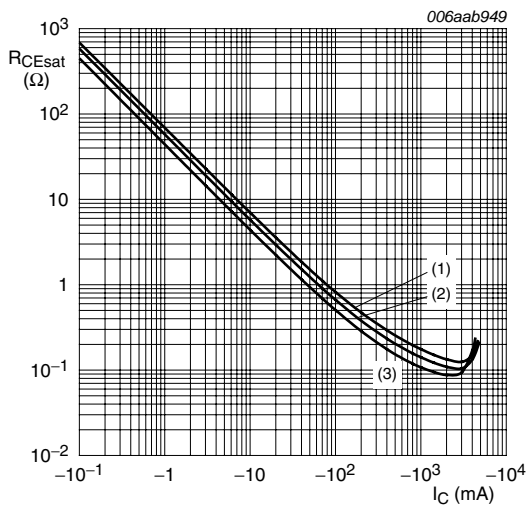
- $I_C/I_B = 20$
- (1)  $T_{amb} = 100\text{ °C}$
  - (2)  $T_{amb} = 25\text{ °C}$
  - (3)  $T_{amb} = -55\text{ °C}$

**Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values**



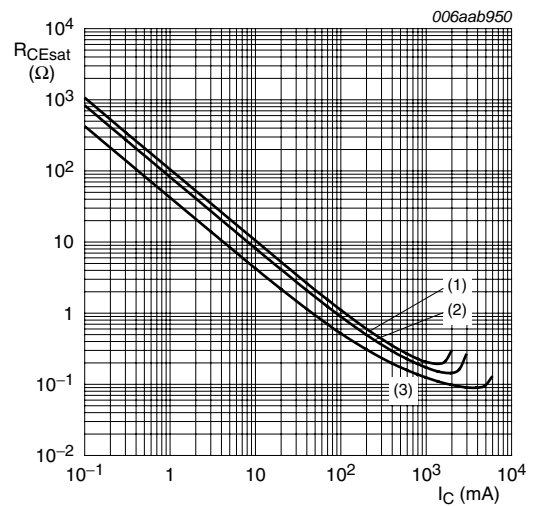
- $T_{amb} = 25\text{ °C}$
- (1)  $I_C/I_B = 100$
  - (2)  $I_C/I_B = 50$
  - (3)  $I_C/I_B = 10$

**Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values**



- $I_C/I_B = 20$
- (1)  $T_{amb} = 100\text{ °C}$
  - (2)  $T_{amb} = 25\text{ °C}$
  - (3)  $T_{amb} = -55\text{ °C}$

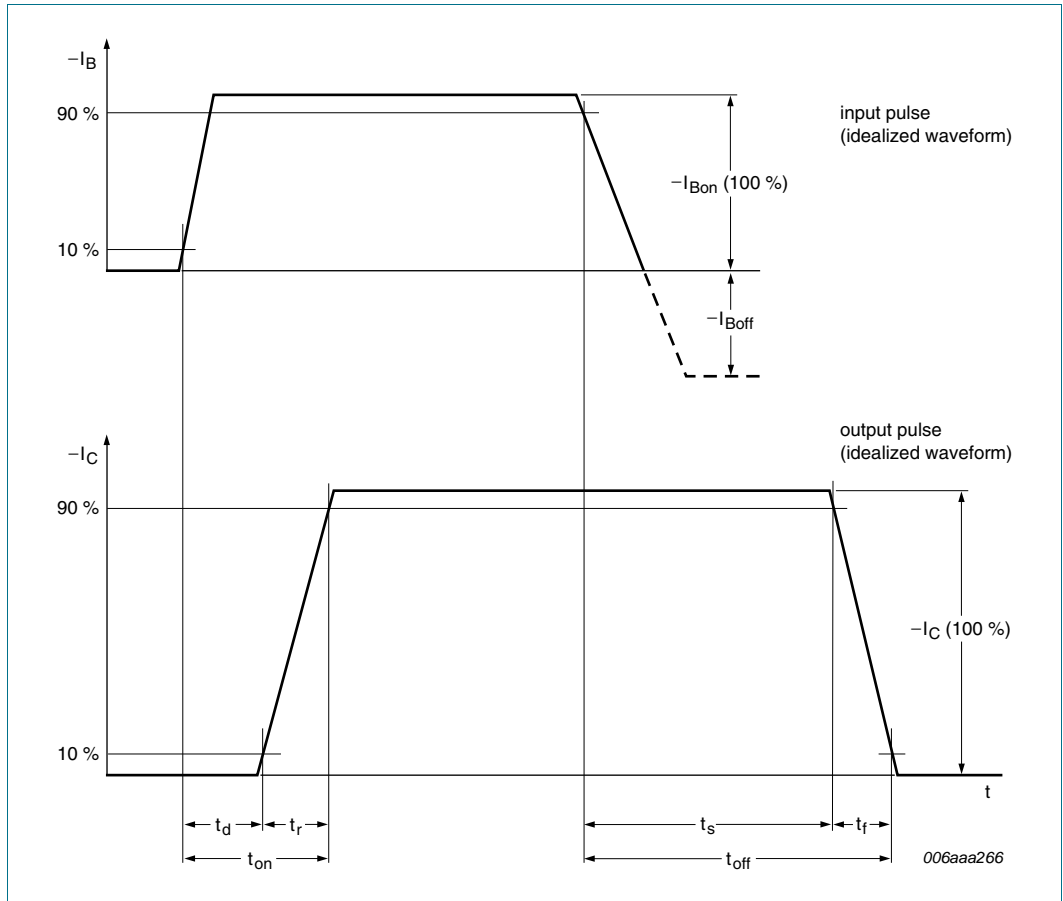
**Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values**



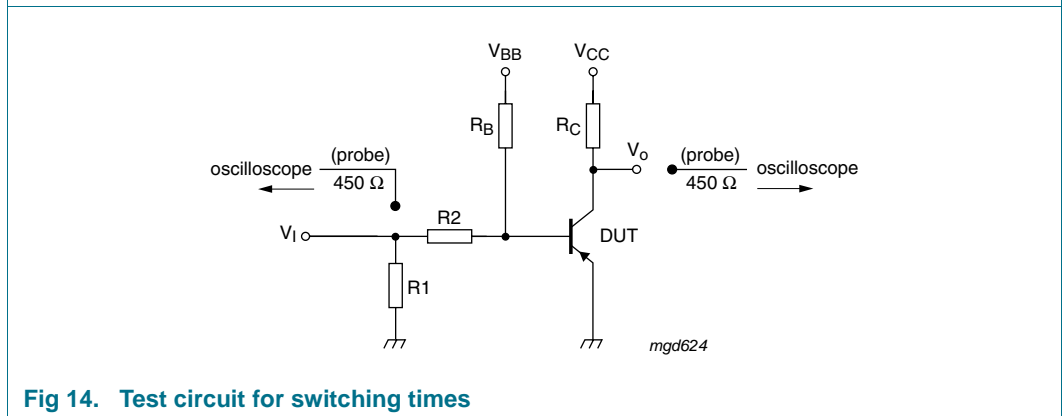
- $T_{amb} = 25\text{ °C}$
- (1)  $I_C/I_B = 100$
  - (2)  $I_C/I_B = 50$
  - (3)  $I_C/I_B = 10$

**Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values**

**8. Test information**



**Fig 13. BISS transistor switching time definition**

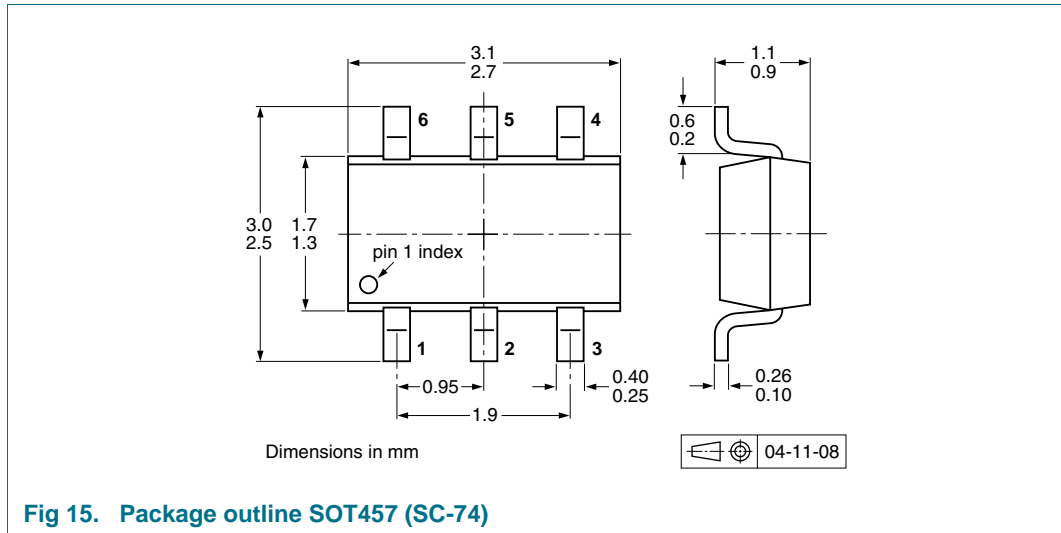


**Fig 14. Test circuit for switching times**

**8.1 Quality information**

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 9. Package outline



## 10. Packing information

**Table 8. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

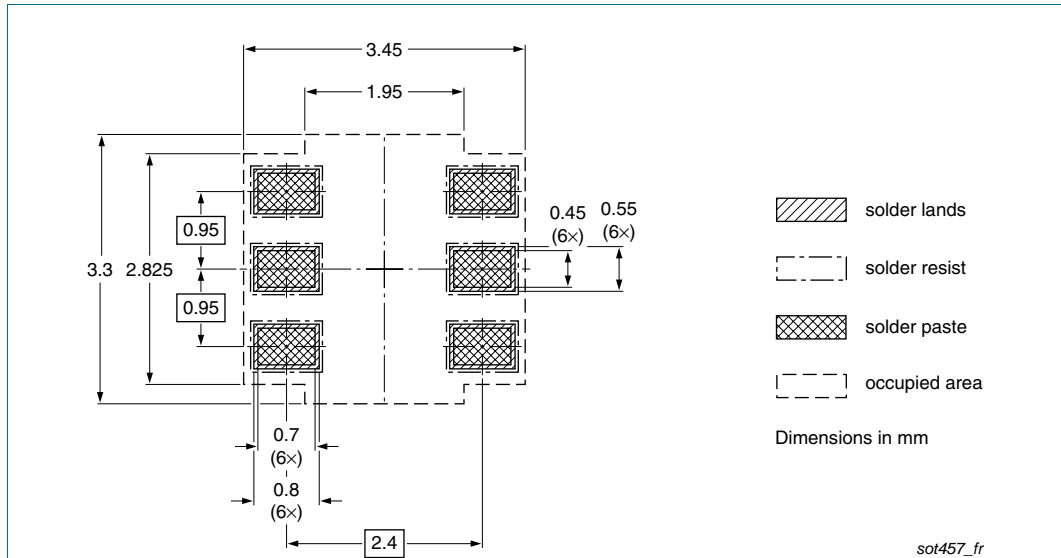
Type number	Package	Description	Packing quantity	
			3000	10000
PBSS4032PD	SOT457	4 mm pitch, 8 mm tape and reel	[2] -115	-135
		4 mm pitch, 8 mm tape and reel	[3] -215	-235

[1] For further information and the availability of packing methods, see [Section 14](#).

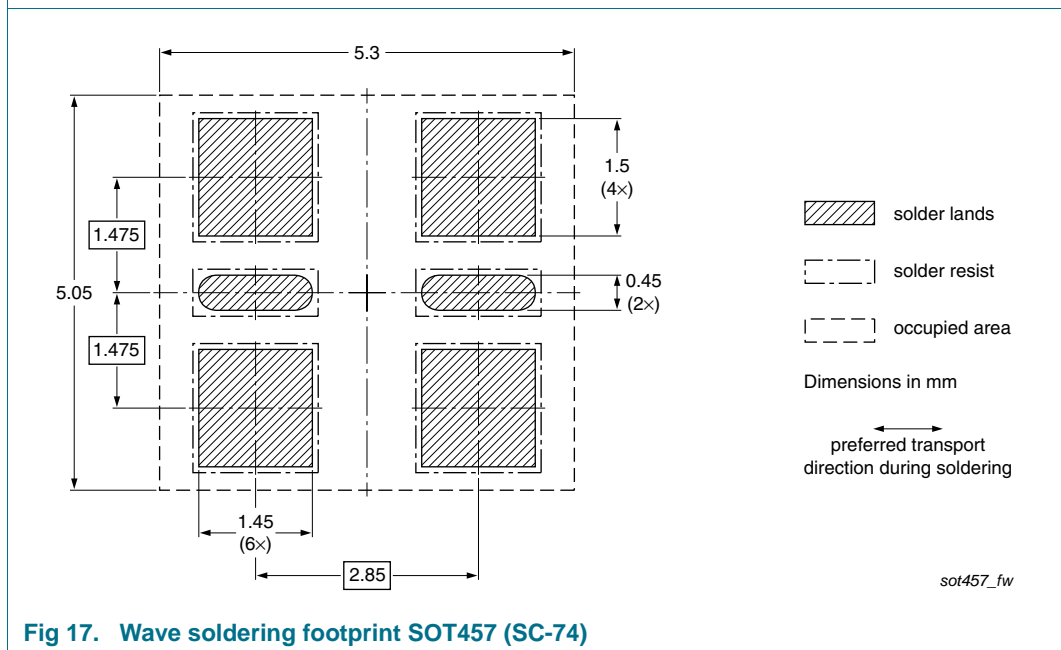
[2] T1: normal taping

[3] T2: reverse taping

## 11. Soldering



**Fig 16. Reflow soldering footprint SOT457 (SC-74)**



**Fig 17. Wave soldering footprint SOT457 (SC-74)**

## 12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4032PD_1	20100127	Product data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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 Date of release: 27 January 2010  
 Document identifier: PBSS4032PD\_1

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