PCMFxUSB3BA/C series

Common-mode EMI filter for differential channels with integrated bidirectional ESD protection

Rev. 3 — 25 November 2019 Product data sheet

1. General description

Common-mode ElectroMagnetic Interference (EMI) filters with integrated bidirectional ElectroStatic Discharge (ESD) protection for one, two and three differential channels. The devices are designed to provide low insertion loss for differential high-speed signals on each channel while unwanted common-mode signals are attenuated.

Each differential channel incorporates two signal lines that are coupled by integrated coils. Diodes provide protection to downstream components from ESD voltages up to ±15 kV on each signal line.

Table 1. Product overview

Type number	Number of channels	Package Name
PCMF1USB3BA/C	1	WLCSP5
PCMF2USB3BA/C	2	WLCSP10
PCMF3USB3BA/C	3	WLCSP15

2. Features and benefits

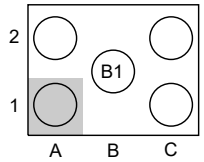
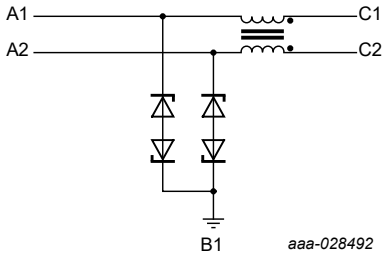
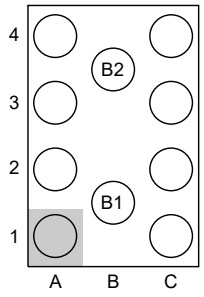
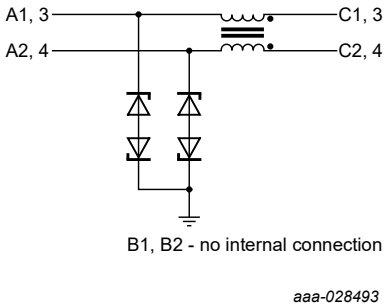
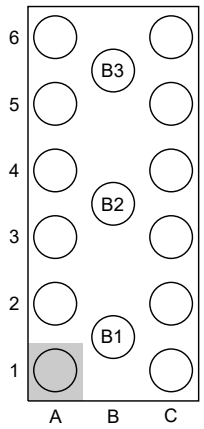
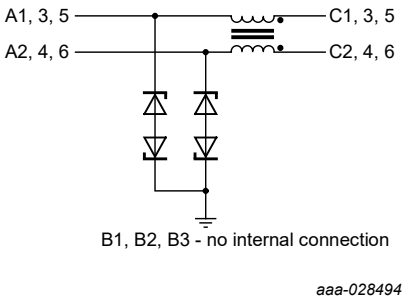
- One, two and three differential channels common-mode EMI filters with integrated ESD protection
- ESD protection up to ±15 kV contact discharge according to IEC 61000-4-2
- Superior common-mode suppression over a wide frequency range
- Superior RF performance compared to other integrated filters or discrete filters with external ESD protection
- Extremely high symmetry between line pairs
- Industry-standard Wafer-Level Chip-Scale Packages: WLCSP5, 10 and 15 for smaller footprint

3. Applications

- Smartphone, cellular and cordless phone
- USB3.2, USB2.0, HDMI2.0, HDMI1.4
- General-purpose downstream ESD protection for differential data lines
- Tablet PC and Mobile Internet Device (MID)
- MIPI M-PHY and D-PHY as used in Camera Serial Interface (CSI) and Display Serial Interface (DSI)

4. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
PCMF1USB3BA/C (WLCSP5_2-1-2)				
A1	CH1_IN+	channel 1+, external	 Transparent top view **WLCSP5_2-1-2**	
A2	CH1_IN-	channel 1-, external		
B1	GND_CH1	ground channel 1		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT-	channel 1-, internal		
PCMF2USB3BA/C (WLCSP10_4-2-4)				
A1	CH1_IN+	channel 1+, external	 Transparent top view **WLCSP10_4-2-4**	
A2	CH1_IN-	channel 1-, external		
A3	CH2_IN+	channel 2+, external		
A4	CH2_IN-	channel 2-, external		
B1	GND_CH1	ground channel 1		
B2	GND_CH2	ground channel 2		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT-	channel 1-, internal		
C3	CH2_OUT+	channel 2+, internal		
C4	CH2_OUT-	channel 2-, internal		
PCMF3USB3BA/C (WLCSP15_6-3-6)				
A1	CH1_IN+	channel 1+, external	 Transparent top view **WLCSP15_6-3-6**	
A2	CH1_IN-	channel 1-, external		
A3	CH2_IN+	channel 2+, external		
A4	CH2_IN-	channel 2-, external		
A5	CH3_IN+	channel 3+, external		
A6	CH3_IN-	channel 3-, external		
B1	GND_CH1	ground channel 1		
B2	GND_CH2	ground channel 2		
B3	GND_CH3	ground channel 3		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT-	channel 1-, internal		
C3	CH2_OUT+	channel 2+, internal		
C4	CH2_OUT-	channel 2-, internal		
C5	CH3_OUT+	channel 3+, internal		
C6	CH3_OUT-	channel 3-, internal		

5. Ordering information

Table 3. Ordering information

Type number	Package	
	Name	Description
PCMF1USB3BA/C	WLCSP5	wafer level chip-size package; 5 bumps (2-1-2)
PCMF2USB3BA/C	WLCSP10	wafer level chip-size package; 10 bumps (4-2-4)
PCMF3USB3BA/C	WLCSP15	wafer level chip-size package; 15 bumps (6-3-6)

6. Marking

Table 4. Marking codes

Type number	Marking code
PCMF1USB3BA/C	PF1A
PCMF2USB3BA/C	PF2A
PCMF3USB3BA/C	PF3A

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			-4	4	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4;all input pins to ground				
		• contact discharge		-15	15	kV
		• air discharge		-15	15	kV
		IEC 61000-4-2, level 4;all output pins to ground				
		• contact discharge		-2	2	kV
		• air discharge		-2	2	kV
I_{PPM}	rated peak-pulse current	t_p = 8/20 µs		-7.5	7.5	A
T_{stg}	storage temperature			-40	+125	°C
T_{amb}	ambient temperature			-40	+125	°C

8. Characteristics

8.1. Channel characteristics

Table 6. Channel characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	parameter	Conditions		Min	Typ	Max	Unit
$R_{S(ch)}$	channel series resistance	single line; input to output		-	2.2	-	Ω
C_d	diode capacitance	f = 1 MHz; V_I = 2.5 V	[1]	-	0.3	-	pF
I_{RM}	reverse leakage current	per line; V_I = 4 V		-	1	100	nA
V_{BR}	breakdown voltage	I_R = 1 mA		6	9	-	V
R_{dyn}	dynamic resistance	TLP; positive transient	[2]	-	0.29	-	Ω
		TLP; negative transient	[2]	-	0.29	-	Ω

[1] This parameter is guaranteed by design

[2] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 70 ns to 90 ns.

8.2. Frequency characteristics

Table 7. Frequency characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Differential mode: S_{dd21}							
f_{-3dB}	cut-off frequency		[1]	-	10	-	GHz

[1] Normalized to attenuation at 1 MHz.

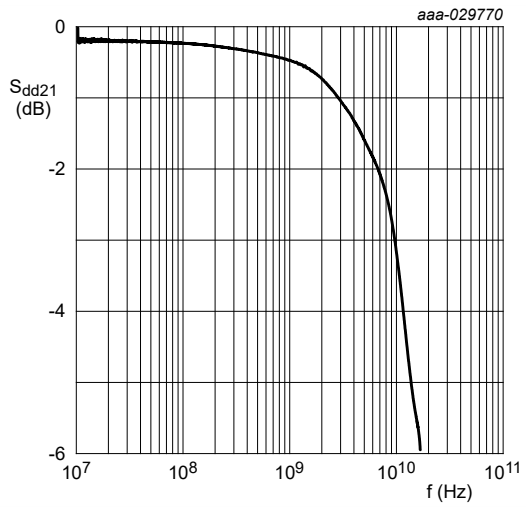


Fig. 1. Differential mode insertion loss; typical values

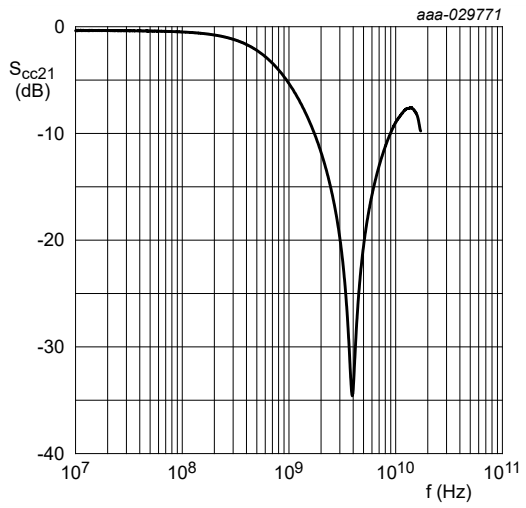
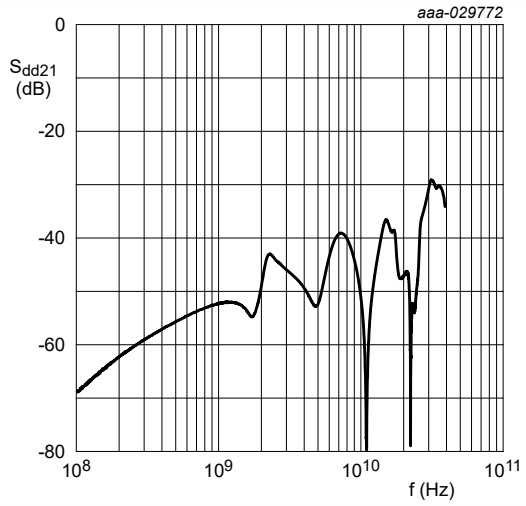
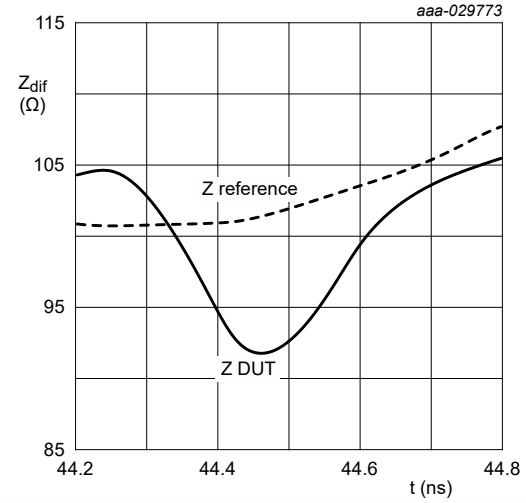


Fig. 2. Common-mode insertion loss; typical values



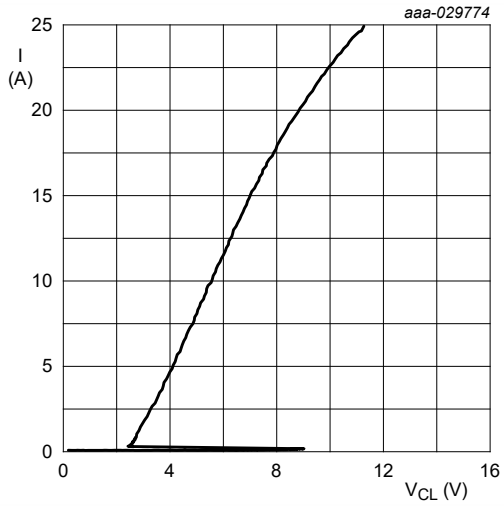
CH1 to CH2

Fig. 3. Differential crosstalk; typical values



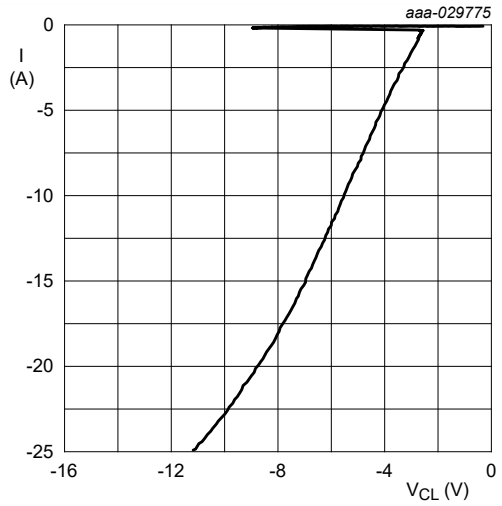
t_r = 200 ps

Fig. 4. Differential Time Domain Reflectometer (TDR) plot; typical values



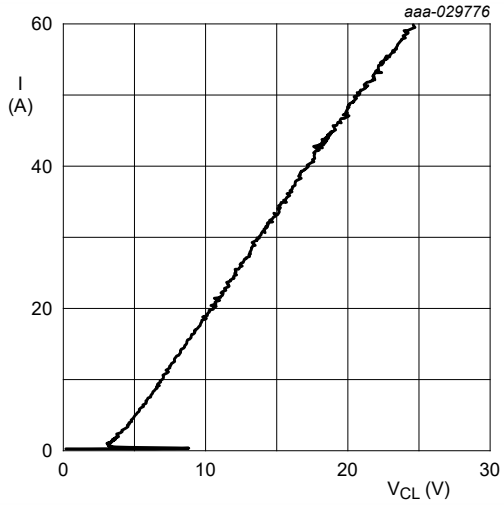
Transmission Line Pulse (TLP) = 100 ns;
measured CH_IN to GND

Fig. 5. Dynamic resistance with positive clamping; typical values



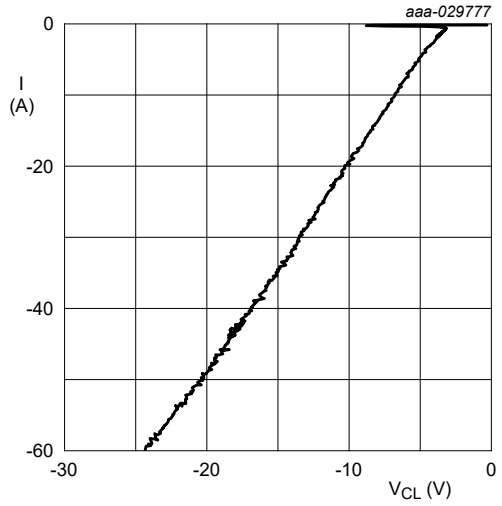
Transmission Line Pulse (TLP) = 100 ns;
measured CH_IN to GND

Fig. 6. Dynamic resistance with negative clamping; typical values



Very-Fast Transmission Line Pulse
(VF-TLP) = 5 ns;
measured CH_IN to GND

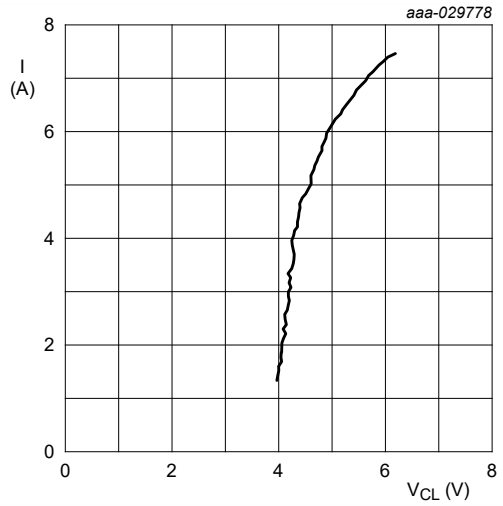
Fig. 7. Dynamic resistance with positive clamping; typical values



Very-Fast Transmission Line Pulse
(VF-TLP) = 5 ns;
measured CH_IN to GND

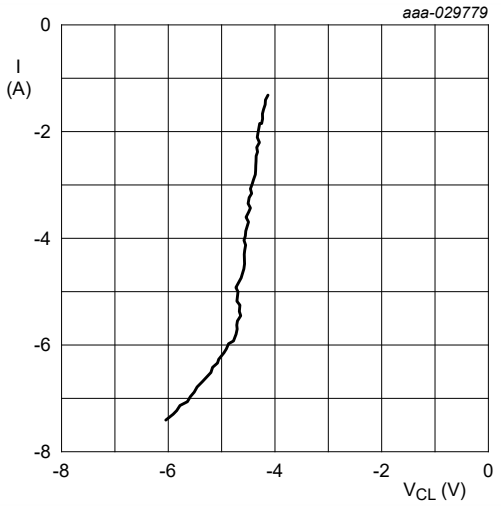
Fig. 8. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



IEC61000-4-5; t_p = 8/20 µs; positive pulse

Fig. 9. Dynamic resistance with positive clamping; typical values



IEC61000-4-5; t_p = 8/20 µs; negative pulse

Fig. 10. Dynamic resistance with negative clamping; typical values

9. Application information

The device is designed to provide high-level ESD protection for differential high-speed data line pairs such as:

- USB 3.2
- HDMI 2.0
- Transition-Minimized Differential Signaling (TMDS)
- DisplayPort
- external Serial Advanced Technology Attachment (eSATA)
- Low Voltage Differential Signaling (LVDS)

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the protected signal lines to unlimited current sources like, for example, a battery.

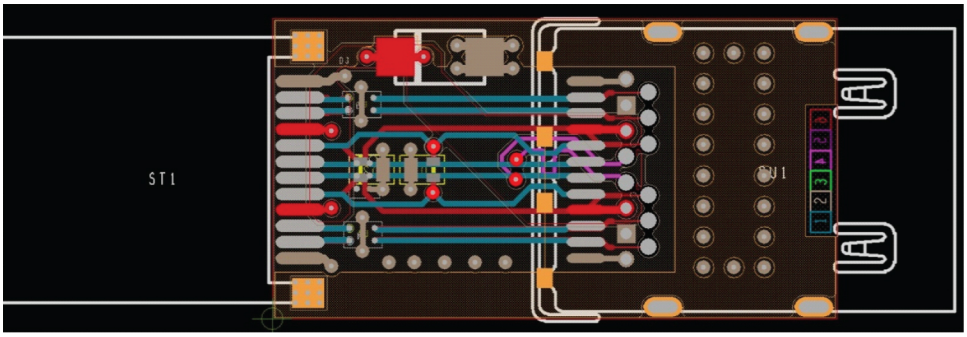
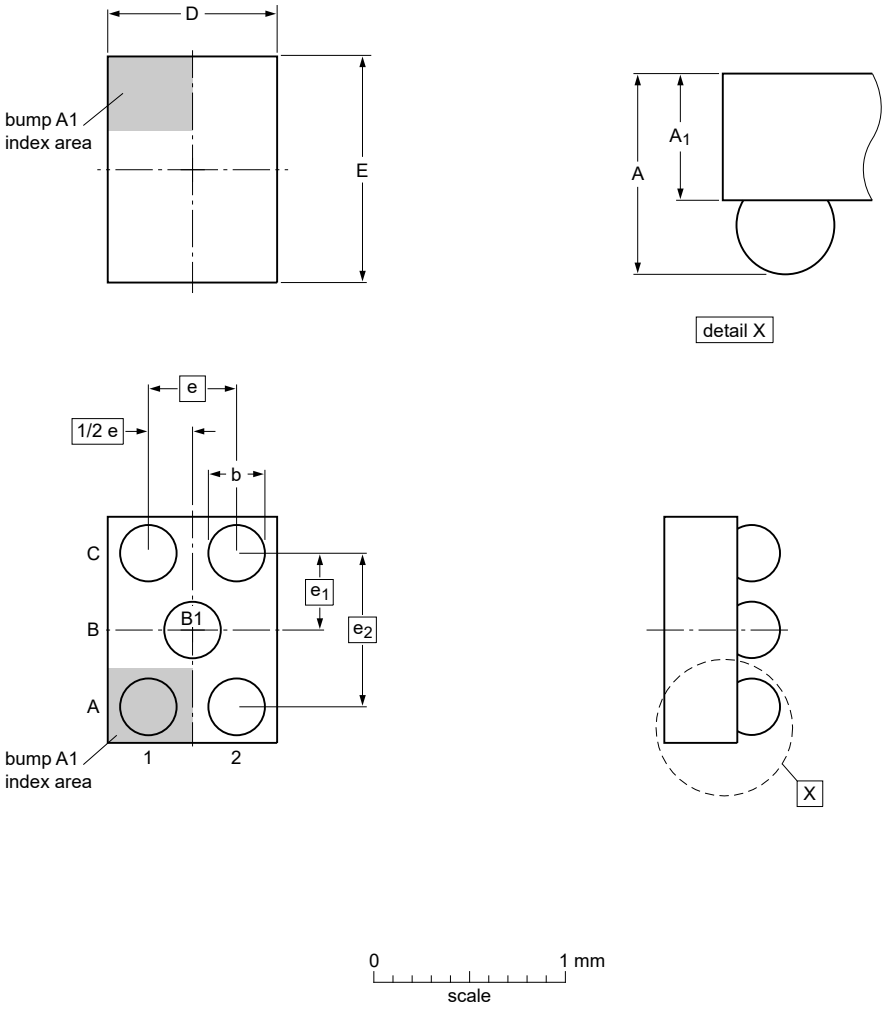


Fig. 11. Application diagram: protecting the differential data lines of a USB Type-C connector evaluation dongle with PCMF1USB3BA/C

Since the SuperSpeed TX/RX lines are separated by GND or VBUS from the Hi-Speed lines, PCMF1USB3BA/C makes it easy to achieve same signal lengths, straight routing, and optimal positioning for ESD protection directly at the connector.

10. Package outline

WLCSP5: wafer level chip-size package; 5 bumps (2-1-2) **PCMF1USB3BA/C**



Dimensions (mm are the original dimensions)

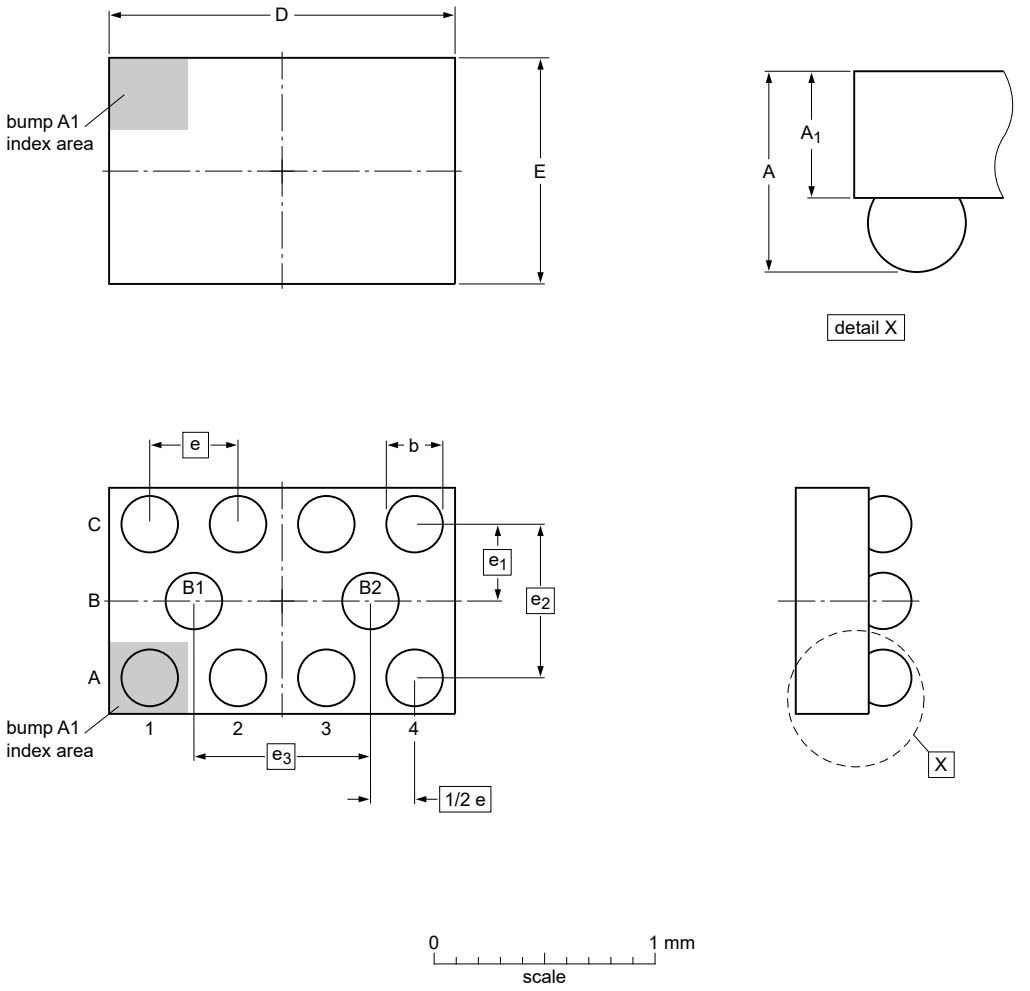
Unit		A	A_1	b	D	E	e	e_1	e_2
mm	max	0.64	0.42	0.31	0.82	1.22			
	nom	0.61	0.41	0.26	0.77	1.17	0.40	0.40	0.80
	min	0.58	0.40	0.21	0.72	1.12			

pcmf1usb3ba-c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCMF1USB3BA/C						~~19-03-20~~ 19-04-02

Fig. 12. Package outline WLCSP5

WLCSP10: wafer level chip-size package; 10 bumps (4-2-4) **PCMF2USB3BA/C**



Dimensions (mm are the original dimensions)

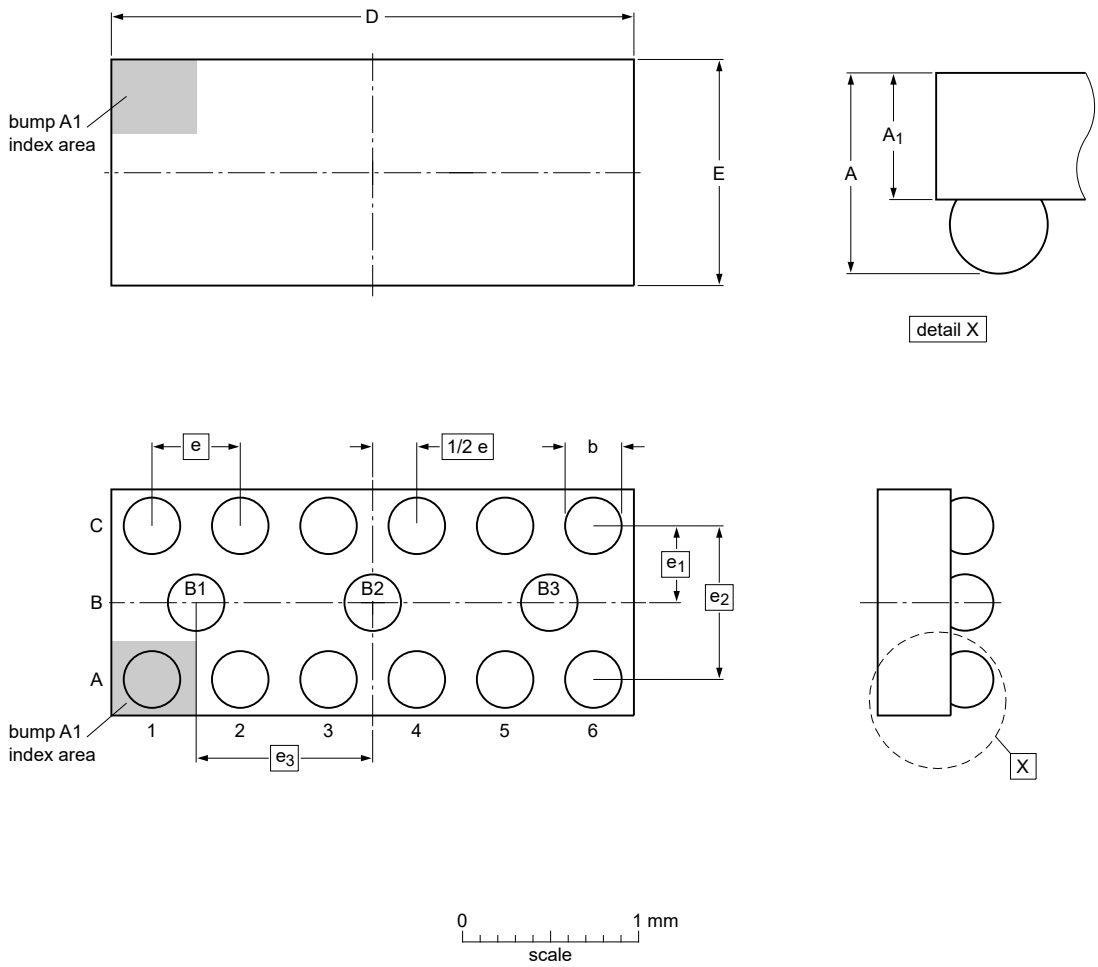
Unit		A	A_1	b	D	E	e	e_1	e_2	e_3
mm	max	0.64	0.42	0.31	1.62	1.22				
	nom	0.61	0.41	0.26	1.57	1.17	0.40	0.40	0.80	0.80
	min	0.58	0.40	0.21	1.52	1.12				

pcmf2usb3ba-c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCMF2USB3BA/C						~~19-03-20~~ 19-04-02

Fig. 13. Package outline WLCSP10

WLCSP15: wafer level chip-size package; 15 bumps (6-3-6) **PCMF3USB3BA/C**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e	e_1	e_2	e_3
	max	0.64	0.42	0.31	2.42	1.22				
mm	nom	0.61	0.41	0.26	2.37	1.17	0.40	0.40	0.80	0.80
	min	0.58	0.40	0.21	2.32	1.12				

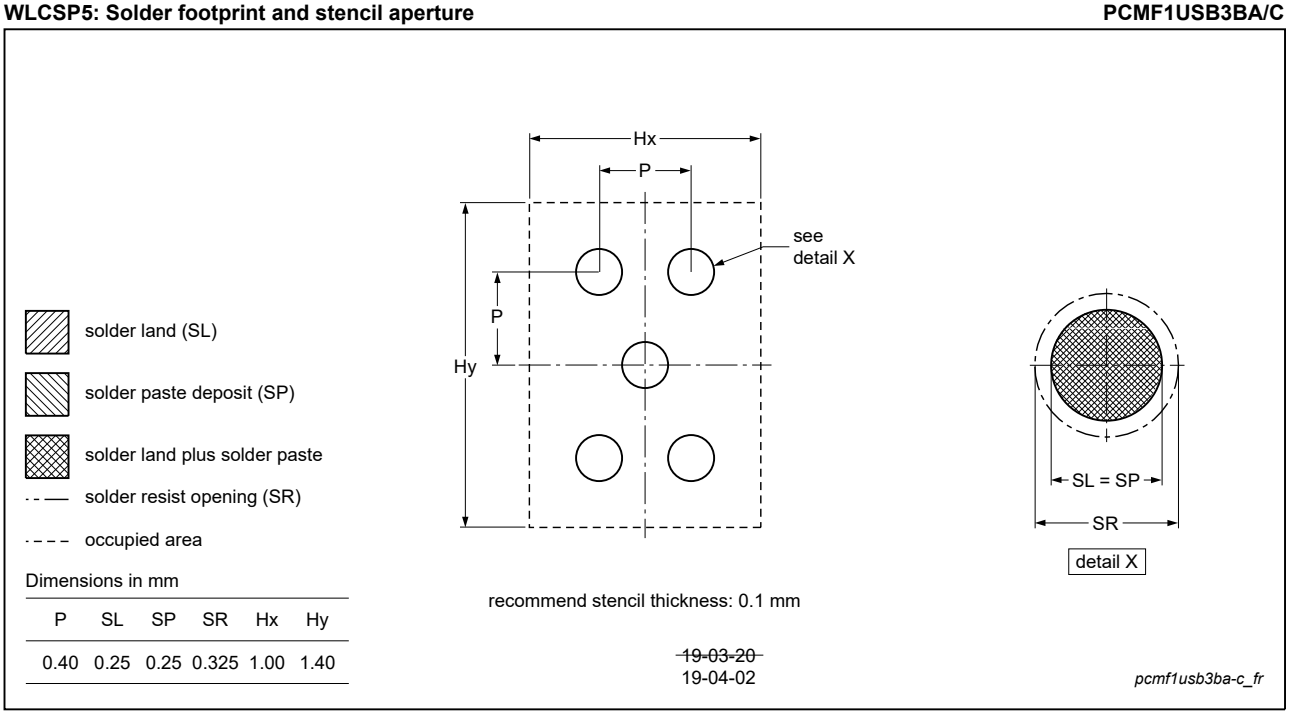
pcmf3usb3ba-c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCMF3USB3BA/C						19-03-20

Fig. 14. Package outline WLCSP15

11. Soldering

WLCSP5: Solder footprint and stencil aperture **PCMF1USB3BA/C**

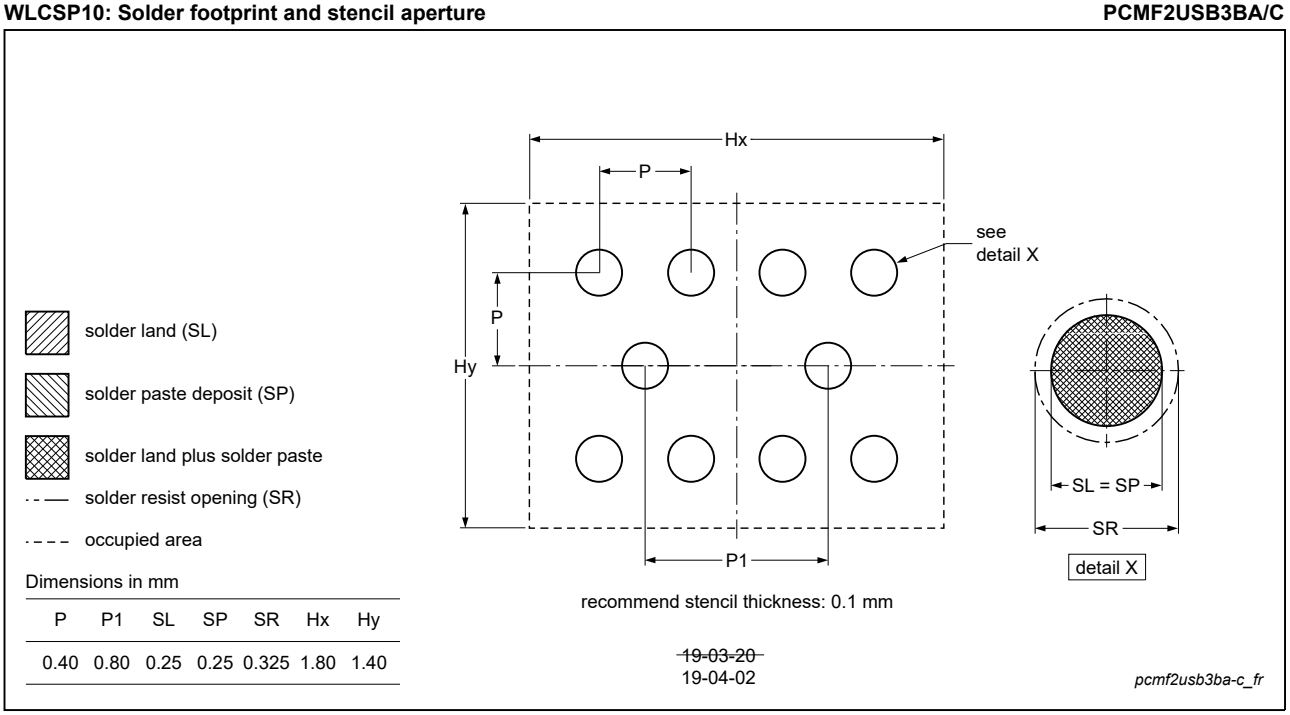


Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.40	0.25	0.25	0.325	1.00	1.40

Fig. 15. Soldering footprint WLCSP5 (PCMF1USB3BA/C)

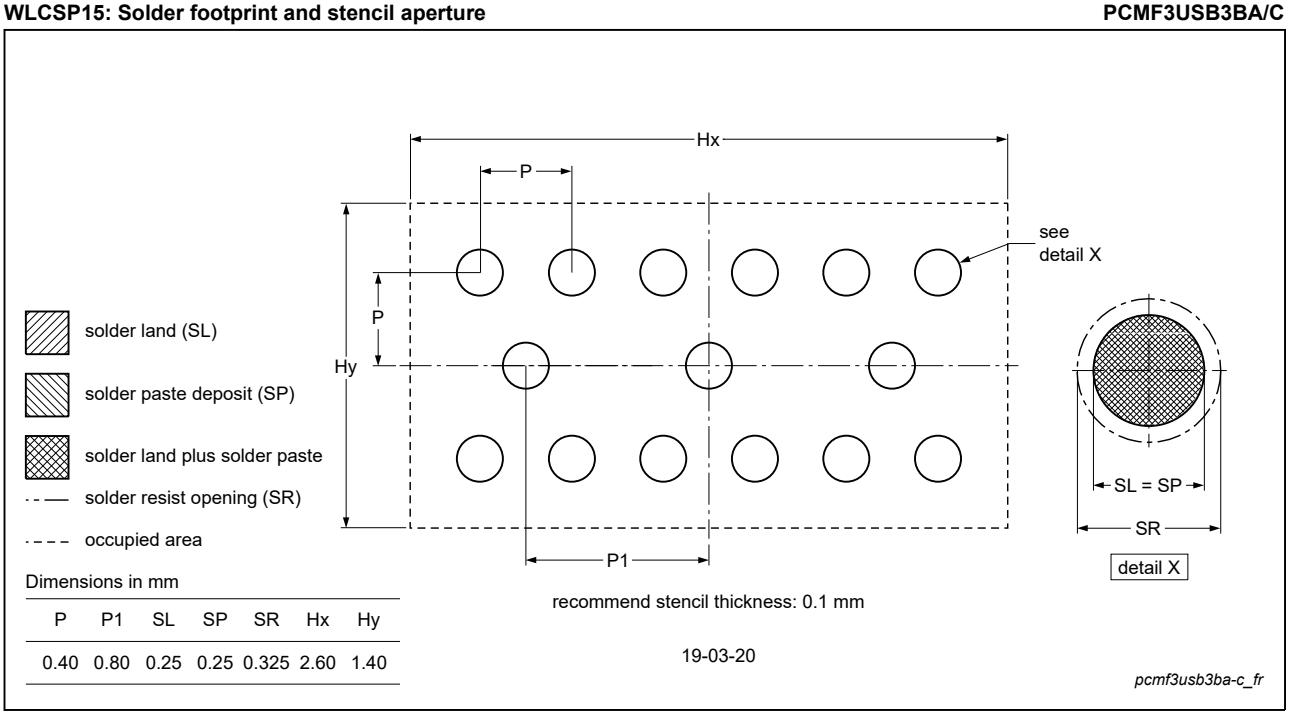
WLCSP10: Solder footprint and stencil aperture **PCMF2USB3BA/C**



Dimensions in mm

P	P1	SL	SP	SR	Hx	Hy
0.40	0.80	0.25	0.25	0.325	1.80	1.40

Fig. 16. Soldering footprint WLCSP10 (PCMF2USB3BA/C)



Dimensions in mm

P	P1	SL	SP	SR	Hx	Hy
0.40	0.80	0.25	0.25	0.325	2.60	1.40

Fig. 17. Soldering footprint WLCSP15 (PCMF3USB3BA/C)

12. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCMFXUSB3BA_C_SER v.3	20191125	Product data sheet	-	PCMFXUSB3BA_C_SER v.2
Modifications:	• Figure 2: corrected y-axis label			
PCMFXUSB3BA_C_SER v.2	20190814	Product data sheet	-	PCMFXUSB3BA_C_SER v.1
PCMFXUSB3BA_C_SER v.1	20190408	Objective data sheet	-	-

Contents

For more information, please visit: http://www.nexperia.com
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Date of release: 25 November 2019

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