# PDTA143/114/124/144EQA series

## 50 V, 100 mA PNP resistor-equipped transistors

Rev. 1 — 18 December 2015 Product data sheet

## 1. Product profile

### 1.1 General description

100 mA PNP Resistor-Equipped Transistor (RET) family in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

**Table 1. Product overview**

| Type number | R1 | R2 | Nexperia | NPN complement |
|---|---|---|---|---|
| PDTA143EQA | 4.7 kΩ | 4.7 kΩ | DFN1010D-3 (SOT1215) | PDTC143EQA |
| PDTA114EQA | 10 kΩ | 10 kΩ | | PDTC114EQA |
| PDTA124EQA | 22 kΩ | 22 kΩ | | PDTC124EQA |
| PDTA144EQA | 47 kΩ | 47 kΩ | | PDTC144EQA |

### 1.2 Features and benefits

- 100 mA output current capability
- built-in bias resistors
- simplifies circuit design
- reduces component count
- reduced pick and place costs
- low package height of 0.37 mm
- AEC-Q101 qualified
- suitable for Automatic Optical Inspection (AOI) of solder joint

### 1.3 Applications

- digital applications
- cost saving alternative for BC847/BC857 series in digital applications
- controlling IC inputs
- switching loads

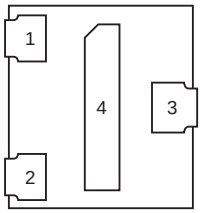
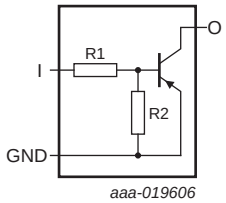
### 1.4 Quick reference data

**Table 2. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CEO}$ | collector-emitter voltage | open base | - | - | –50 | V |
| $I_O$ | output current | | - | - | –100 | mA |

## 2. Pinning information

**Table 3. Pinning**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | I | input (base) |  Transparent top view |  aaa-019606 |
| 2 | GND | GND (emitter) | | |
| 3 | O | output (collector) | | |
| 4 | O | output (collector) | | |

## 3. Ordering information

**Table 4. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PDTA143EQA | DFN1010D-3 | plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body: 1.1 × 1.0 × 0.37 mm | SOT1215 |
| PDTA114EQA | | | |
| PDTA124EQA | | | |
| PDTA144EQA | | | |

# 4. Marking

**Table 5. Marking codes**

| Type number | Marking code |
|---|---|
| PDTA143EQA | 10 10 11 |
| PDTA114EQA | 11 01 11 |
| PDTA124EQA | 10 11 10 |
| PDTA144EQA | 10 01 11 |

## 4.1 Binary marking code description

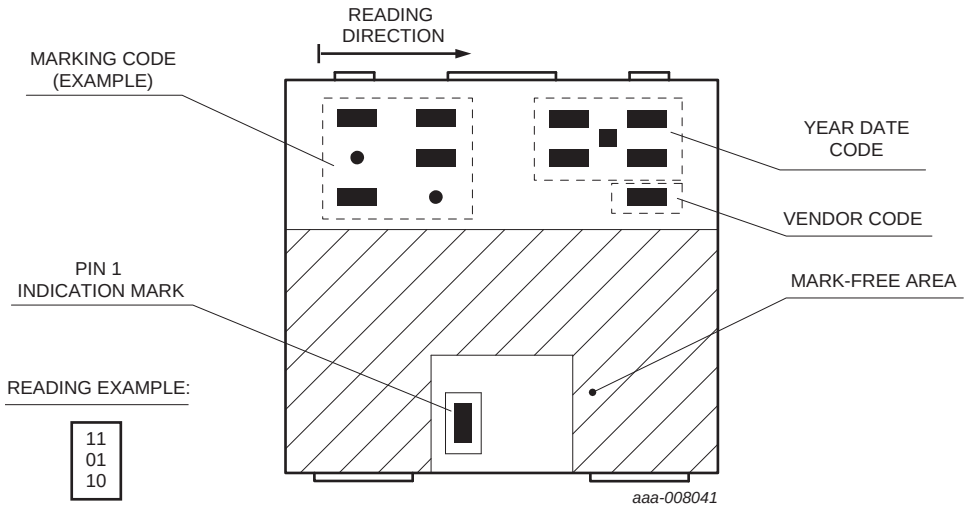



**Fig 1. SOT1215 binary marking code description**

# 5. Limiting values

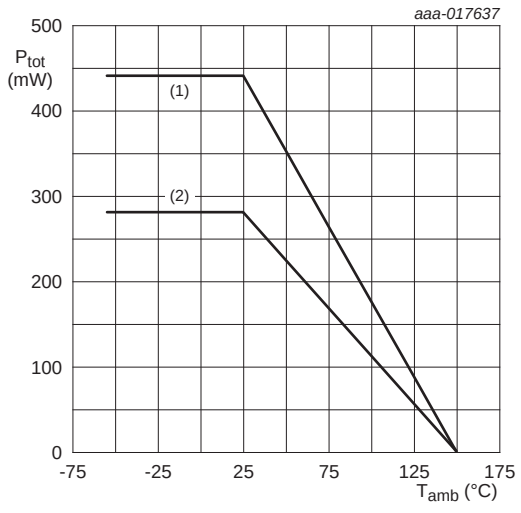
**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CBO}$ | collector-base voltage | open emitter | | - | –50 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | –50 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | | - | –10 | V |
| $V_I$ | input voltage | | | | | |
| | PDTA143EQA | | | –30 | +10 | V |
| | PDTA114EQA | | | –40 | +10 | V |
| | PDTA124EQA | | | –40 | +10 | V |
| | PDTA144EQA | | | –40 | +10 | V |
| $I_O$ | output current | | | - | –100 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 280 | mW |
| | | | [2] | - | 440 | mW |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | –55 | +150 | °C |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.




(1) FR4 PCB, 4-layer copper, standard footprint

(2) FR4 PCB, standard footprint

**Fig 2. Power derating curves**

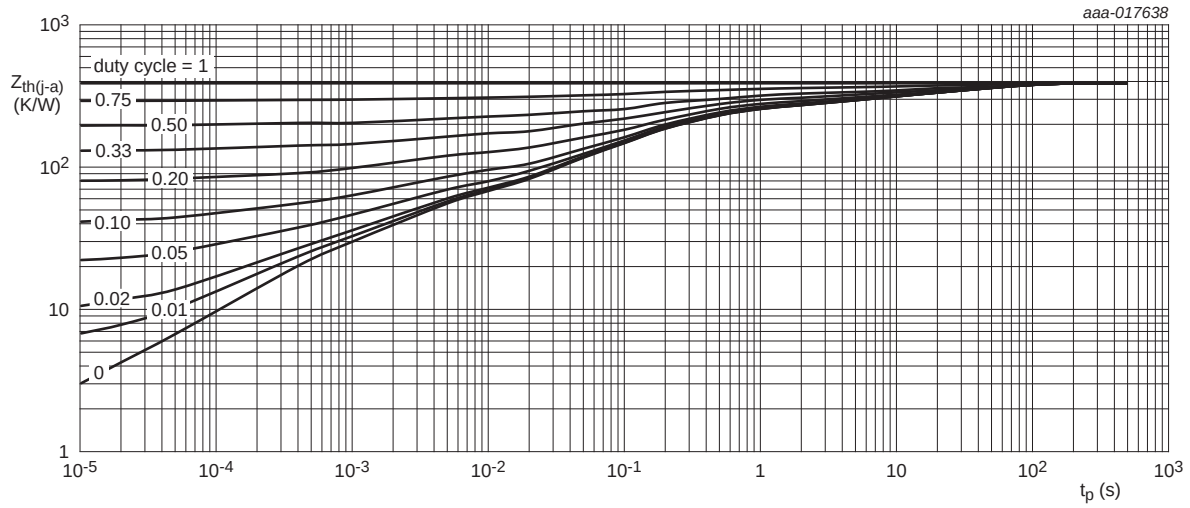
# 6. Thermal characteristics

**Table 7. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 446 | K/W |
| | | | [2] | - | - | 284 | K/W |

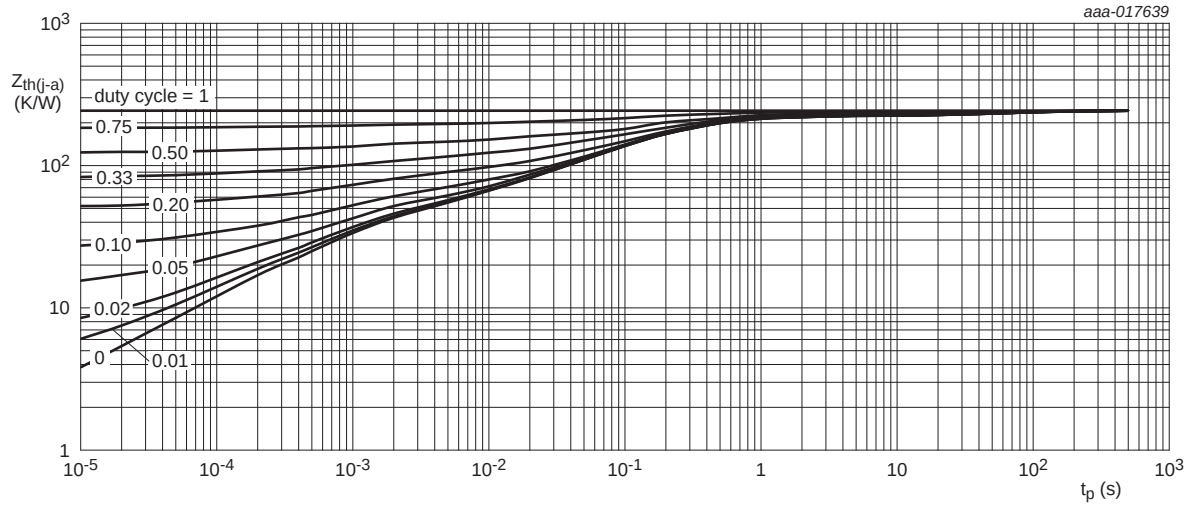
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.




FR4 PCB, single-sided copper, tin-plated and standard footprint

**Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**




FR4 PCB, 4-layer copper, tin-plated and standard footprint.

**Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

# 7. Characteristics

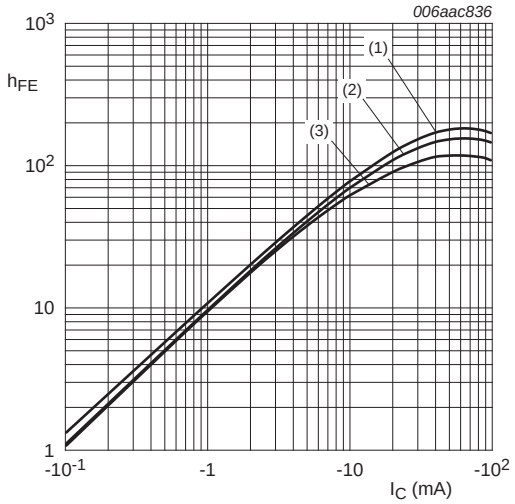
**Table 8. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = -50 V; $I_E$ = 0 A | - | - | -100 | nA |
| $I_{CEO}$ | collector-emitter cut off current | $V_{CE}$ = -30; $I_B$ = 0 A; | - | - | -1 | µA |
| | | $V_{CE}$ = -30; $I_B$ = 0 A; $T_j$ = 150 °C | - | - | -5 | µA |
| $I_{EBO}$ | emitter-base cut-off current | | | | | |
| | PDTA143EQA | $V_{EB}$ = -5 V; $I_C$ = 0 A | - | - | -900 | µA |
| | PDTA114EQA | | - | - | -400 | µA |
| | PDTA124EQA | | - | - | -180 | µA |
| | PDTA144EQA | | - | - | -90 | µA |
| $h_{FE}$ | DC current gain | | | | | |
| | PDTA143EQA | $V_{CE}$ = -5 V; $I_C$ = -10 mA | 30 | - | - | |
| | PDTA114EQA | $V_{CE}$ = -5 V; $I_C$ = -5 mA | 30 | - | - | |
| | PDTA124EQA | $V_{CE}$ = -5 V; $I_C$ = -5 mA | 60 | - | - | |
| | PDTA144EQA | $V_{CE}$ = -5 V; $I_C$ = -5 mA | 80 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = -10 mA; $I_B$ = -0.5 mA | - | - | -150 | mV |
| $V_{I(off)}$ | off-state input voltage | | | | | |
| | PDTA143EQA | $V_{CE}$ = -5 V; $I_C$ = -100 µA | - | -1.1 | -0.5 | V |
| | PDTA114EQA | | - | -1.1 | -0.8 | V |
| | PDTA124EQA | | - | -1.1 | -0.8 | V |
| | PDTA144EQA | | - | -1.2 | -0.8 | V |
| $V_{I(on)}$ | on-state input voltage | | | | | |
| | PDTA143EQA | $V_{CE}$ = -0.3 V; $I_C$ = -20 mA | -2.5 | -1.9 | - | V |
| | PDTA114EQA | $V_{CE}$ = -0.3 V; $I_C$ = -10 mA | -2.5 | -1.8 | - | V |
| | PDTA124EQA | $V_{CE}$ = -0.3 V; $I_C$ = -5 mA | -2.5 | -1.7 | - | V |
| | PDTA144EQA | $V_{CE}$ = -0.3 V; $I_C$ = -2 mA | -3 | -1.6 | - | V |
| R1 | bias resistor 1 (input) | [1] | | | | |
| | PDTA143EQA | | 3.3 | 4.7 | 6.1 | kΩ |
| | PDTA114EQA | | 7 | 10 | 13 | kΩ |
| | PDTA124EQA | | 15.4 | 22 | 28.6 | kΩ |
| | PDTA144EQA | | 33 | 47 | 61 | kΩ |
| R2/R1 | bias resistor ratio | [1] | 0.8 | 1 | 1.2 | |
| $C_c$ | collector capacitance | $V_{CB}$ = -10 V; $I_E$ = $i_e$ = 0 A; f = 1 MHz | - | - | 3 | pF |
| $f_T$ | transition frequency | $V_{CE}$ = -5 V; $I_C$ = -10 mA; f = 100 MHz [2] | - | 180 | - | MHz |

[1] See section test information for resistor calculation and test conditions.

[2] Characteristics of built-in transistor.



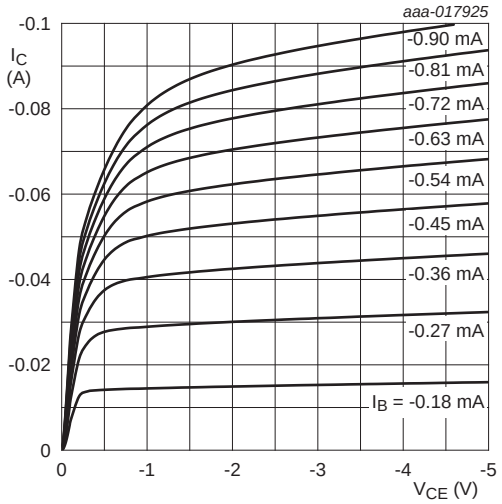

$V_{CE}$ = −5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

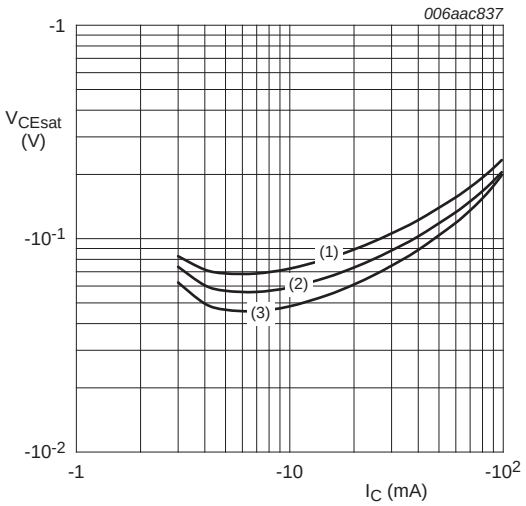
(3) $T_{amb}$ = −40 °C

**Fig 5. PDTA143EQA: DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 6. PDTA143EQA: Collector current as a function of collector-emitter voltage; typical values**



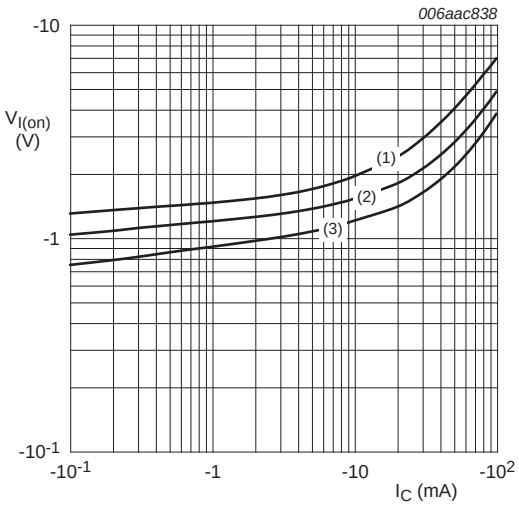

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 7. PDTA143EQA: Collector-emitter saturation voltage as a function of collector current; typical values**



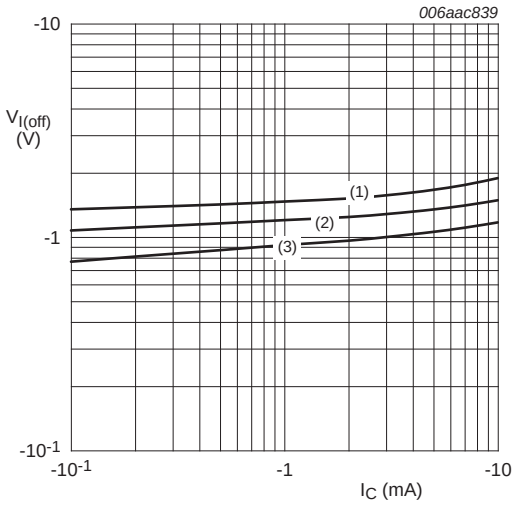

$V_{CE}$ = −0.3 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 8. PDTA143EQA: On-state input voltage as a function of collector current; typical values**



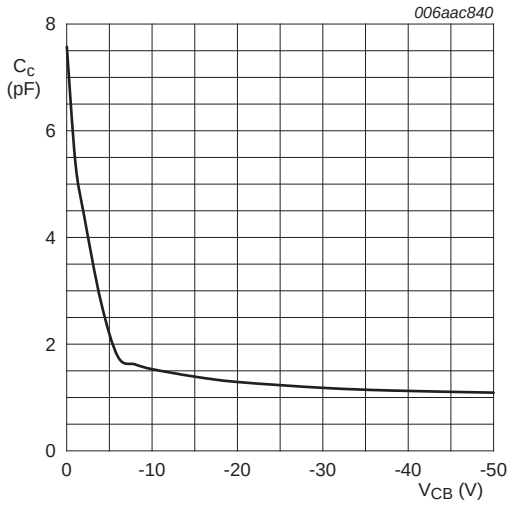

$V_{CE}$ = −5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

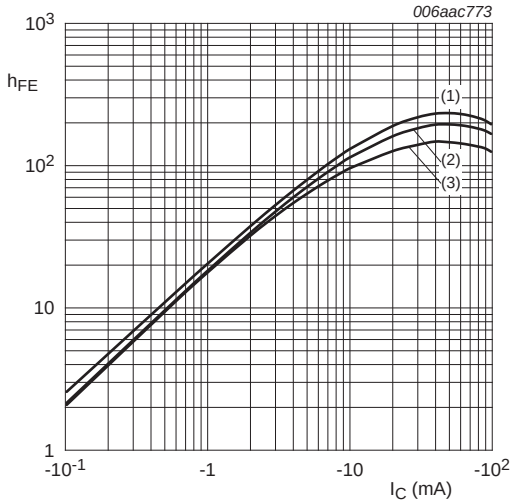
(3) $T_{amb}$ = 100 °C

**Fig 9. PDTA143EQA: Off-state input voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 10. PDTA143EQA: Collector capacitance as a function of collector-base voltage; typical values**



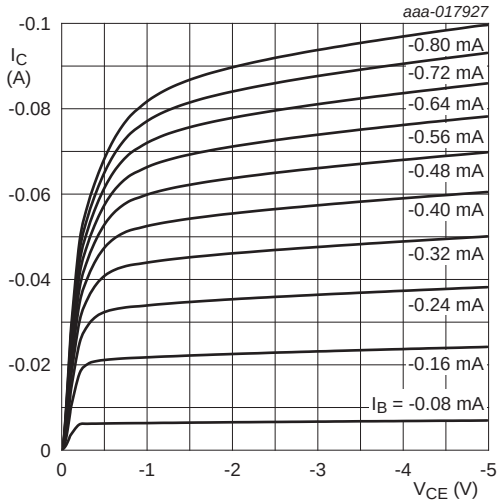

$V_{CE}$ = −5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

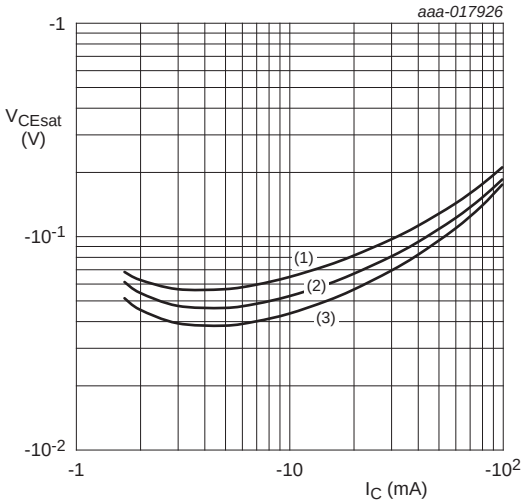
(3) $T_{amb}$ = −40 °C

**Fig 11. PDTA114EQA: DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 12. PDTA114EQA: Collector current as a function of collector-emitter voltage; typical values**



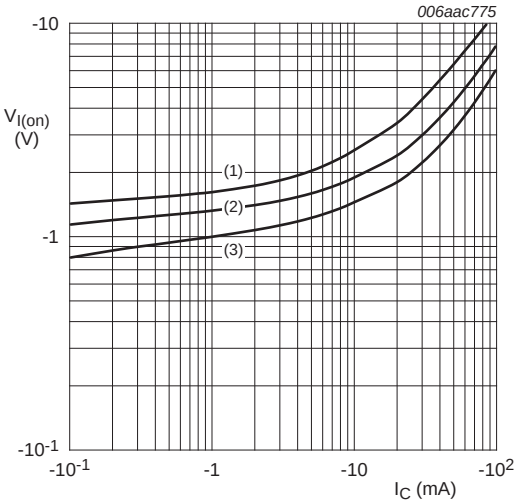

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 13. PDTA114EQA: Collector-emitter saturation voltage as a function of collector current; typical values**



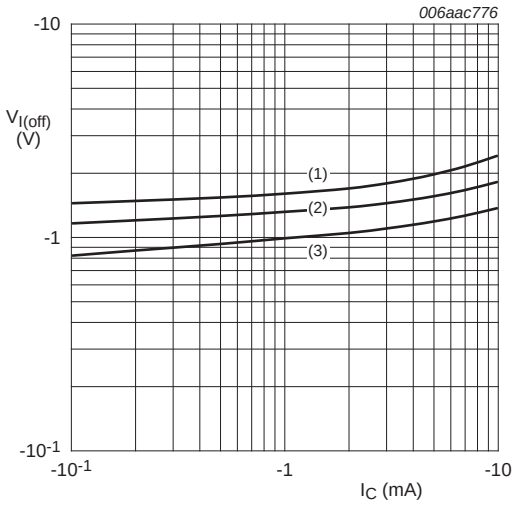

$V_{CE}$ = −0.3V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 14. PDTA114EQA: On-state input voltage as a function of collector current; typical values**



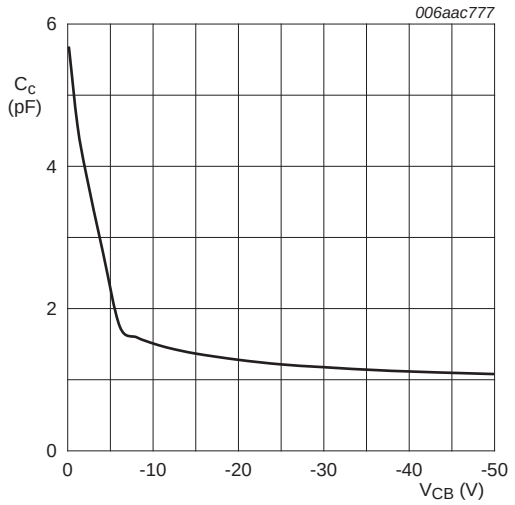

$V_{CE}$ = −5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

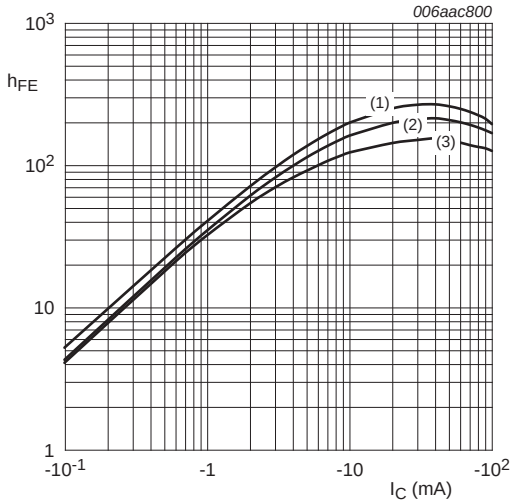
(3) $T_{amb}$ = 100 °C

**Fig 15. PDTA114EQA: Off-state input voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 16. PDTA114EQA: Collector capacitance as a function of collector-base voltage; typical values**



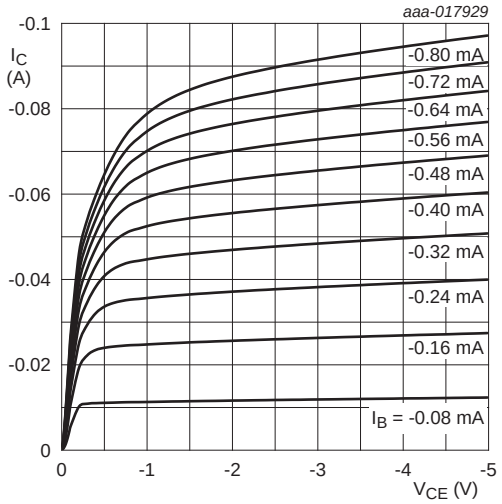

$V_{CE}$ = −5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

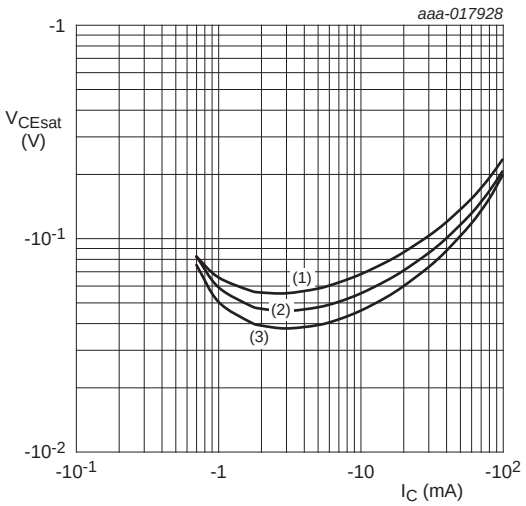
(3) $T_{amb}$ = −40 °C

**Fig 17. PDTA124EQA: DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 18. PDTA124EQA: Collector current as a function of collector-emitter voltage; typical values**



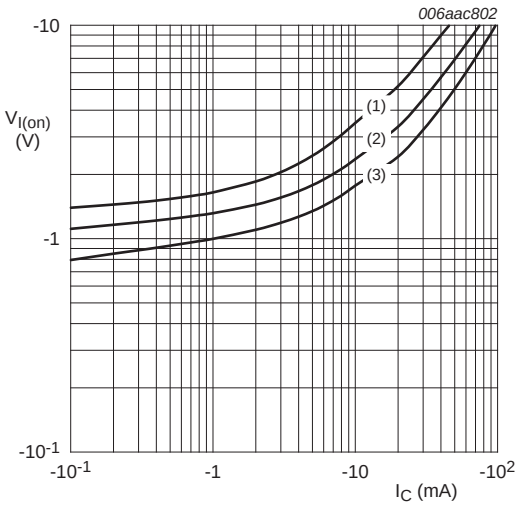

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 19. PDTA124EQA: Collector-emitter saturation voltage as a function of collector current; typical values**



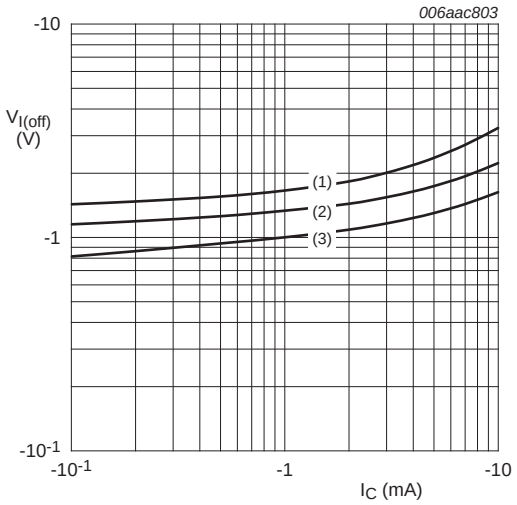

$V_{CE}$ = −0.3 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 20. PDTA124EQA: On-state input voltage as a function of collector current; typical values**



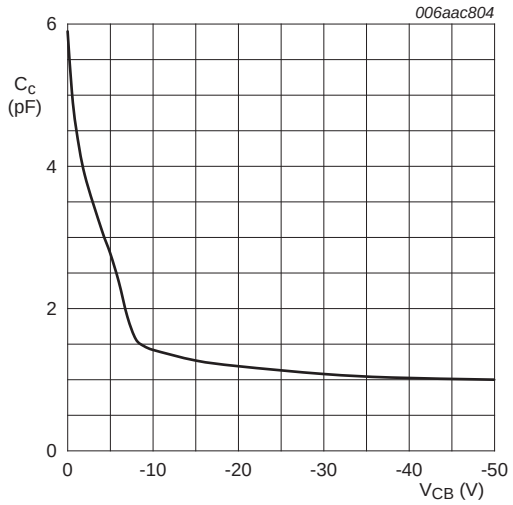

$V_{CE}$ = −5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

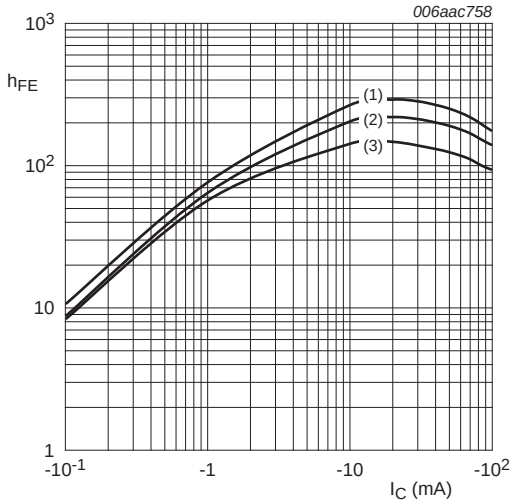
(3) $T_{amb}$ = 100 °C

**Fig 21. PDTA124EQA: Off-state input voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 22. PDTA124EQA: Collector capacitance as a function of collector-base voltage; typical values**



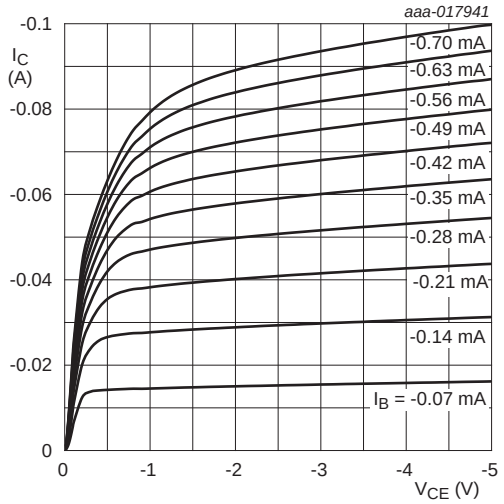

$V_{CE}$ = −5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

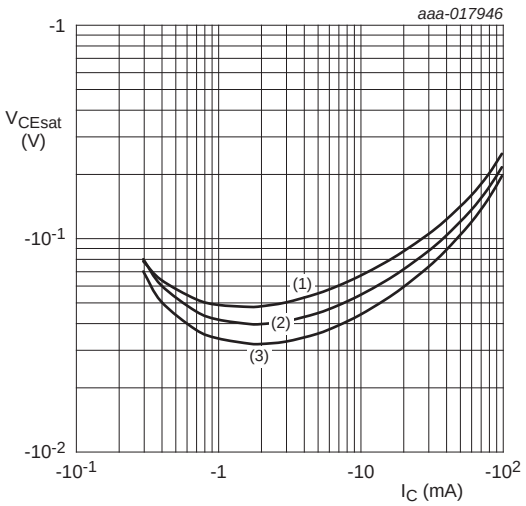
(3) $T_{amb}$ = −40 °C

**Fig 23. PDTA144EQA: DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 24. PDTA144EQA: Collector current as a function of collector-emitter voltage; typical values**



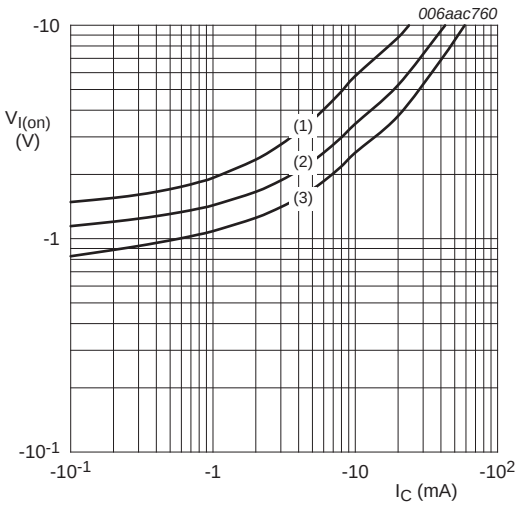

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 25. PDTA144EQA: Collector-emitter saturation voltage as a function of collector current; typical values**



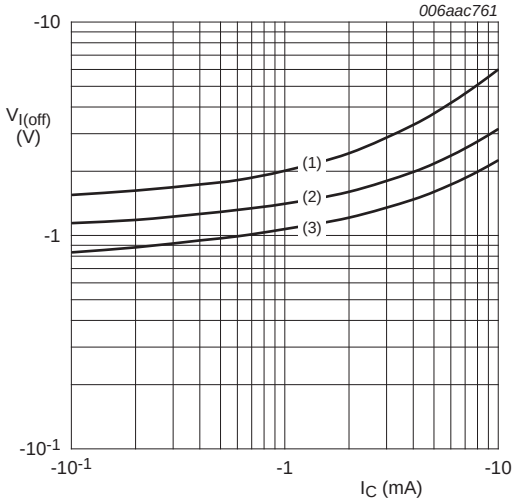

$V_{CE}$ = −0.3 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 26. PDTA144EQA: On-state input voltage as a function of collector current; typical values**



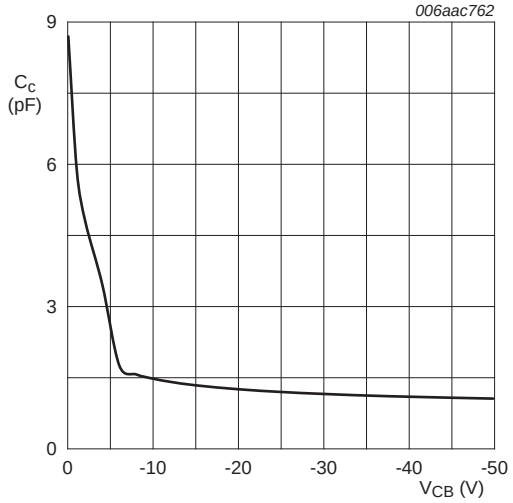

$V_{CE}$ = −5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

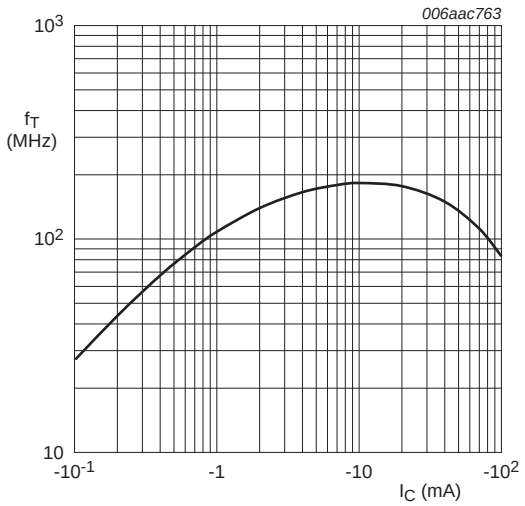
(3) $T_{amb}$ = 100 °C

**Fig 27. PDTA144EQA: Off-state input voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 28. PDTA144EQA: Collector capacitance as a function of collector-base voltage; typical values**




$V_{CE}$ = −5 V; f = 100 MHz; $T_{amb}$ = 25 °C

**Fig 29. Transition frequency as a function of collector current; typical values of built-in transistor**

# 8. Test information

## 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 8.2 Resistor calculation

- Calculation of bias resistor 1 (R1):

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation of bias resistor ratio (R2/R1):

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

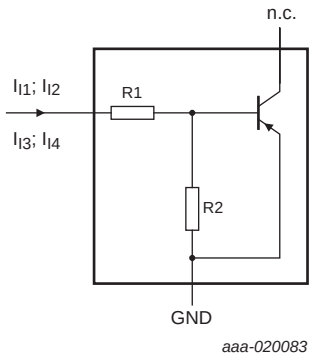



**Fig 30. Resistor test circuit**

## 8.3 Resistor test conditions

**Table 9. Resistor test conditions**

| Type number | R1 | R2 | Test conditions | | | |
|---|---|---|---|---|---|---|
| | (kΩ) | (kΩ) | $I_{I1}$ | $I_{I2}$ | $I_{I3}$ | $I_{I4}$ |
| PDTA143EQA | 4.7 | 4.7 | −600 µA | −700 µA | 600 µA | 700 µA |
| PDTA114EQA | 10 | 10 | −350 µA | −450 µA | 350 µA | 450 µA |
| PDTA124EQA | 22 | 22 | −150 µA | −230 µA | 150 µA | 230 µA |
| PDTA144EQA | 47 | 47 | −55 µA | −105 µA | 55 µA | 105 µA |

## 9. Package outline

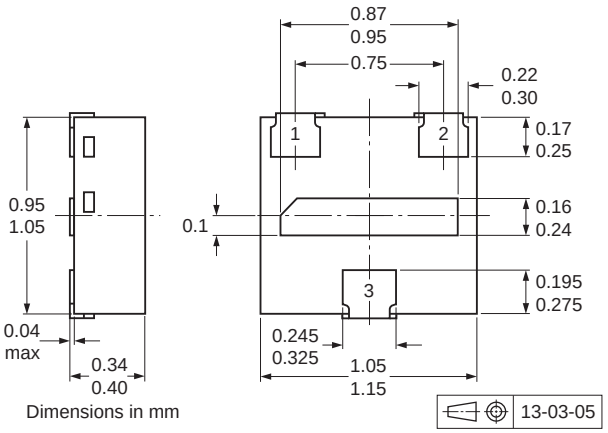



**Fig 31. Package outline DFN1010D-3 (SOT1215)**

## 10. Soldering

**Footprint information for reflow soldering of DFN1010D-3 package** **SOT1215**

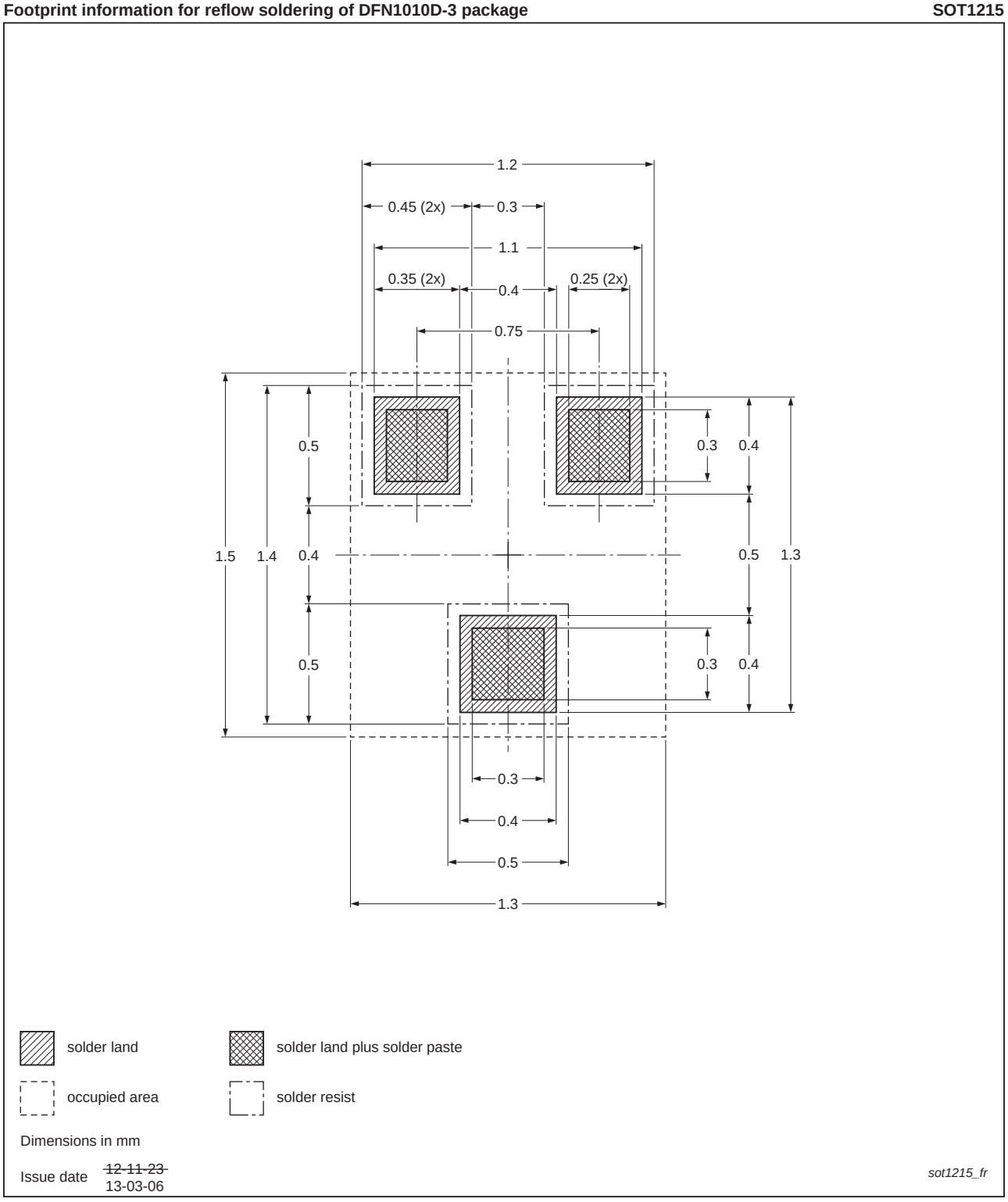



**Fig 32. Reflow soldering footprint DFN1010D-3 (SOT1215)**

## 11. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PDTA143/114/124/144EQA_SER v.1 | 20151218 | Product data sheet | - | - |

# 12. Legal information

## 12.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 14. Contents





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**Date of release: 18 December 2015**

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