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Kind regards,

Team Nexperia



PDTA144WMB

PNP resistor-equipped transistor; R1 = 47 k Ω , R2 = 22 k Ω

Rev. 1 — 2 July 2012

Product data sheet

1. Product profile

1.1 General description

PNP Resistor-Equipped Transistor (RET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package.

NPN complement: PDTC144WMB.

1.2 Features and benefits

- 100 mA output current capability
- Reduces component count
- Built-in bias resistors
- Reduces pick and place costs
- Simplifies circuit design
- AEC-Q101 qualified
- Leadless ultra small SMD plastic package
- Low package height of 0.37 mm

1.3 Applications

- Low-current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications
- Mobile applications

1.4 Quick reference data

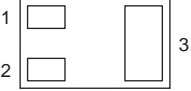
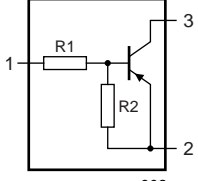
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _O	output current		-	-	-100	mA
R1	bias resistor 1 (input)	T _{amb} = 25 °C	33	47	61	k Ω
R2/R1	bias resistor ratio		0.37	0.47	0.57	



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 <p>Transparent top view</p>	 <p>sym003</p>
2	G	GND (emitter)		
3	O	output (collector)		

DFN1006B-3 (SOT883B)

3. Ordering information

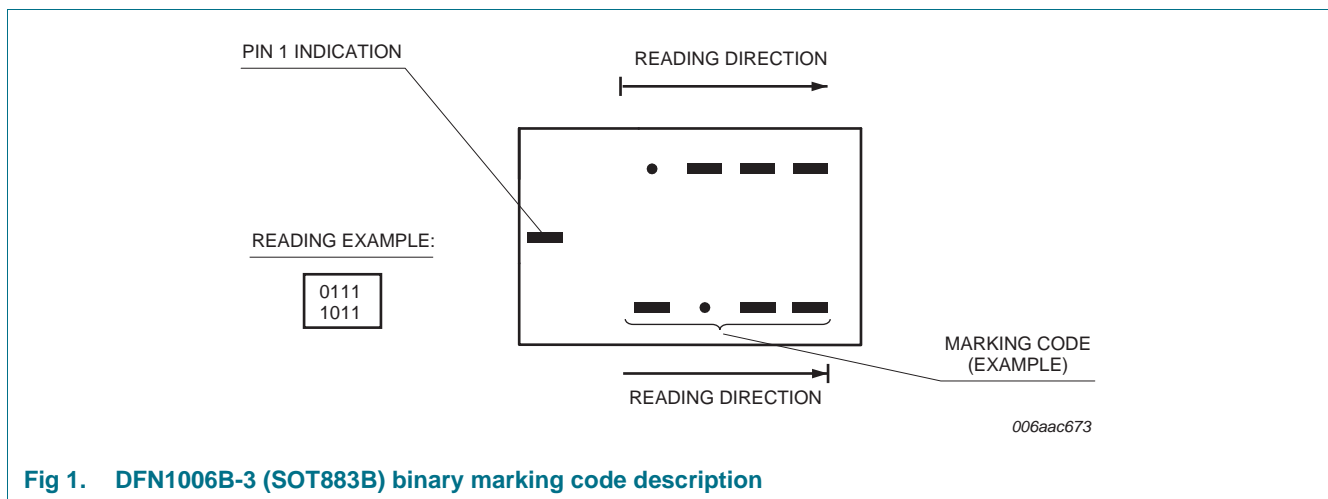
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTA144WMB	DFN1006B-3	Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm	SOT883B

4. Marking

Table 4. Marking codes

Type number	Marking code
PDTA144WMB	0010 1110



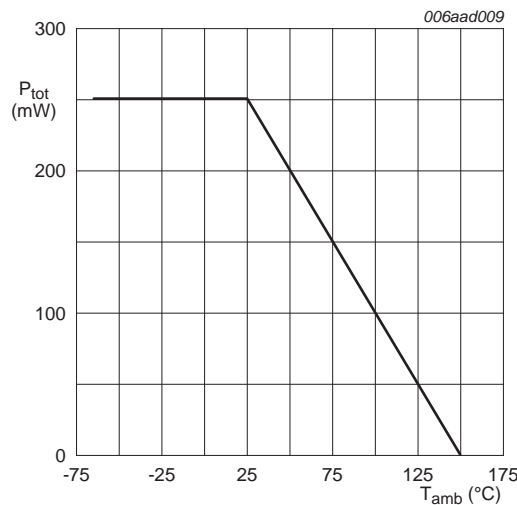
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter	-	-50	V
V _{CEO}	collector-emitter voltage	open base	-	-50	V
V _{EBO}	emitter-base voltage	open collector	-	-10	V
V _I	input voltage	positive	-	10	V
		negative	-	-40	V
I _O	output current		-	-100	mA
I _{CM}	peak collector current	pulsed; t _p ≤ 1 ms	-	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	250	mW
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	150	°C
T _{stg}	storage temperature		-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

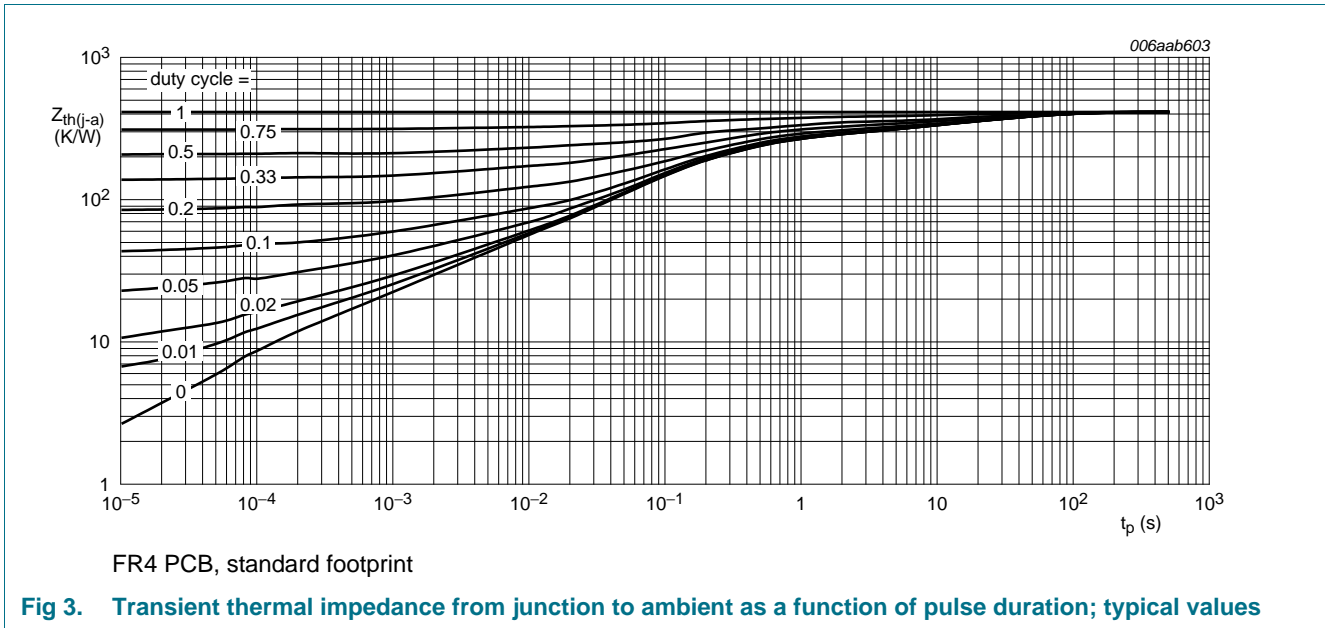
Fig. 2. Power derating curve for DFN1006B-3 (SOT883B)

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

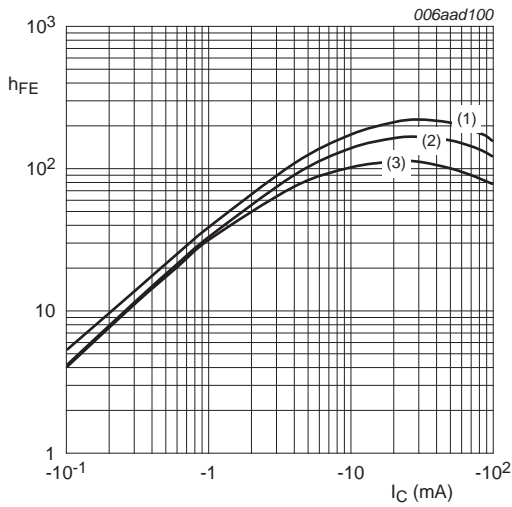


7. Characteristics

Table 7. Characteristics

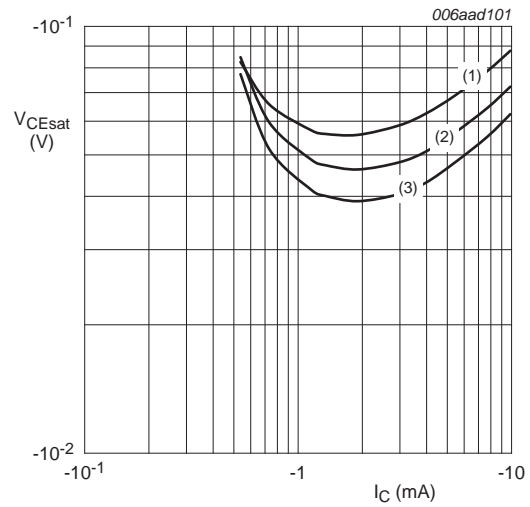
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CBO}	collector-base cut-off current	V _{CB} = -50 V; I _E = 0 A; T _{amb} = 25 °C	-	-	-100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = -30 V; I _B = 0 A; T _{amb} = 25 °C	-	-	-1	μA
		V _{CE} = -30 V; I _B = 0 A; T _j = 150 °C	-	-	-5	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	-110	μA
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -5 mA; T _{amb} = 25 °C	60	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -10 mA; I _B = -0.5 mA; T _{amb} = 25 °C	-	-	-150	mV
V _{I(off)}	off-state input voltage	V _{CE} = -5 V; I _C = -100 μA; T _{amb} = 25 °C	-	-1.7	-1.2	V
V _{I(on)}	on-state input voltage	V _{CE} = -0.3 V; I _C = -2 mA; T _{amb} = 25 °C	-4	-2.7	-	V
R1	bias resistor 1 (input)	T _{amb} = 25 °C	33	47	61	kΩ
R2/R1	bias resistor ratio		0.37	0.47	0.57	
C _C	collector capacitance	V _{CB} = -10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C	-	-	3	pF
f _T	transition frequency	V _{CE} = -5 V; I _C = -10 mA; f = 100 MHz; T _{amb} = 25 °C	[1]	180	-	MHz

[1] Characteristics of built-in transistor.



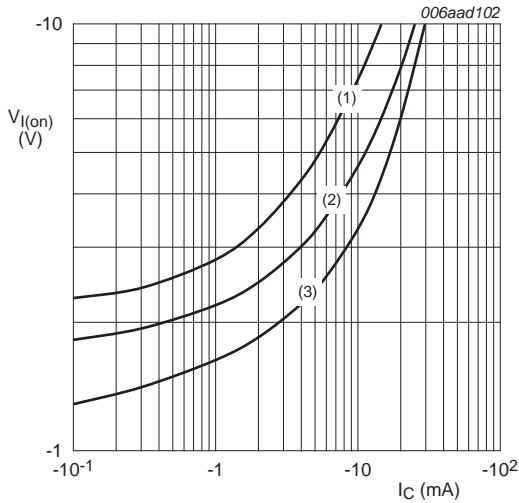
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 4. DC current gain as a function of collector current; typical values



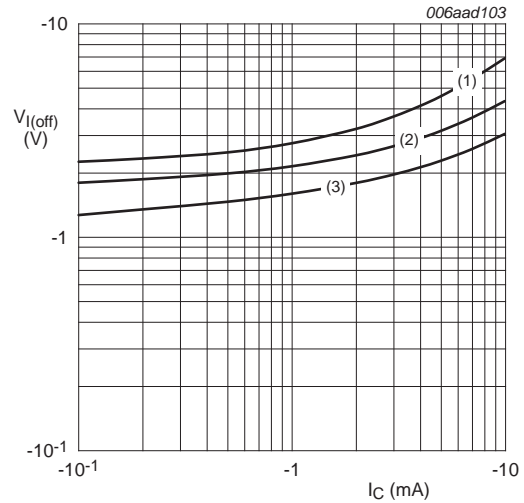
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 5. Collector-emitter saturation voltage as a function of collector current; typical values



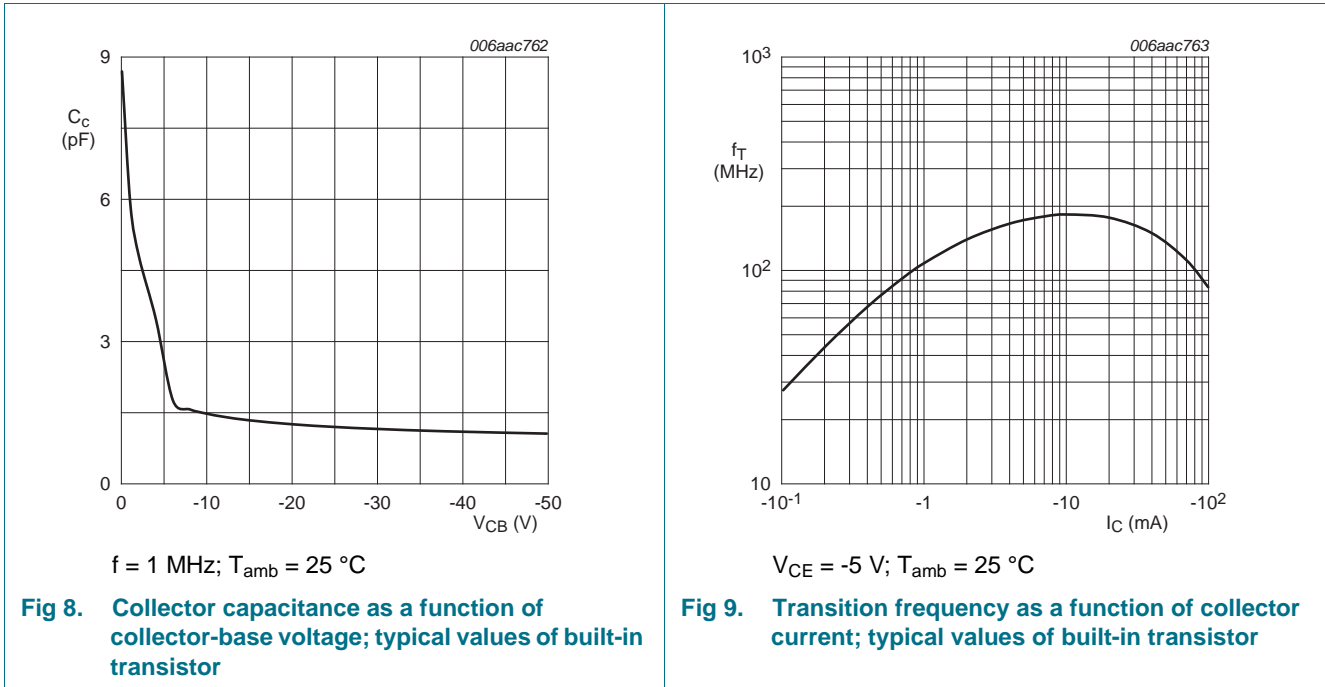
$V_{CE} = -0.3\text{ V}$
 (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 6. On-state input voltage as a function of collector current; typical values



$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 7. Off-state input voltage as a function of collector current; typical values



8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline

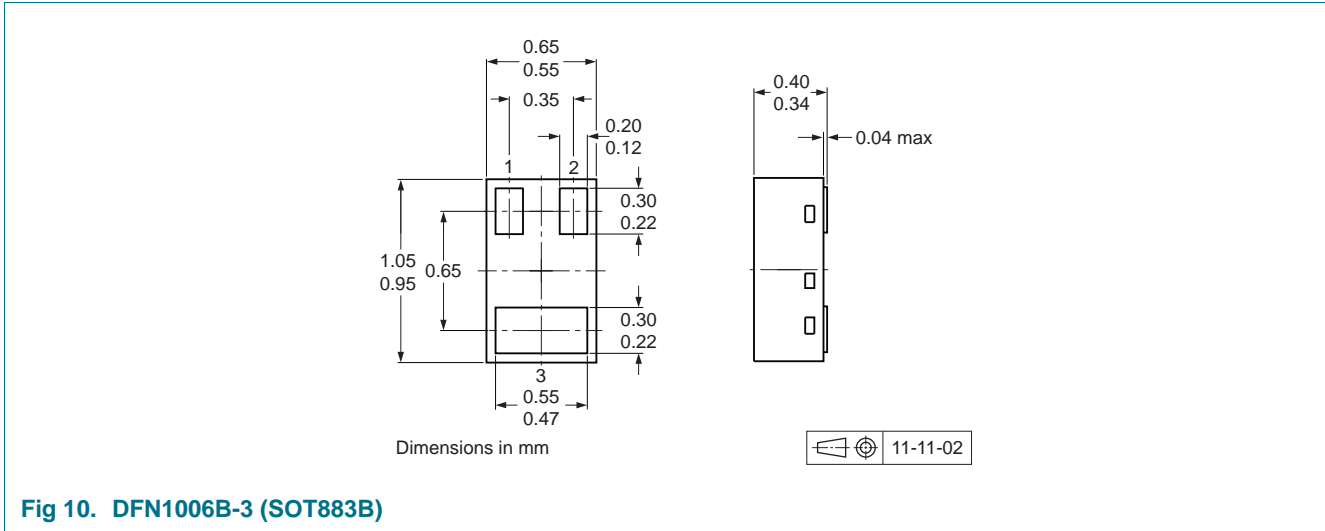


Fig 10. DFN1006B-3 (SOT883B)

10. Soldering

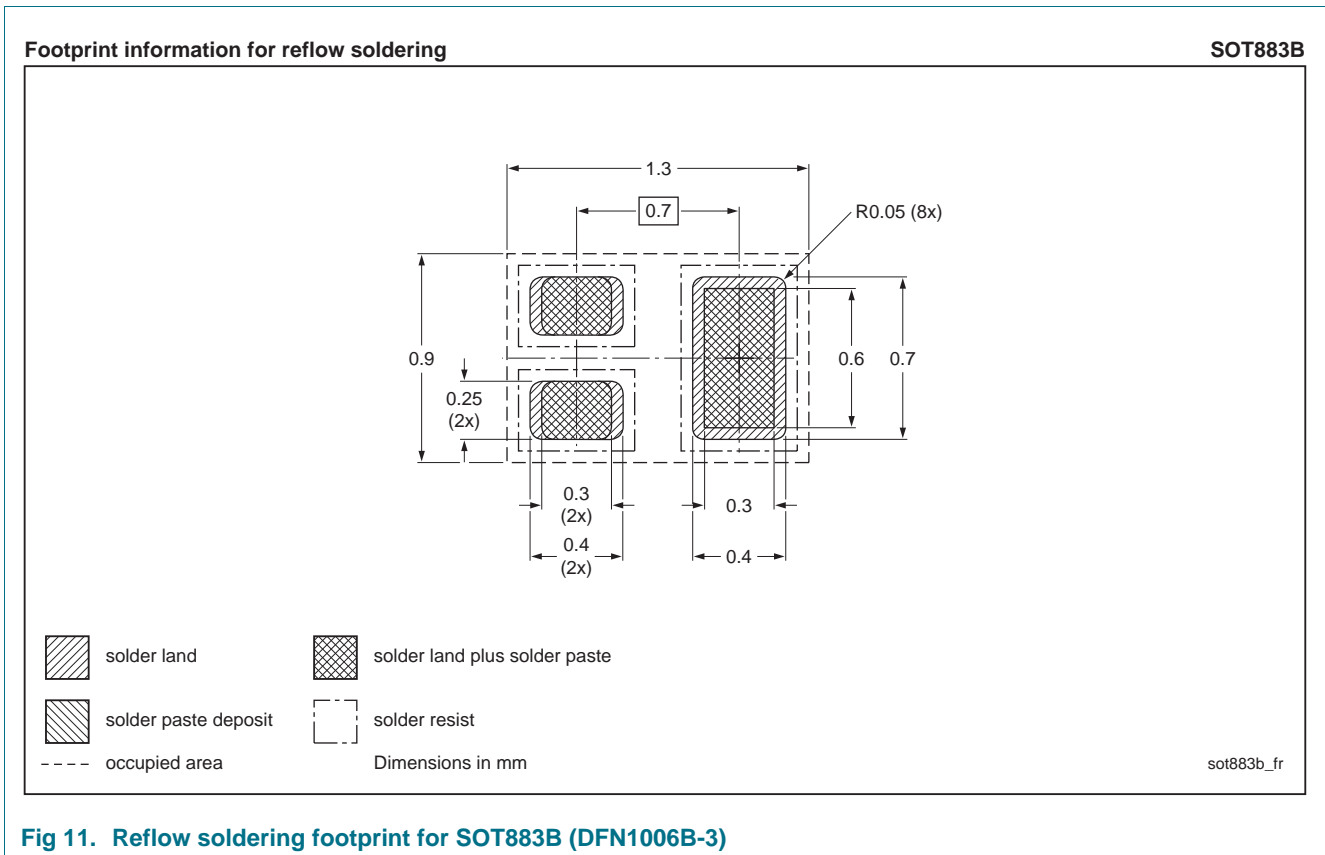


Fig 11. Reflow soldering footprint for SOT883B (DFN1006B-3)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA144WMB v.1	20120702	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^[1] [2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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