PESD24VF1BSF

Ultra low capacitance bidirectional ESD protection diode

11 December 2015 **Product data sheet**

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Ultra low diode capacitance C_d = 0.25 pF
- High reverse standoff voltage V_{RWM} = 24 V
- ESD protection up to ±10 kV according to IEC 61000-4-2

3. Applications

- NFC antenna protection
- Protection of high-speed and standard data lines with high signal levels

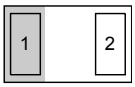
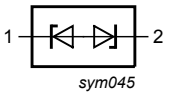
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_d	diode capacitance	f = 1 MHz; V_R = 0 V		-	0.25	0.4	pF
V_{RWM}	reverse standoff voltage			-	-	24	V

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DSN0603-2 (SOD962-2)**	
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD24VF1BSF	DSN0603-2	Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm	SOD962-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD24VF1BSF	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	peak pulse current	t_p = 8/20 µs	[1]	-	1	A
T_j	junction temperature			-45	125	°C
T_{amb}	ambient temperature			-45	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-	10	kV
		IEC 61000-4-2; air discharge	[2]	-	15	kV
		MIL-STD-883; human body model; HBM		-	10	kV

[1] According to IEC 61000-4-5 and IEC 61643-321.
[2] Device stressed with ten non-repetitive ESD pulses.

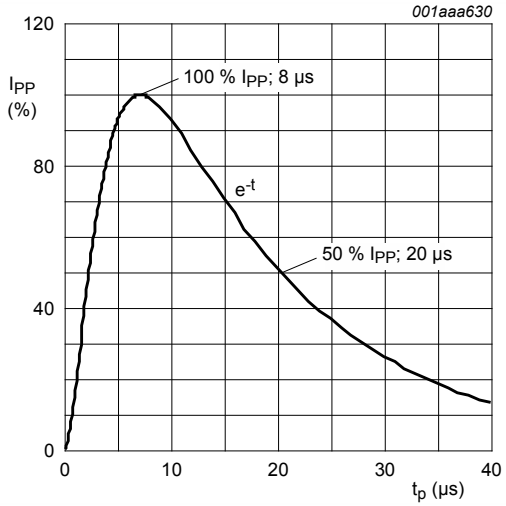


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

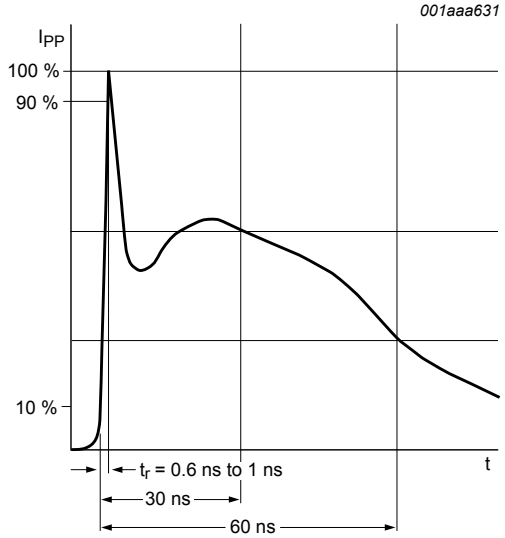


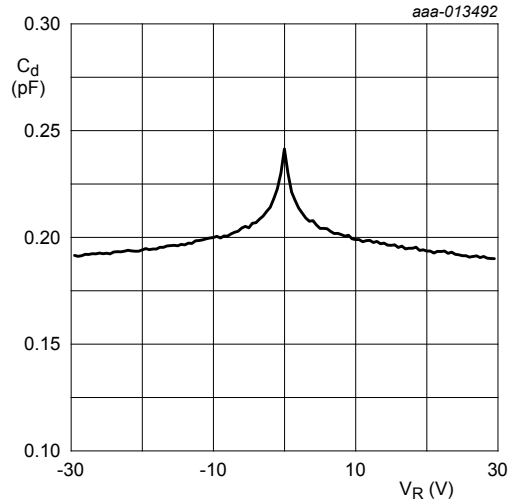
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage			-	-	24	V
I_{RM}	reverse leakage current	V_R = 24 V		-	1	30	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V		-	0.25	0.4	pF
V_{BR}	breakdown voltage	I_R = 1 mA		24.5	28	-	V
V_{CL}	clamping voltage	I_{PPM} = 1 A	[1]	-	-	17	V
R_{dyn}	dynamic resistance	I_R = 5 A	[2]	-	0.7	-	Ω

[1] According to IEC 61000-4-5 and IEC 61643-321.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.



f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C

Fig. 3. Diode capacitance as a function of reverse voltage; typical values

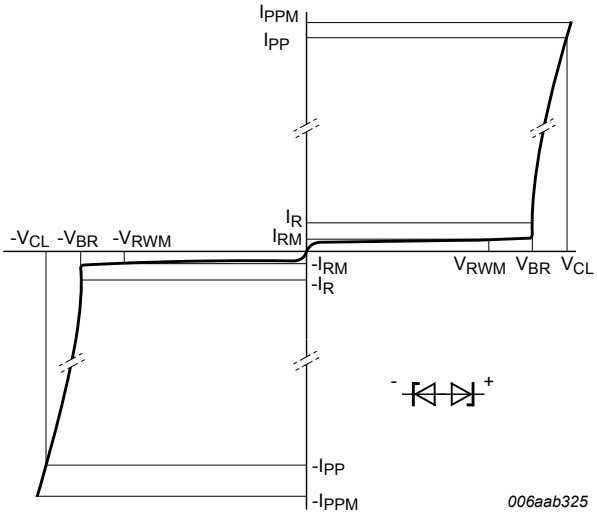
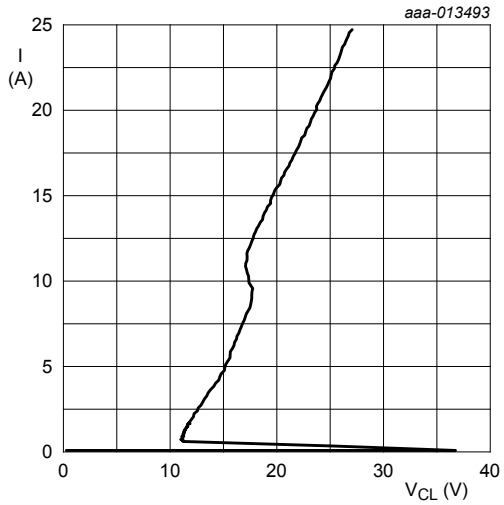


Fig. 4. V-I characteristics for a bidirectional ESD protection diode



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 5. Dynamic resistance

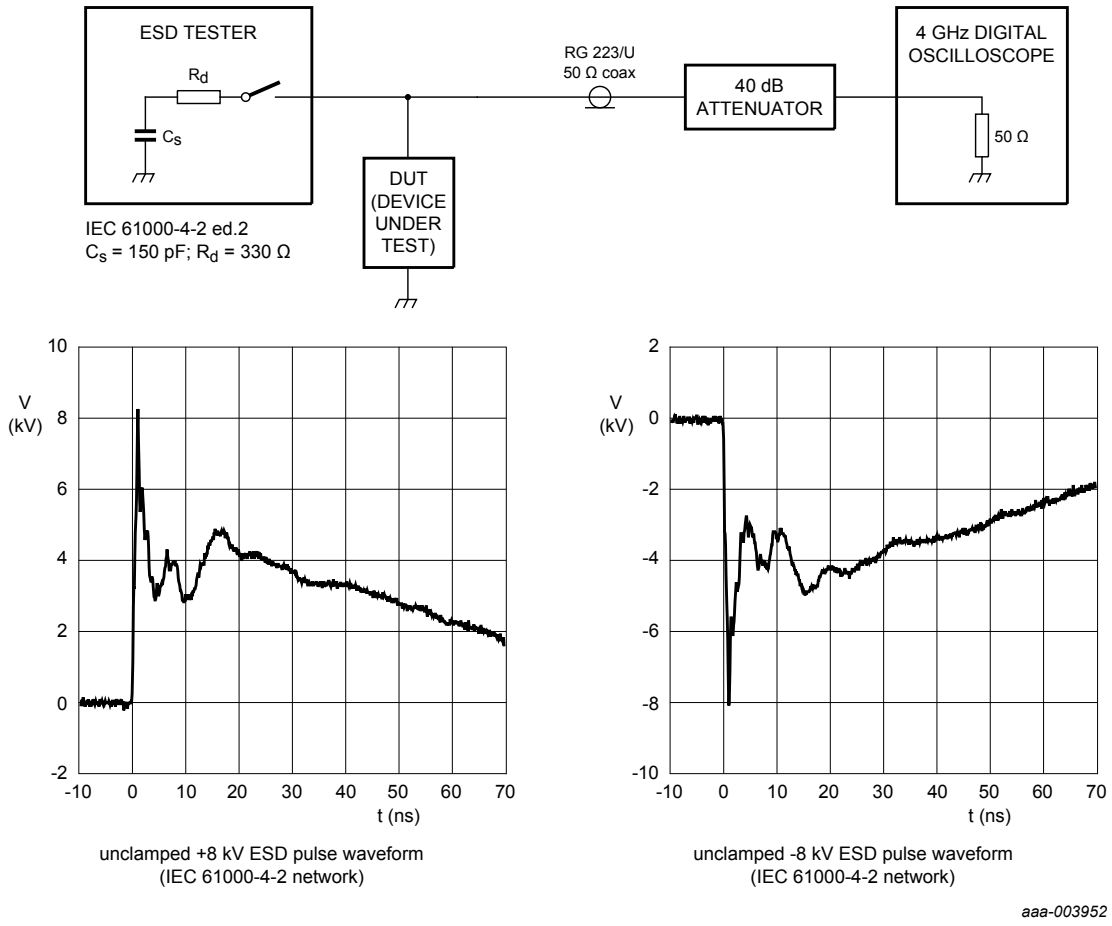


Fig. 6. ESD clamping test setup and waveforms

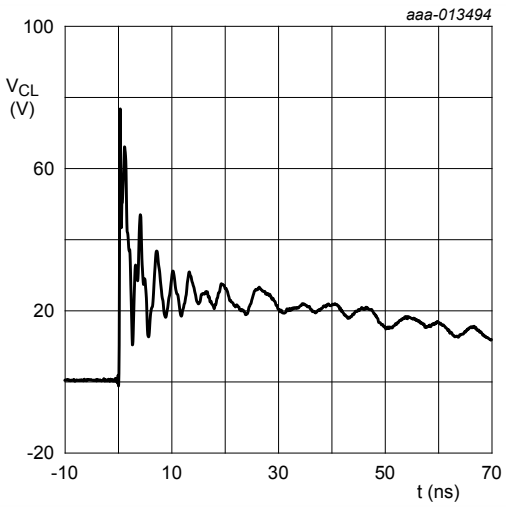


Fig. 7. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

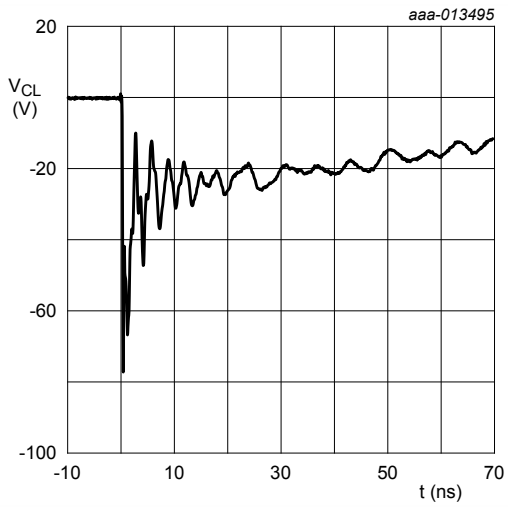


Fig. 8. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

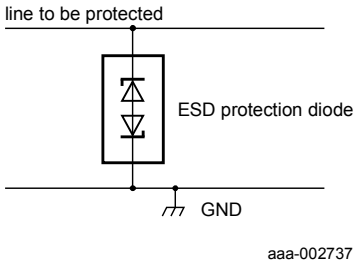


Fig. 9. Application diagram

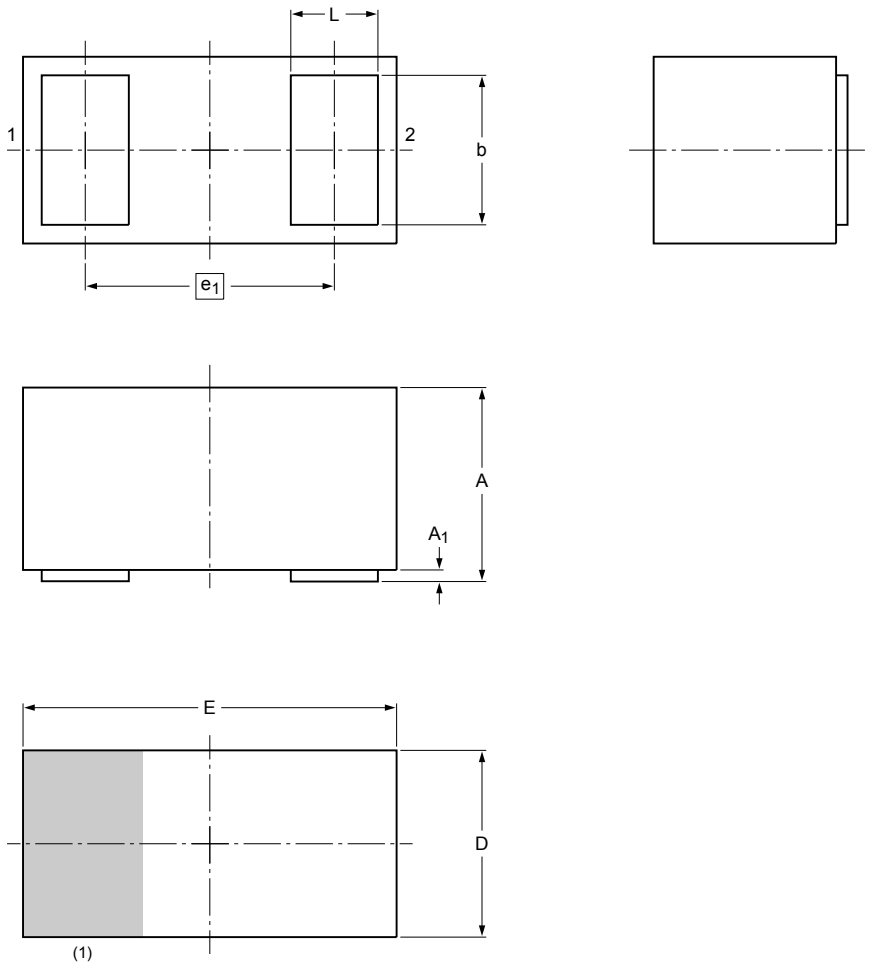
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm **SOD962-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e_1	L
mm	max	0.32	0.03	0.25	0.325	0.625		0.15
	nom						0.4	
	min	0.28		0.23	0.275	0.575		0.13

Note
1. The marking bar indicates the cathode.

sod962-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD962-2						~~13-07-12~~ 13-07-17

Fig. 10. Package outline DSN0603-2 (SOD962-2)

12. Soldering

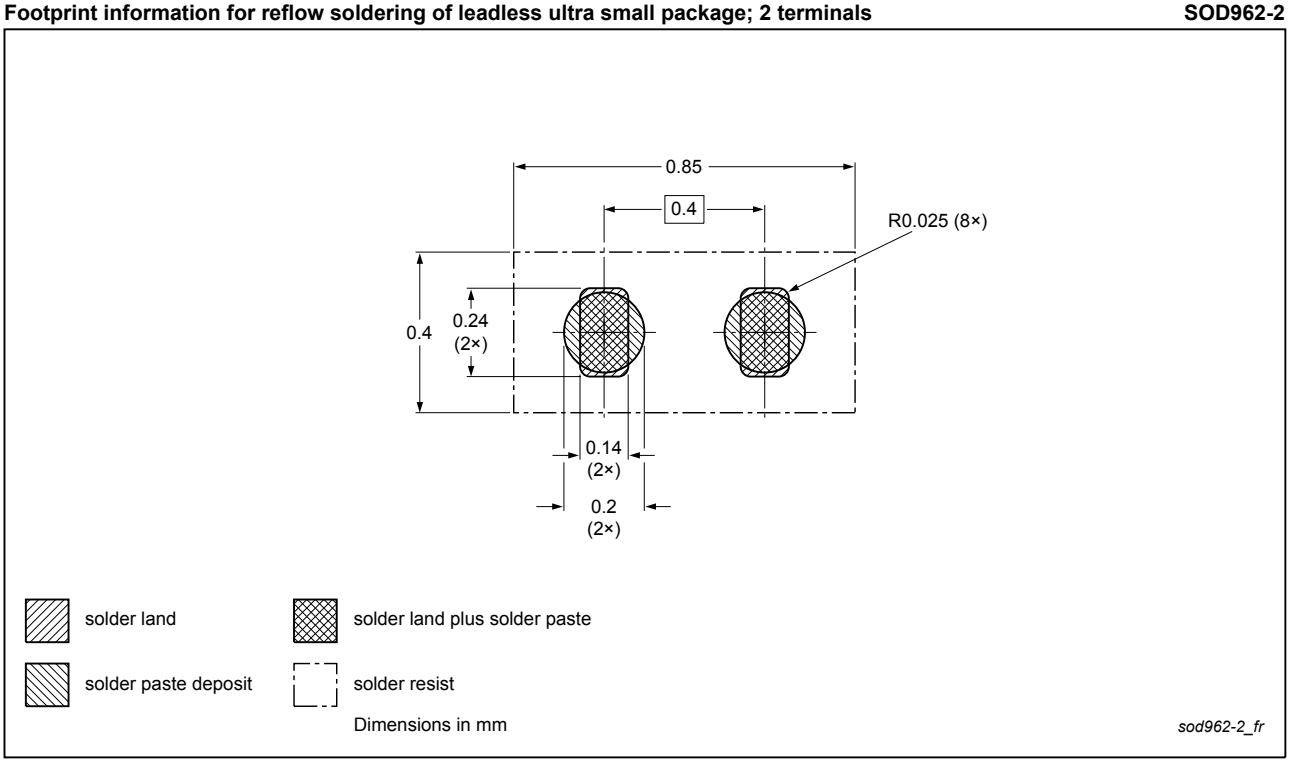


Fig. 11. Reflow soldering footprint for DSN0603-2 (SOD962-2)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD24VF1BSF v.1	20151211	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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