



PESD2ETH100-T

ESD protection for In-vehicle networks

13 December 2019

Product data sheet

1. General description

Fully OPEN Alliance 100BASE-T1 compliant Electrostatic discharge (ESD) protection device in a small SOT23 surface-mounted plastic package designed to protect two automotive in-vehicle network bus lines from the damage caused by ESD and other transients.

2. Features and benefits

- Fully OPEN Alliance 100BASE-T1 compliant
- High trigger voltage: $V_{t1} = 100$ V min.
- Low capacitance: $C_d < 3$ pF
- ESD protection up to 30 kV (IEC 61000-4-2)
- 1000 contact discharges (OPEN Alliance specification) with 30 kV (IEC 61000-4-2)
- AEC-Q101 qualified / automotive grade

3. Applications

ESD protection for in-vehicle network lines In-automotive environments

- OPEN Alliance 100BASE-T1 Ethernet
- Low-Voltage Differential Signaling (LVDS) automotive

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{RWM}	reverse standoff voltage	$T_{amb} = 25$ °C	-	-	24	V	
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	-	2.5	3	pF	
V_{t1}	trigger voltage	$T_{amb} = 25$ °C	[1]	100	140	V	
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	30	-	-	kV
		1000 contact discharges (IEC 61000-4-2); OPEN Alliance specification	[3]	30	-	-	kV

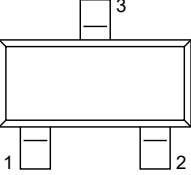
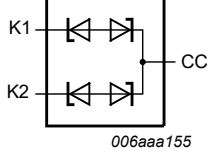
[1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

[2] Device stressed with ten non-repetitive ESD pulses.

[3] Measured from pin 1 or 2 to pin 3.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p style="text-align: center;">SOT23</p>	 <p style="text-align: center;">006aaa155</p>
2	K	cathode		
3	CC	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2ETH100-T	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PESD2ETH100-T	%HG

[1] % = placeholder for manufacturing site code

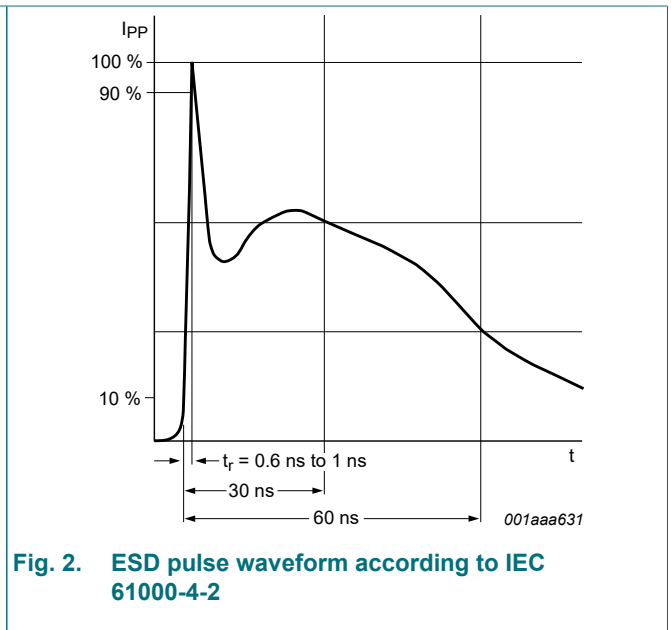
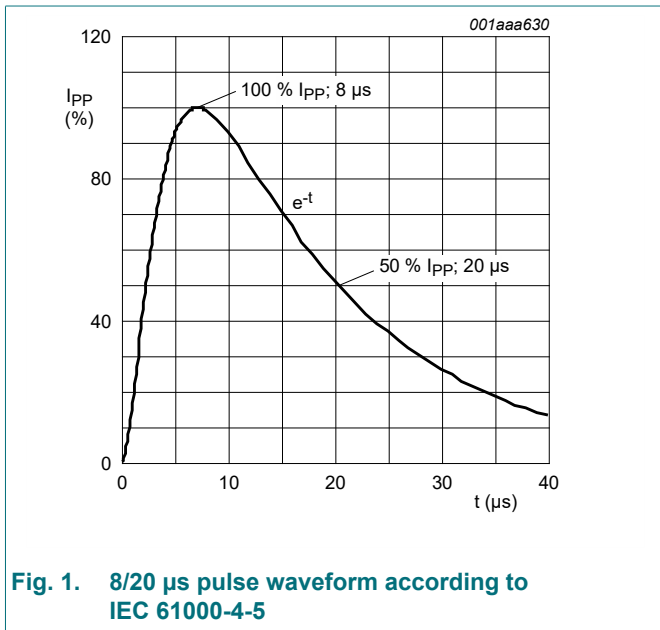
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC60134)

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1] [2]	-	3.2	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[3] [2]	30	-	kV
		ISO 10605; contact discharge; C = 150 pF; R = 330 Ω	[3] [2]	30	-	kV
		ISO 10605; contact discharge; C = 330 pF; R = 330 Ω	[3] [2]	30	-	kV
		1000 contact discharges (IEC 61000-4-2); OPEN Alliance specification	[2]	30	-	kV

- [1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.
- [2] Measured from pin 1 or 2 to pin 3.
- [3] Device stressed with ten non-repetitive ESD pulses.



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	24	V
V_h	holding voltage		[1]	28	-	V
V_{t1}	trigger voltage		[1]	100	140	V
I_{RM}	reverse leakage current	$V_{RWM} = 24\text{ V}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	1	100	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	2.5	3	pF
$\Delta C_d/C_d$	diode capacitance matching		[2]	0.5	-	%
		$f = 1\text{ MHz}; V_R = 2.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	0.5	-	%
R_{dyn}	dynamic resistance	$I_R = 70\text{ A}; t_r = 1\text{ ns}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	0.44	-	Ω

- [1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008
- [2] ΔC_d is the difference of the capacitance measured between pin 1 and pin 3 and the capacitance measured between pin 2 and pin 3.

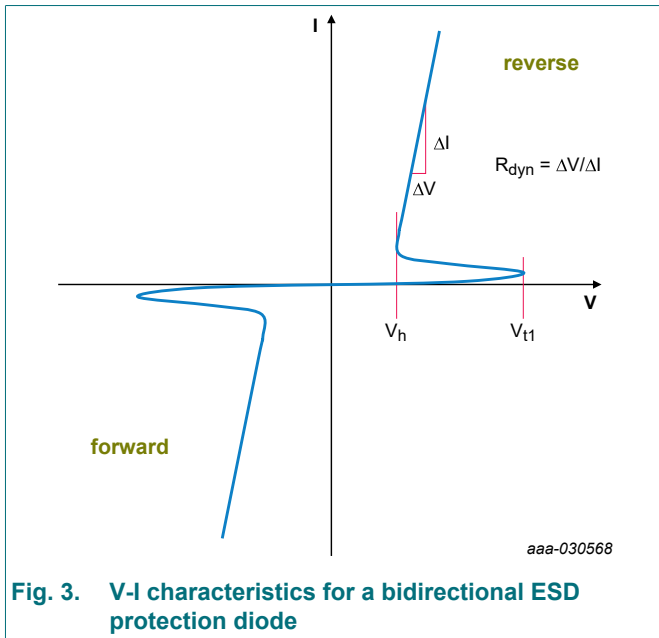


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

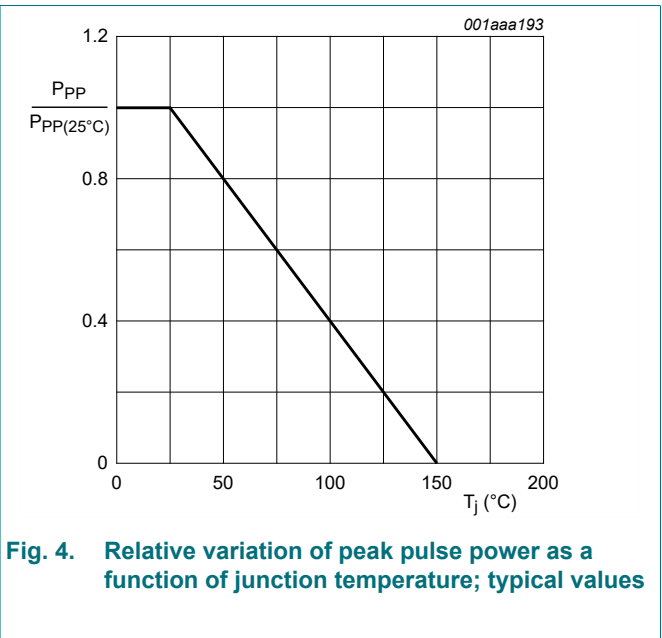
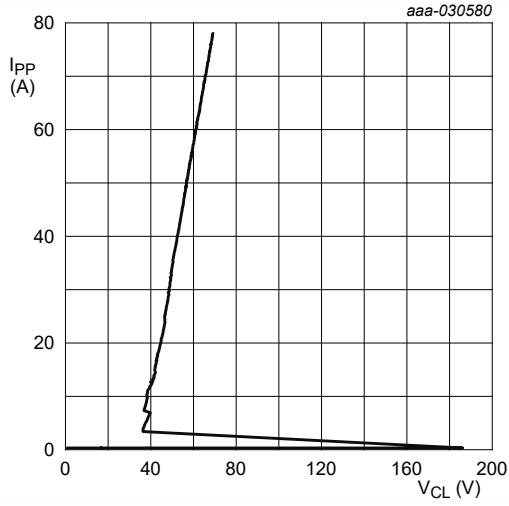
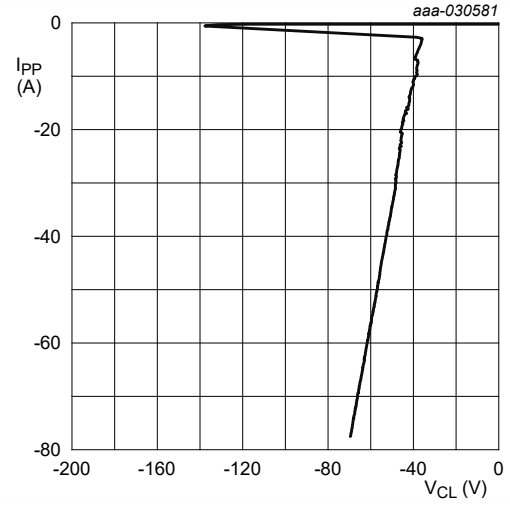


Fig. 4. Relative variation of peak pulse power as a function of junction temperature; typical values



$t_r = 1 \text{ ns}$
 $t_p = 100 \text{ ns}$; Transmission Line Pulse (TLP)

Fig. 5. Dynamic resistance with positive clamping; typical values



$t_r = 1 \text{ ns}$
 $t_p = 100 \text{ ns}$; Transmission Line Pulse (TLP)

Fig. 6. Dynamic resistance with negative clamping; typical values

10. Application information

In the „IEEE 100BASE-T1 EMC Test Specification for ESD suppression devices“¹ document (further referred as OPEN Alliance 100BASE-T1 specification), the OPEN Alliance describes four different tests to ensure compliance of ESD suppressor devices and PHYs which are compliant according to the document “Transceiver EMC Test Specification”. The PESD2ETH100-T passes all tests as shown on figures 7 to 18. Furthermore, it complies with the requirements mentioned in Section 2.2. of „IEEE 100BASE-T1 EMC Test Specification for ESD suppression devices“.

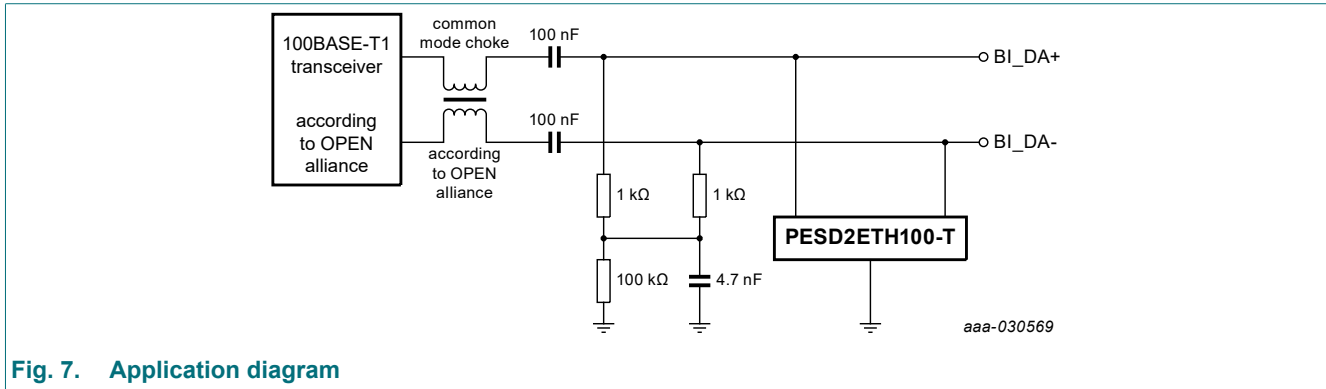


Fig. 7. Application diagram

The return loss and insertion loss are evaluated using the differential S-parameters S_{dd11} and S_{dd21}. These measurements replace the requirement for a certain capacitance value. To ensure symmetry, the differential to common mode rejection is evaluated using the S-parameter S_{sd21}. This measurement replaces the requirement for a matching of the capacitance per line. To ensure that the device does not degrade and changes behavior after repetitive ESD events, the S-parameter measurements are repeated after discharging 20 times ±8 kV ESD on signal lines 1 and 2, with C = 150 pF, R = 330 Ω according to ISO 10605. Subsequently, the S-parameters are measured again and compared to the original data. The S-parameter measurements for return and insertion loss as well as the measurements for ESD damage are conducted on different Printed-Circuit Boards (PCB).

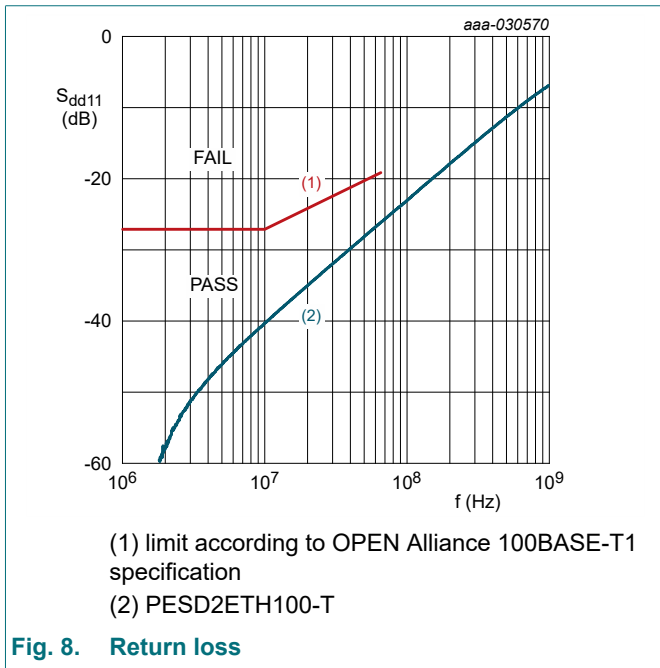


Fig. 8. Return loss

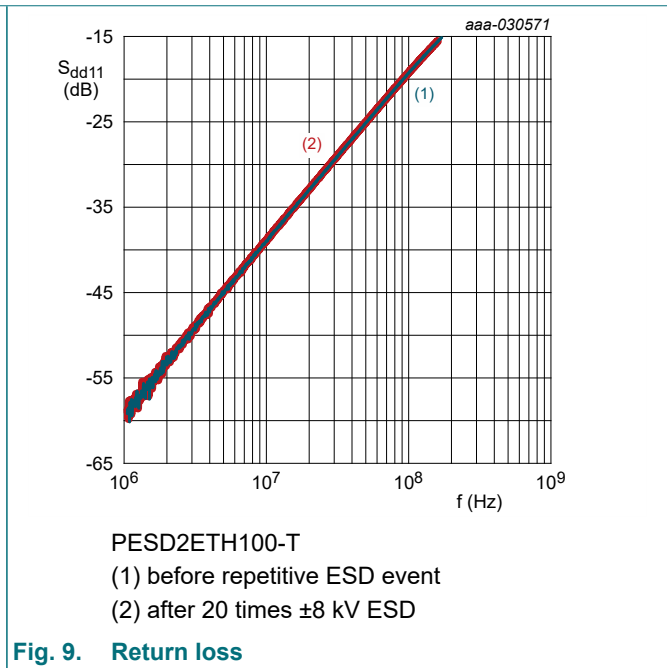
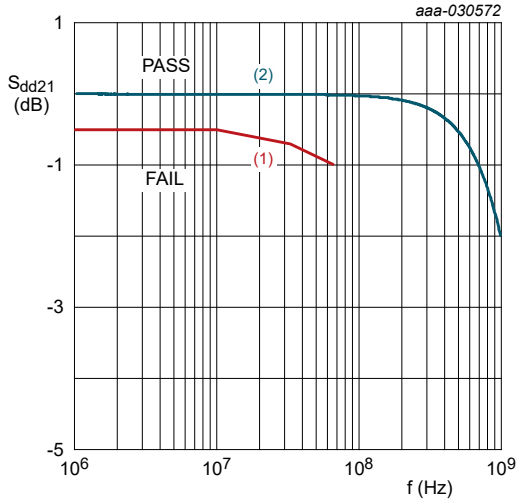


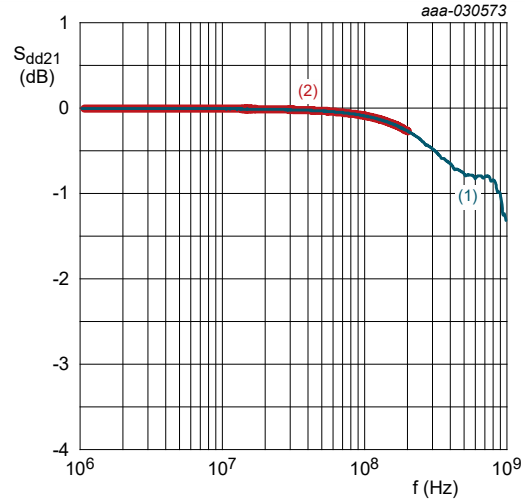
Fig. 9. Return loss

¹ OPEN Alliance: “IEEE 100BASE-T1 EMC Test Specification for ESD suppression devices”, version 1.0 rev.draft, December 10, 2018



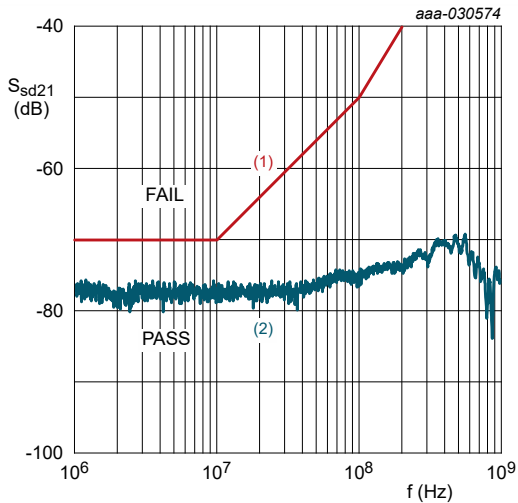
(1) limit according to OPEN Alliance 100BASE-T1 specification
(2) PESD2ETH100-T

Fig. 10. Insertion loss



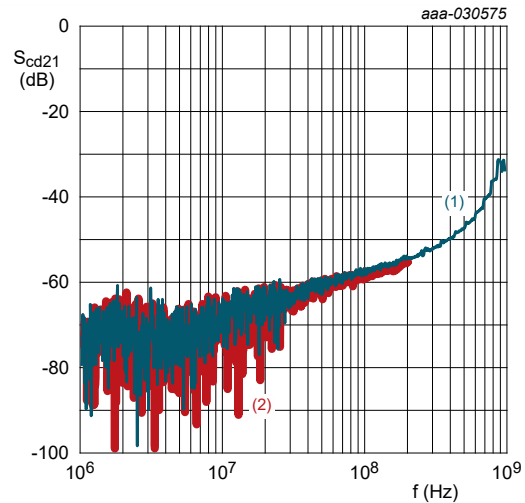
PESD2ETH100-T
(1) before repetitive ESD event
(2) after 20 times ±8 kV ESD

Fig. 11. Insertion loss



(1) limit according to OPEN Alliance 100BASE-T1 specification
(2) PESD2ETH100-T

Fig. 12. Differential to common mode rejection



PESD2ETH100-T
(1) before repetitive ESD event
(2) after 20 times ±8 kV ESD

Fig. 13. Differential to common mode rejection

To predict if the ESD suppressor device would protect a PHY of a certain robustness class (Class I (JEDEC-HBM 4 kV) and Class II (JEDEC-HBM 2 kV)), the ESD discharge current is measured in a reference circuit according to OPEN Alliance 100BASE-T1 specification for ± 4 kV and ± 6 kV according to IEC 61000-4-2 with $C = 150$ pF and $R = 330 \Omega$. Unlike in the OPEN Alliance 100BASE-T1 specification of October 29 2017, the „Transceiver Simulation network“ is implemented with 2Ω and 50Ω resistors.

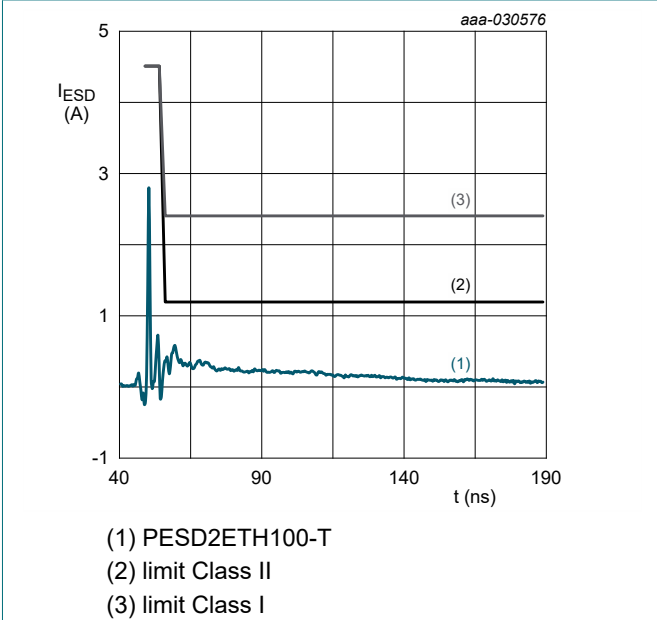


Fig. 14. ESD discharge current at +4 kV

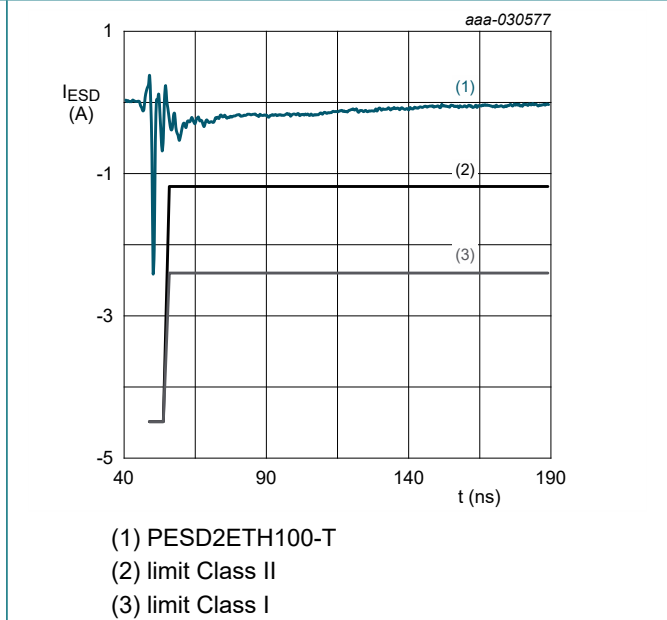


Fig. 15. ESD discharge current at -4 kV

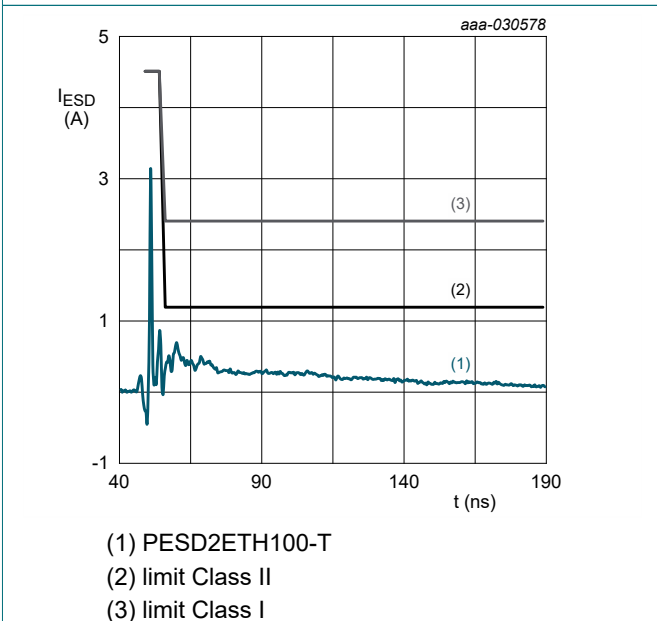


Fig. 16. ESD discharge current at +6 kV

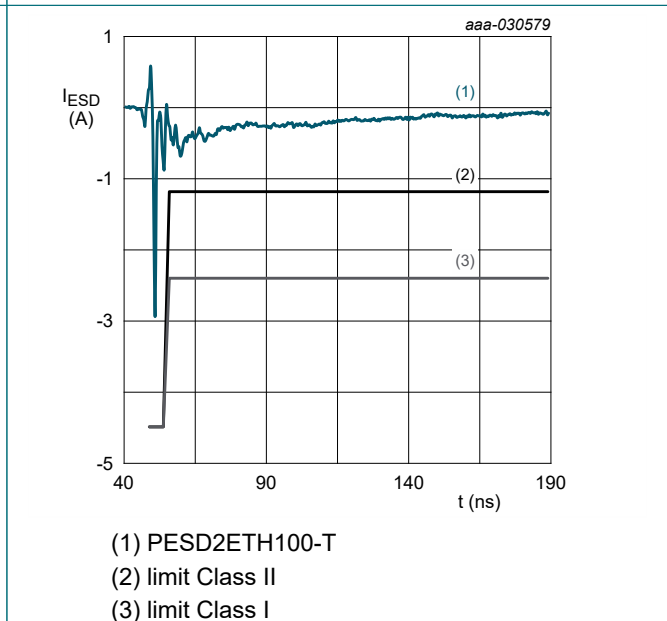
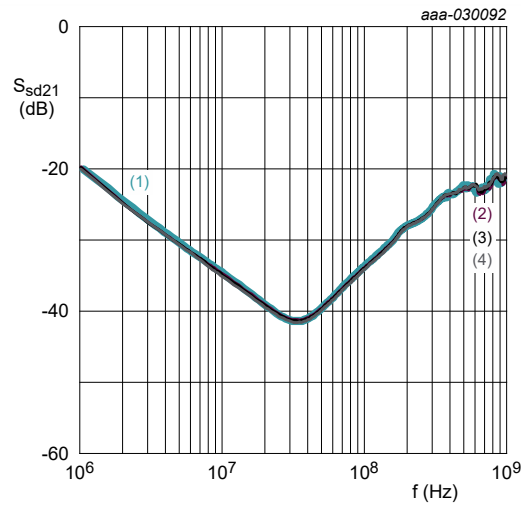


Fig. 17. ESD discharge current at -6 kV

To ensure that the ESD suppressor device is not impacting the EMC performance of the complete module, the RF Clamping Test as defined in the OPEN Alliance specification is applied. First a measurement at a reference power level of 25 dBm is conducted in an environment defined by the OPEN Alliance 100BASE-T1 specification. Next, the power is increased to 33 dBm (Class I), 36 dBm (Class II), and 39 dBm (Class III). No change in the measured common mode rejection indicates that the ESD suppressor device is not impacting the modules EMC performance.



According to OPEN Alliance 100BASE-T1 specification

Common mode rejection for:

- (1) reference
- (2) Class I
- (3) Class II
- (4) Class III

Fig. 18. RF Clamping Test

11. Package outline

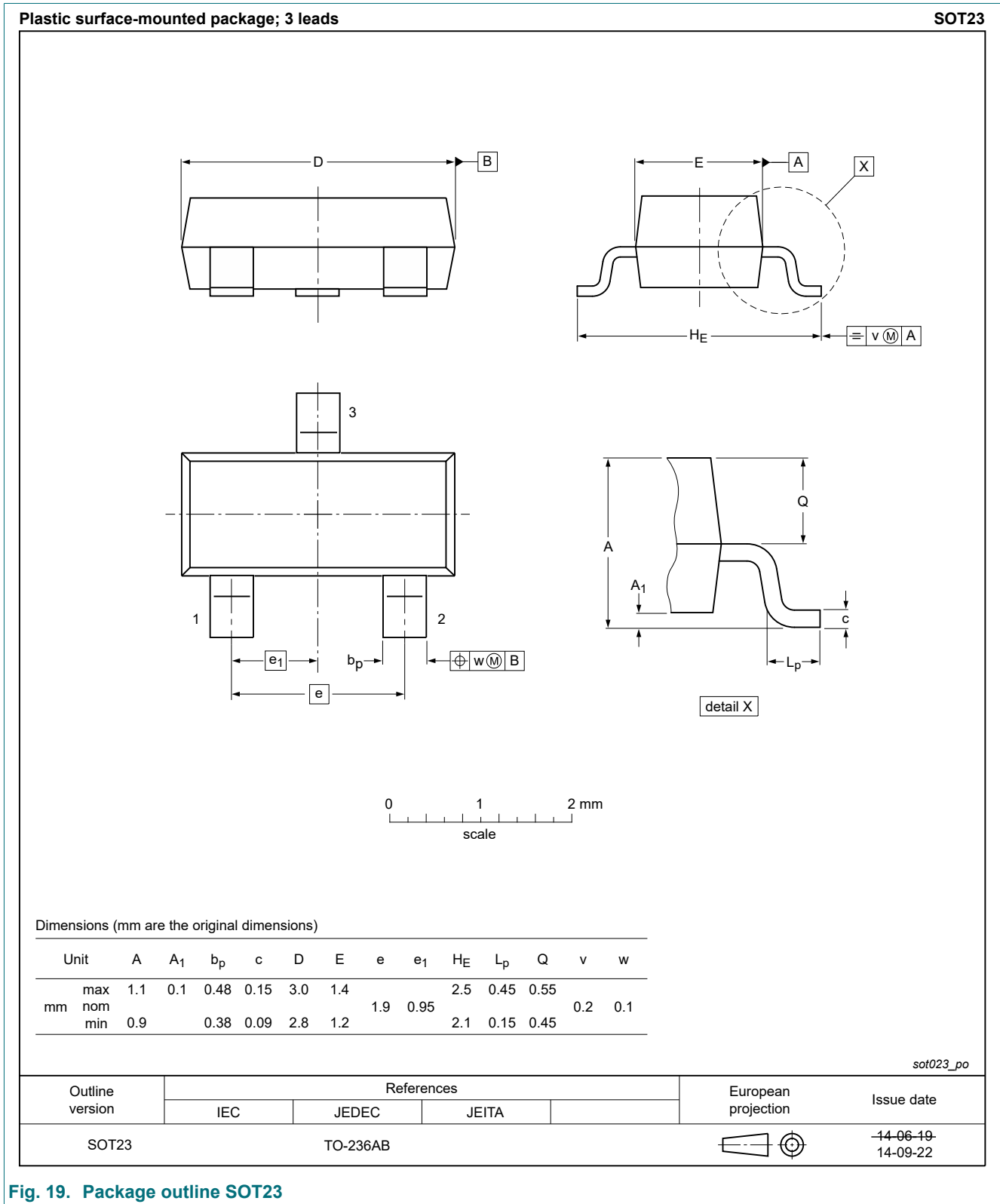


Fig. 19. Package outline SOT23

12. Soldering

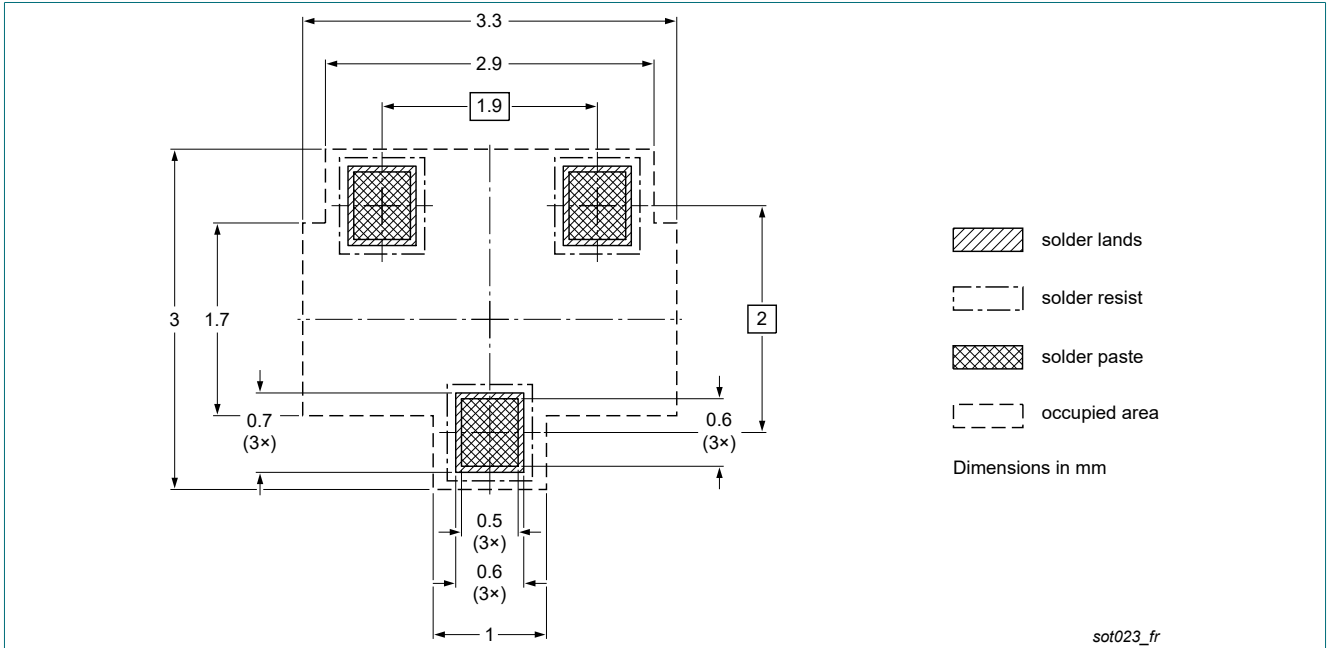


Fig. 20. Reflow soldering footprint for SOT23

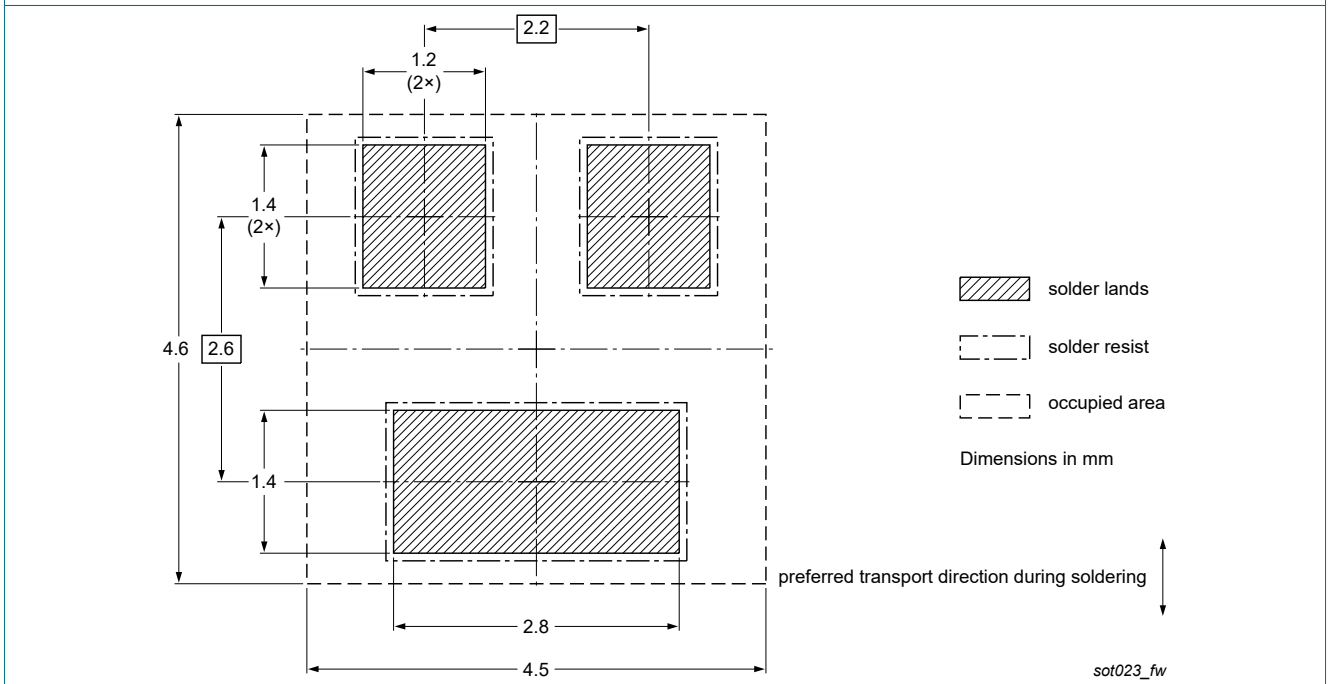


Fig. 21. Wave soldering footprint for SOT23

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2ETH100-T v.1	20191213	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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