PESD2V8R1BSF

Ultra low capacitance bidirectional ESD protection diode

5 November 2019 **Product data sheet**

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS Protection family. This device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package. The TrEOS Protection family is optimized for safeguarding very sensitive high-speed interfaces against ESD pulses with a high level of robustness.

2. Features and benefits

- Suitable for USB4 and Thunderbolt3 data lines
- Backwards compatible to USB 3.2 due to V_{RWM} = 2.8 V
- Extremely low insertion loss of -0.21 dB at 10 GHz
- Extremely low return loss of -17.4 dB at 10 GHz
- Bidirectional ESD protection of one line
- Extremely low diode capacitance C_d = 0.1 pF
- ESD protection up to ±10 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

ESD and surge protection for:

- USB4 and Thunderbolt3 data lines
- very sensitive interface lines

in portable electronics, communication, consumer and computing devices.

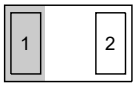
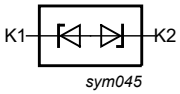
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-2.8	-	2.8	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.1	0.15	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DSN0603-2 (SOD962-2)**	
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2V8R1BSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD2V8R1BSF	B

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-2.8	2.8	V
I_{PPM}	rated rated peak pulse current	t_p = 8/20 µs	[1]	-	4.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-40	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-	10	kV
		IEC 61000-4-2; air discharge	[2]	-	15	kV

[1] According to IEC 61000-4-5 and IEC 61643-321.
[2] Device stressed with ten non-repetitive ESD pulses.

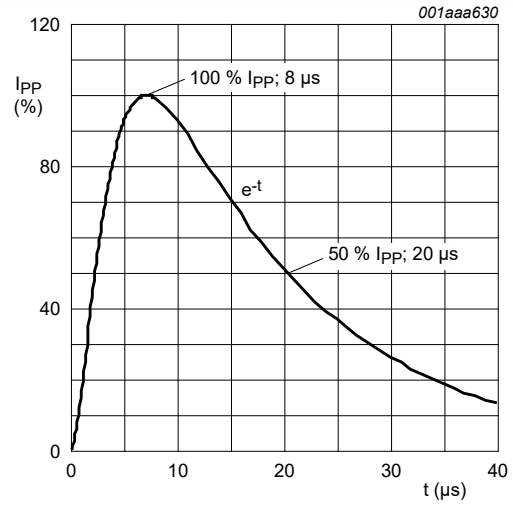


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

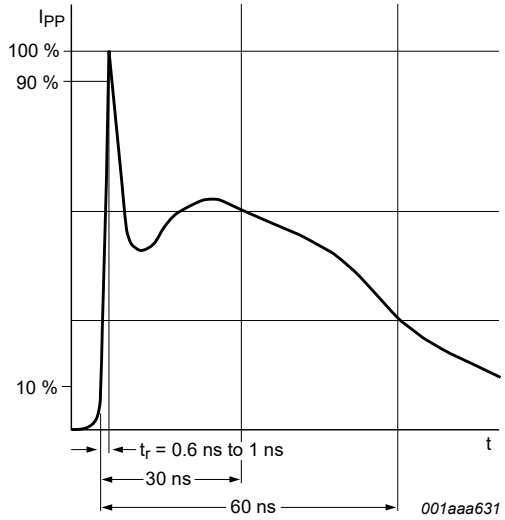


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_R = 0.1 mA; T_{amb} = 25 °C		7.5	9	11	V
I_{RM}	reverse leakage current	V_{RWM} = 2.8 V; T_{amb} = 25 °C		-	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.1	0.15	pF
		f = 2.5 GHz; V_R = 0 V; T_{amb} = 25 °C		-	0.1	-	pF
V_{CL}	clamping voltage	I_{PPM} = 4.5 A; t_p = 8/20 µs; T_{amb} = 25 °C	[1]	-	-	5	V
		I_{PP} = 8 A; t_p = TLP; T_{amb} = 25 °C	[2]	-	6	-	V
R_{dyn}	dynamic resistance	I_R = 10 A; T_{amb} = 25 °C	[2]	-	0.45	-	Ω
α_{IL}	insertion loss	f = 10 GHz		-	-0.21	-	dB
α_{RL}	return loss			-	-17.4	-	dB

[1] According to IEC 61000-4-5 and IEC 61643-321.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

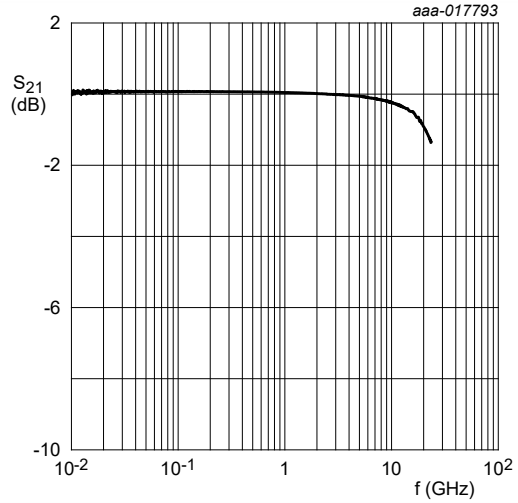


Fig. 3. Insertion loss; typical values

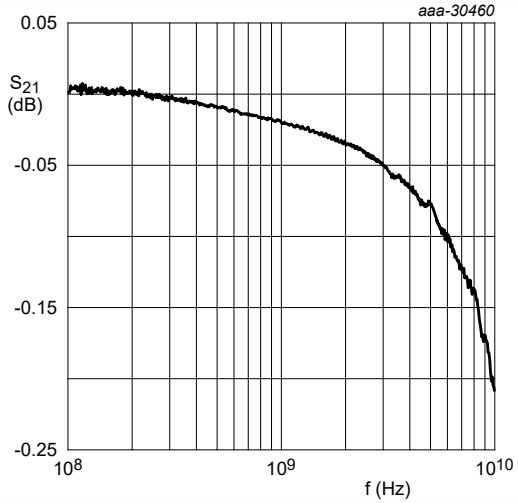


Fig. 4. Insertion loss; typical values

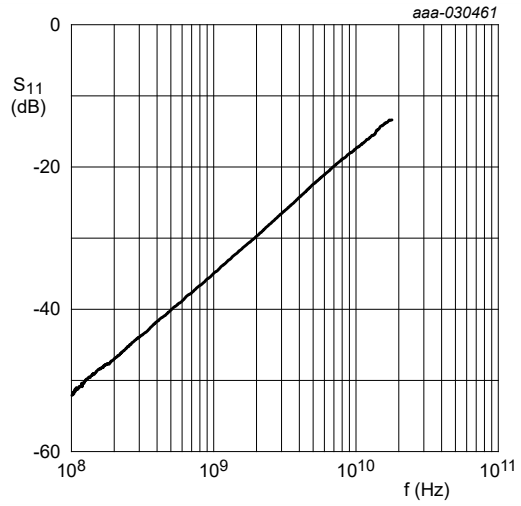
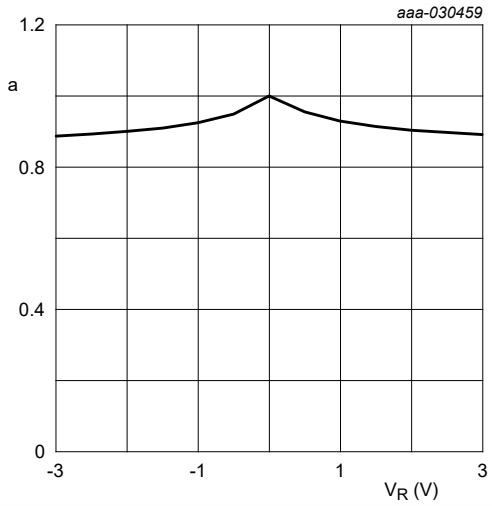


Fig. 5. Return loss; typical values



$$a = \frac{C_d}{C_d(V_{RWM} = 0\ V)}$$

Fig. 6. Relative capacitance as a function of reverse standoff voltage; typical values

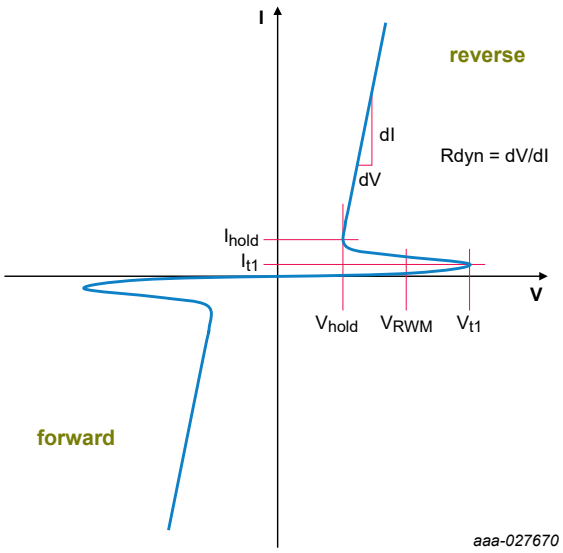
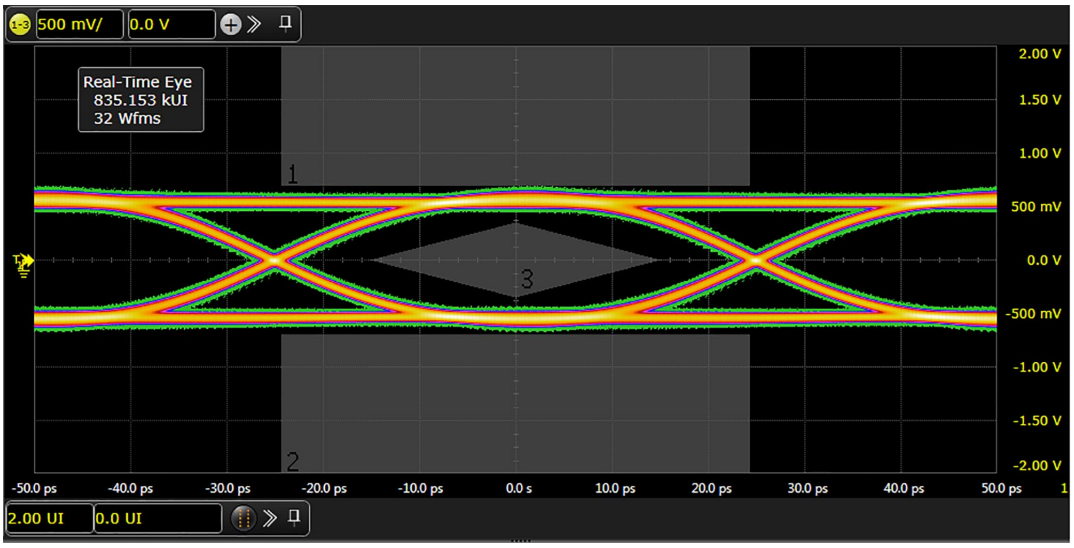
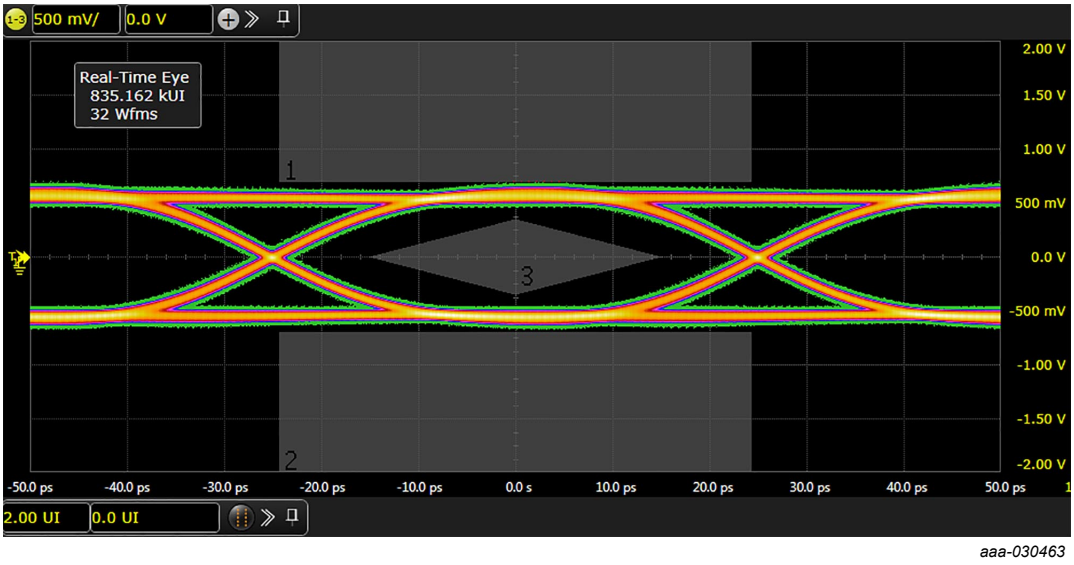


Fig. 7. V-I characteristics for a bidirectional ESD protection diode



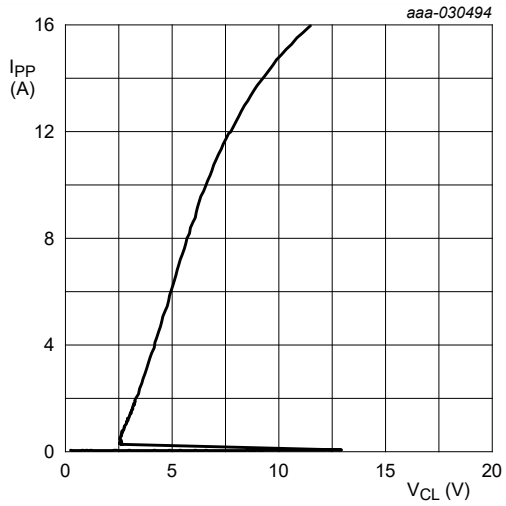
Data rate: 20 Gbit/s

Fig. 8. Thunderbolt eye diagram with device; typical values



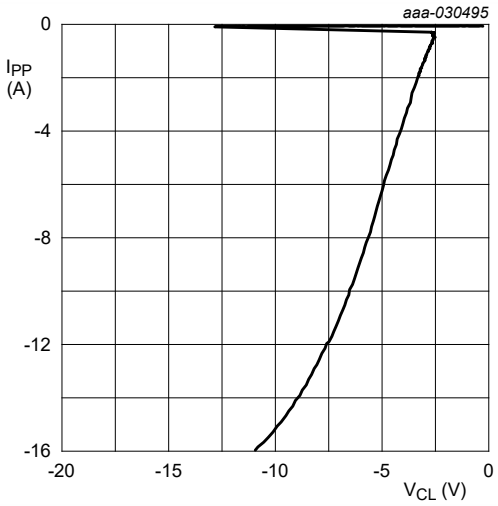
Data rate: 20 Gbit/s

Fig. 9. Thunderbolt eye diagram without device; typical values



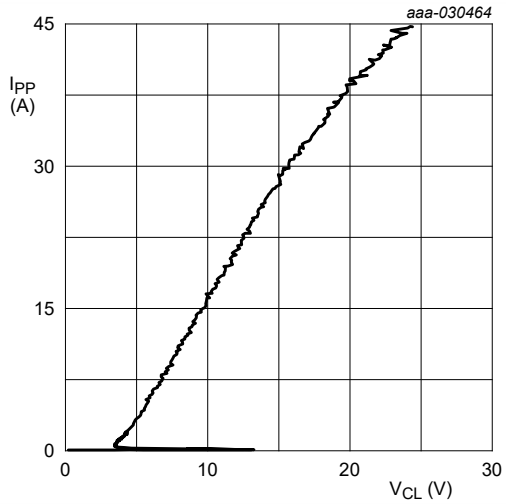
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 10. Dynamic resistance with positive clamping voltage; typical values



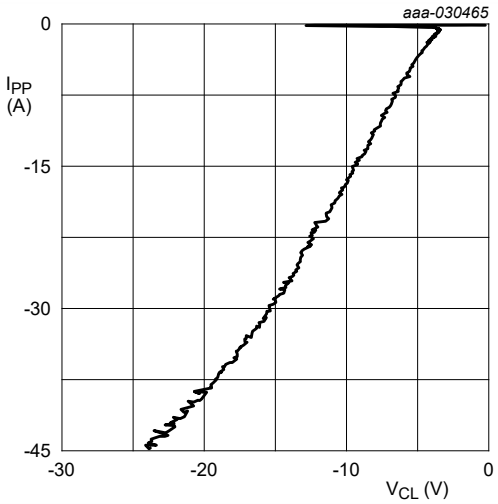
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 11. Dynamic resistance with negative clamping voltage; typical values



t_r = 600 ps
t_p = 5 ns; Very-Fast Transmission Line Pulse (VF-TLP)

Fig. 12. Dynamic resistance with positive clamping; typical values



t_r = 600 ps
t_p = 5 ns; Very-Fast Transmission Line Pulse (VF-TLP)

Fig. 13. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

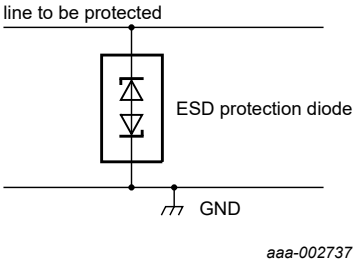


Fig. 14. Application diagram

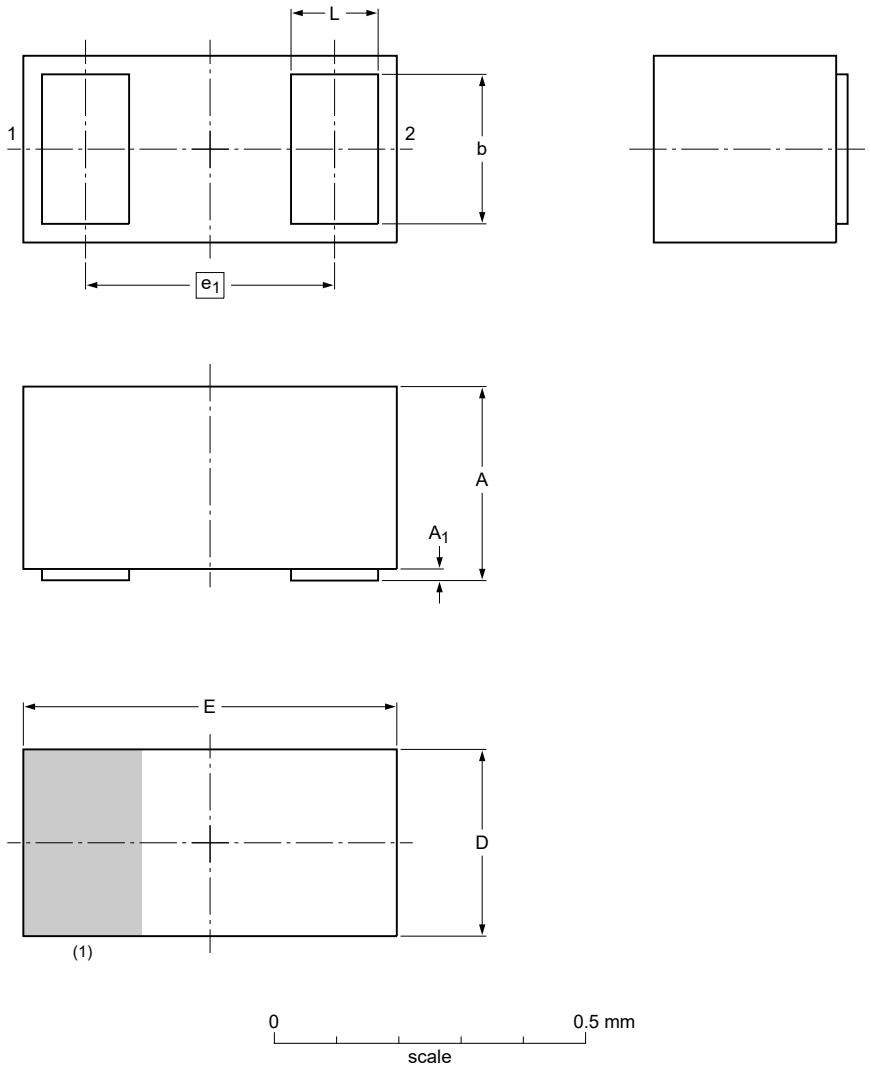
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm **SOD962-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	E	e_1	L
mm	max	0.32	0.03	0.25	0.325	0.625		0.15
	nom						0.4	
	min	0.28		0.23	0.275	0.575		0.13

Note
1. The marking bar indicates the cathode.

sod962-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD962-2						~~13-07-12~~ 13-07-17

Fig. 15. Package outline DSN0603-2 (SOD962-2)

12. Soldering

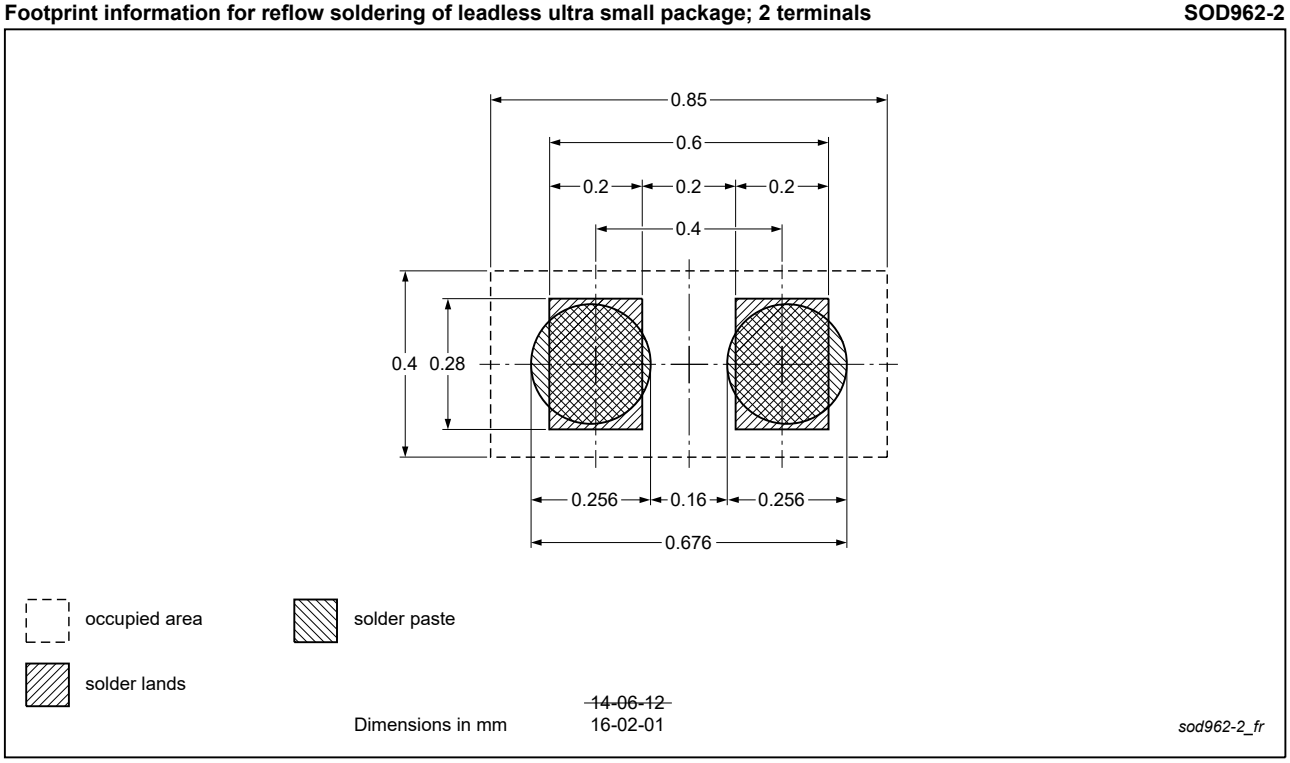


Fig. 16. Reflow soldering footprint for DSN0603-2 (SOD962-2)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2V8R1BSF v.1	20191105	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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