



PESD3V3X4UHM

4-fold ESD protection array for SD-card protection

12 February 2019

Product data sheet

1. General description

4-fold unidirectional ElectroStatic Discharge (ESD) protection array designed to protect up to four lines from the damage caused by ESD and other transients.

The device is housed in a leadless extremely thin small DFN1308-6 (SOT8006B) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Unidirectional ESD protection of up to 4 lines
- Very high surge robustness; $I_{PP} = 14.2$ A (average measured) for 8/20 μ s pulse
- Very low clamping voltage: $V_{CL} = 3.7$ V typ. for 11 A 8/20 μ s pulse
- ESD protection up to 25 kV
- Very low dynamic resistance $R_{dyn} = 0.15$ Ω (TLP)

3. Applications

ESD protection for SD-card in portable communication, consumer devices and computing devices.

4. Quick reference data

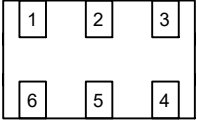
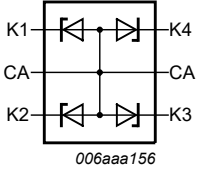
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--------------------------|---|-----|-----|-----|------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25$ °C | - | - | 3.3 | V |
| I_{PPM} | rated peak pulse current | $t_p = 8/20$ μ s; $T_{amb} = 25$ °C | [1] | - | 11 | A |
| V_{CL} | clamping voltage | $I_{PPM} = 11$ A; $t_p = 8/20$ μ s; $T_{amb} = 25$ °C | [1] | 3.7 | 4.5 | V |

[1] Non-repetitive current pulse 8/20 μ s exponential decay waveform according to IEC 61000-4-5.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------|---|--|
| 1 | K1 | cathode (diode 1) |  <p>DFN1308-6 (SOT8006B)</p> |  <p>006aaa156</p> |
| 2 | CA | common anode | | |
| 3 | K2 | cathode (diode 2) | | |
| 4 | K3 | cathode (diode 3) | | |
| 5 | CA | common anode | | |
| 6 | K4 | cathode (diode 4) | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|-----------|---|----------|
| | Name | Description | Version |
| PESD3V3X4UHM | DFN1308-6 | plastic, leadless extremely thin small package; 6 terminals; body 1.3 x 0.8 x 0.38 mm | SOT8006B |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|--------------|--------------|
| PESD3V3X4UHM | X4 |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|----------------------------|---------------------------------|--|-----|-----|-----|------------------|
| I_{PPM} | rated peak pulse current | $t_p = 8/20 \mu\text{s}$; $T_{amb} = 25 \text{ }^\circ\text{C}$ | [1] | - | 11 | A |
| T_j | junction temperature | | | - | 150 | $^\circ\text{C}$ |
| T_{amb} | ambient temperature | | | -55 | 150 | $^\circ\text{C}$ |
| T_{stg} | storage temperature | | | -65 | 150 | $^\circ\text{C}$ |
| ESD maximum ratings | | | | | | |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2 (contact discharge) | [2] | - | 25 | kV |
| | | IEC 61000-4-2 (air discharge) | [2] | - | 25 | kV |

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Device stressed with ten non-repetitive ESD pulses.

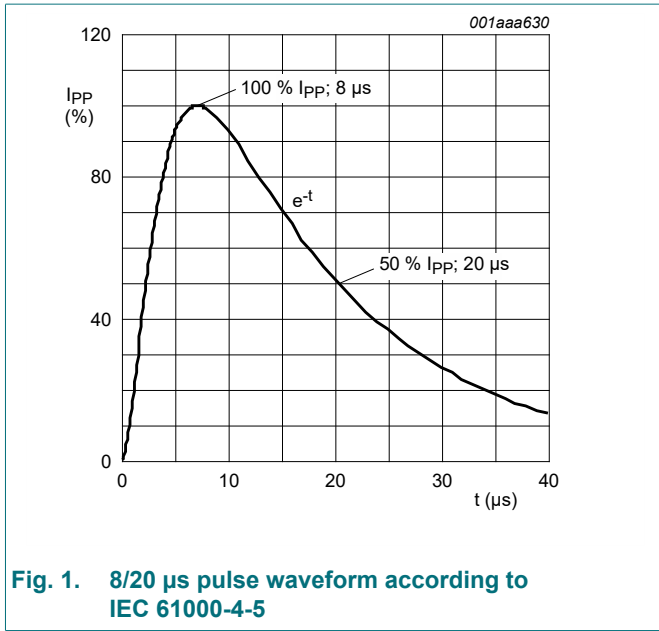


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

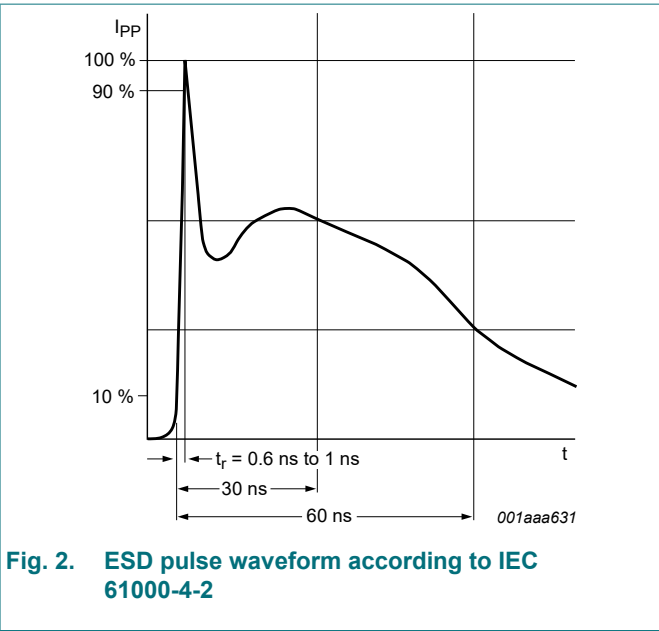


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

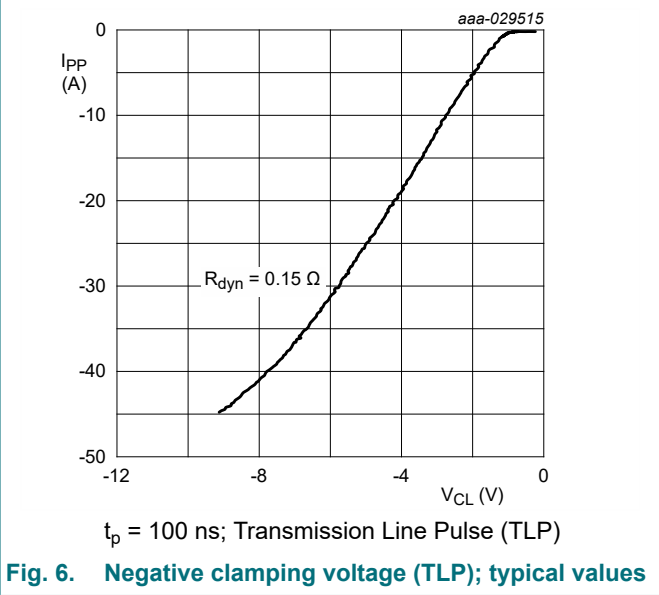
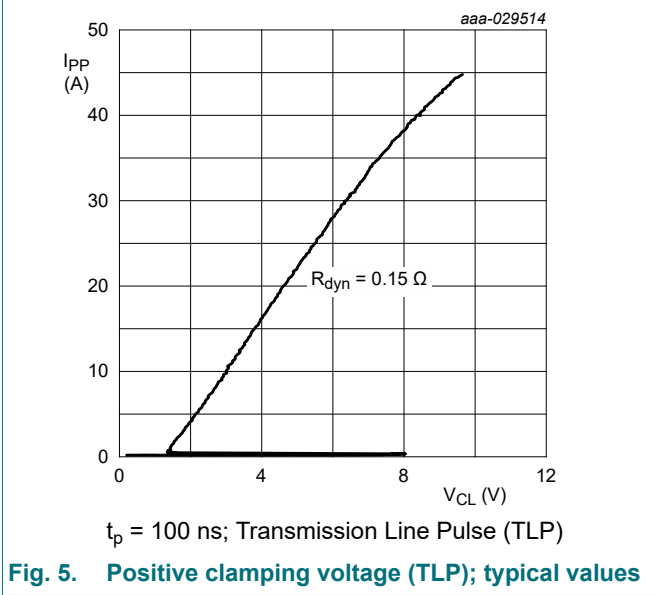
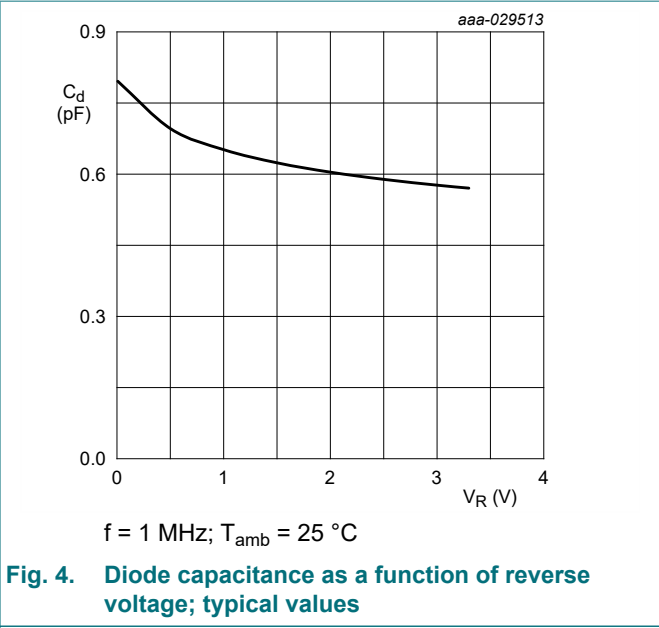
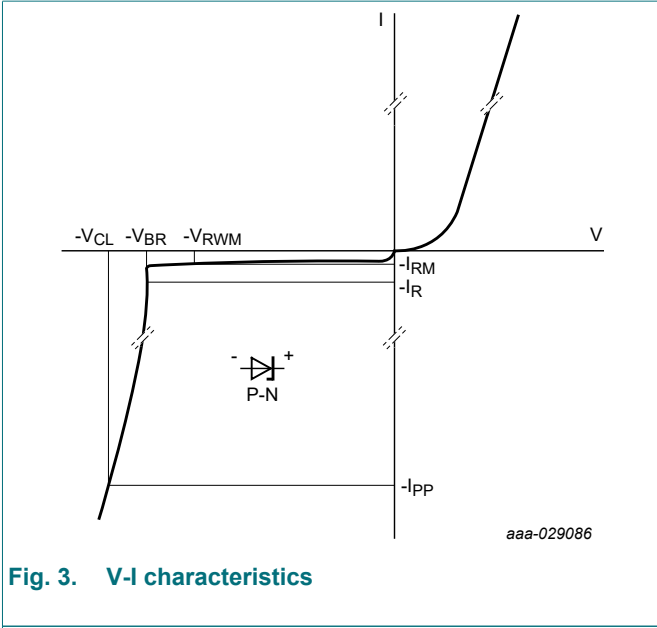
9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--------------------------|--|-----|------|-----|----------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25 \text{ }^\circ\text{C}$ | - | - | 3.3 | V |
| V_{BR} | breakdown voltage | $I_R = 1 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$ | 5 | 6.2 | 7 | V |
| I_{RM} | reverse leakage current | $V_{RWM} = 3.3 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$ | - | 1 | 100 | nA |
| C_d | diode capacitance | $f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$ | - | 0.8 | 0.9 | pF |
| V_{CL} | clamping voltage | $I_{PP} = 1 \text{ A}; t_p = 8/20 \mu s; T_{amb} = 25 \text{ }^\circ\text{C}$ [1] | - | 2 | - | V |
| | | $I_{PPM} = 11 \text{ A}; t_p = 8/20 \mu s; T_{amb} = 25 \text{ }^\circ\text{C}$ [1] | - | 3.7 | 4.5 | V |
| | | $I_{PP} = 16 \text{ A}; t_p = 100 \text{ ns}; T_{amb} = 25 \text{ }^\circ\text{C}$ [2] | - | 3.8 | - | V |
| R_{dyn} | dynamic resistance | $I_R = 10 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$ [2] | - | 0.15 | - | Ω |
| V_{t1} | trigger voltage | $T_{amb} = 25 \text{ }^\circ\text{C}$ | - | 8.1 | - | V |

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100 \text{ ns}$; square pulse; ANSI/ESD STM5.5.1-2008.



4-fold ESD protection array for SD-card protection

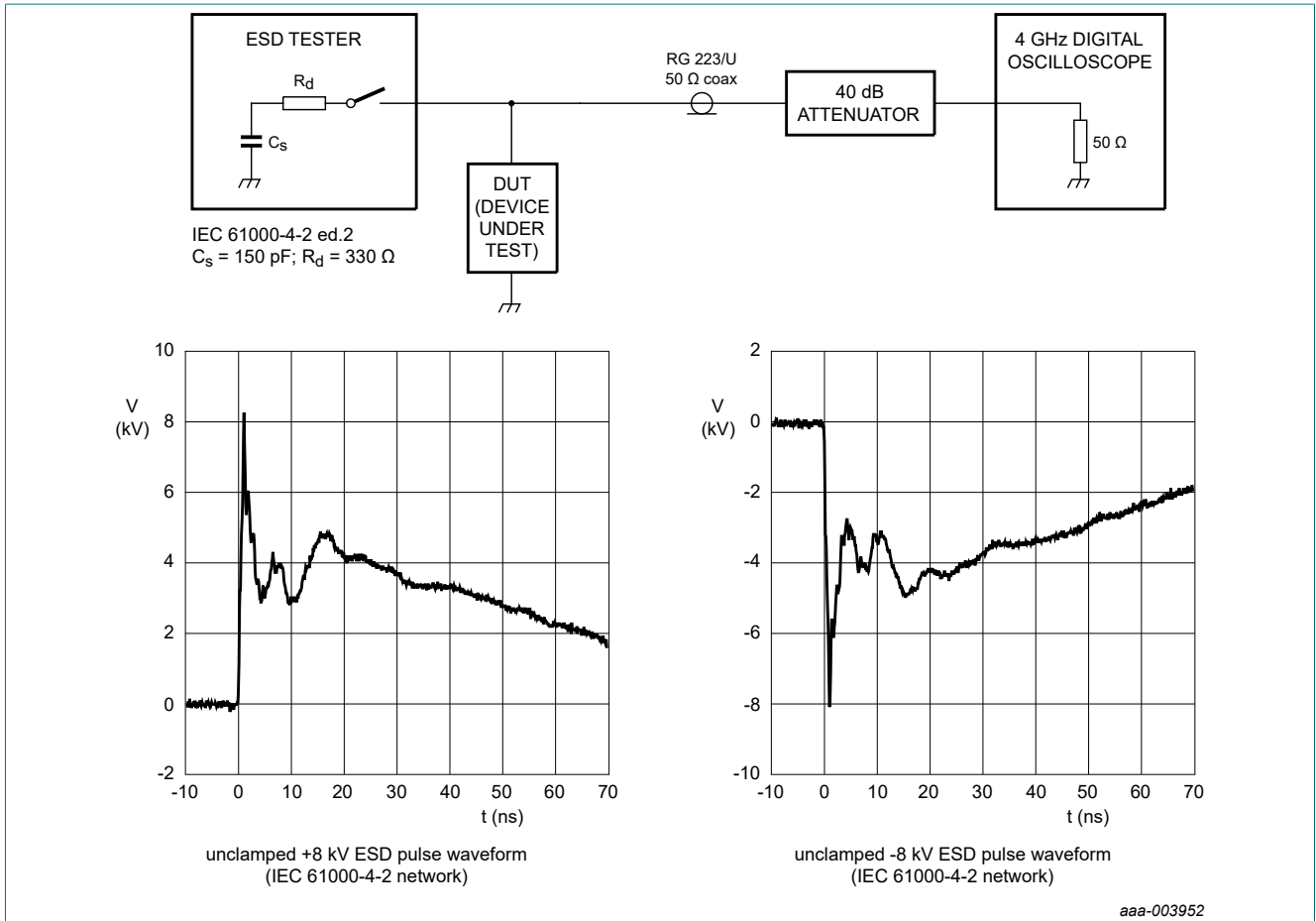


Fig. 7. ESD clamping test setup and waveforms

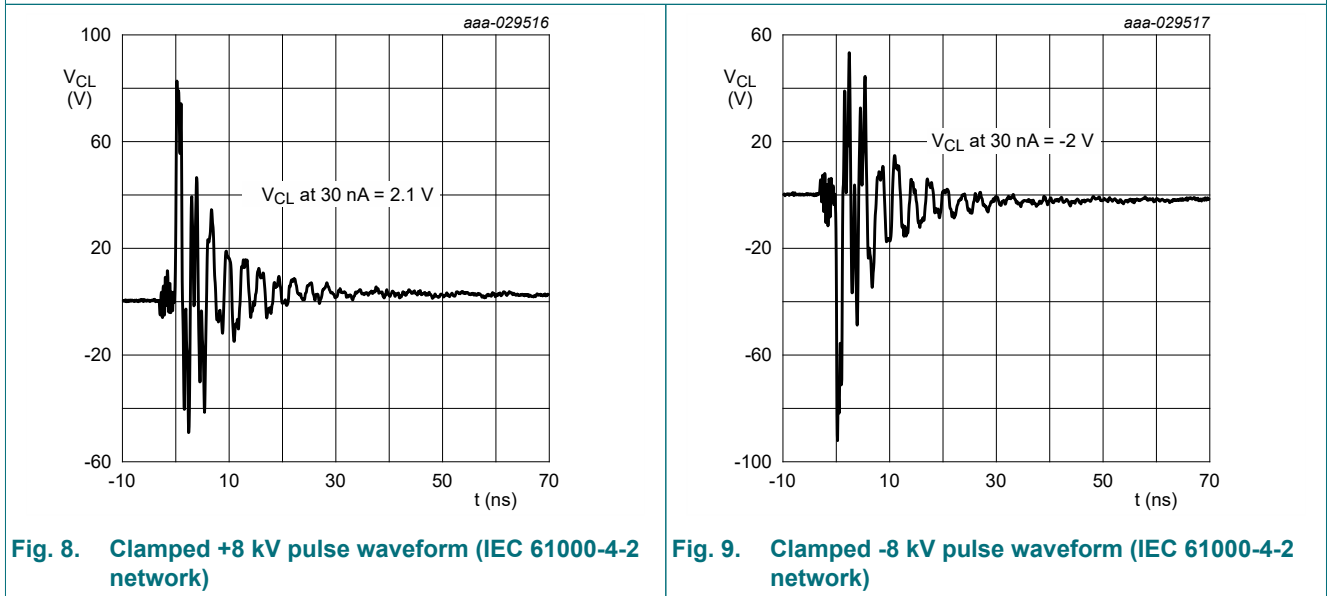


Fig. 8. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

Fig. 9. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The device is designed for protection of up to 4 unidirectional data lines from the damage caused by ESD and surge pulses. The device is suitable on lines where the signal polarities are above or below ground.

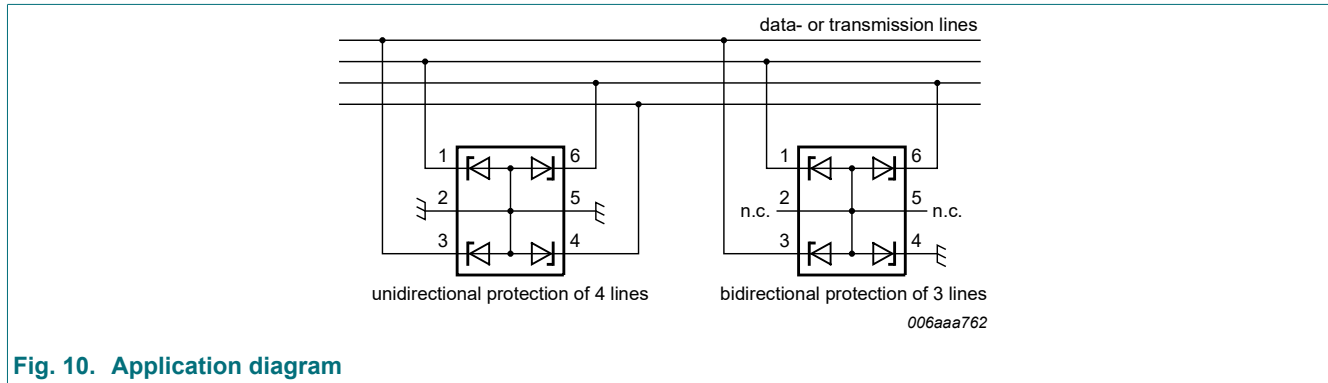


Fig. 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- Place the device as close to the input terminal or connector as possible
- Minimize the path length between the device and the protected line.
- Keep parallel signal paths to a minimum.
- Avoid running protected conductors in parallel with unprotected conductors.
- Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- Minimize the length of the transient return path to ground.
- Avoid using shared transient return paths to a common ground point.
- Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

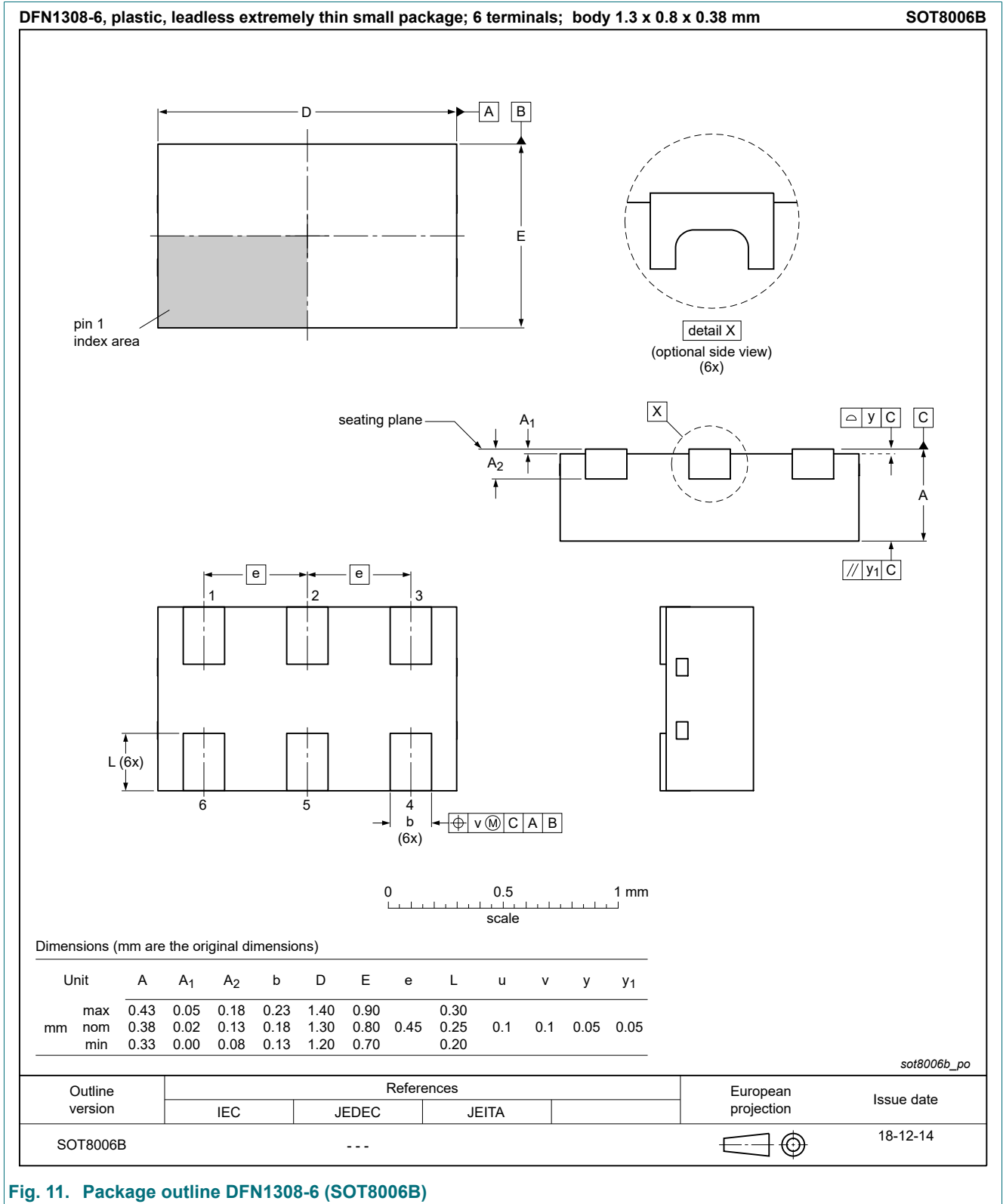


Fig. 11. Package outline DFN1308-6 (SOT8006B)

12. Soldering

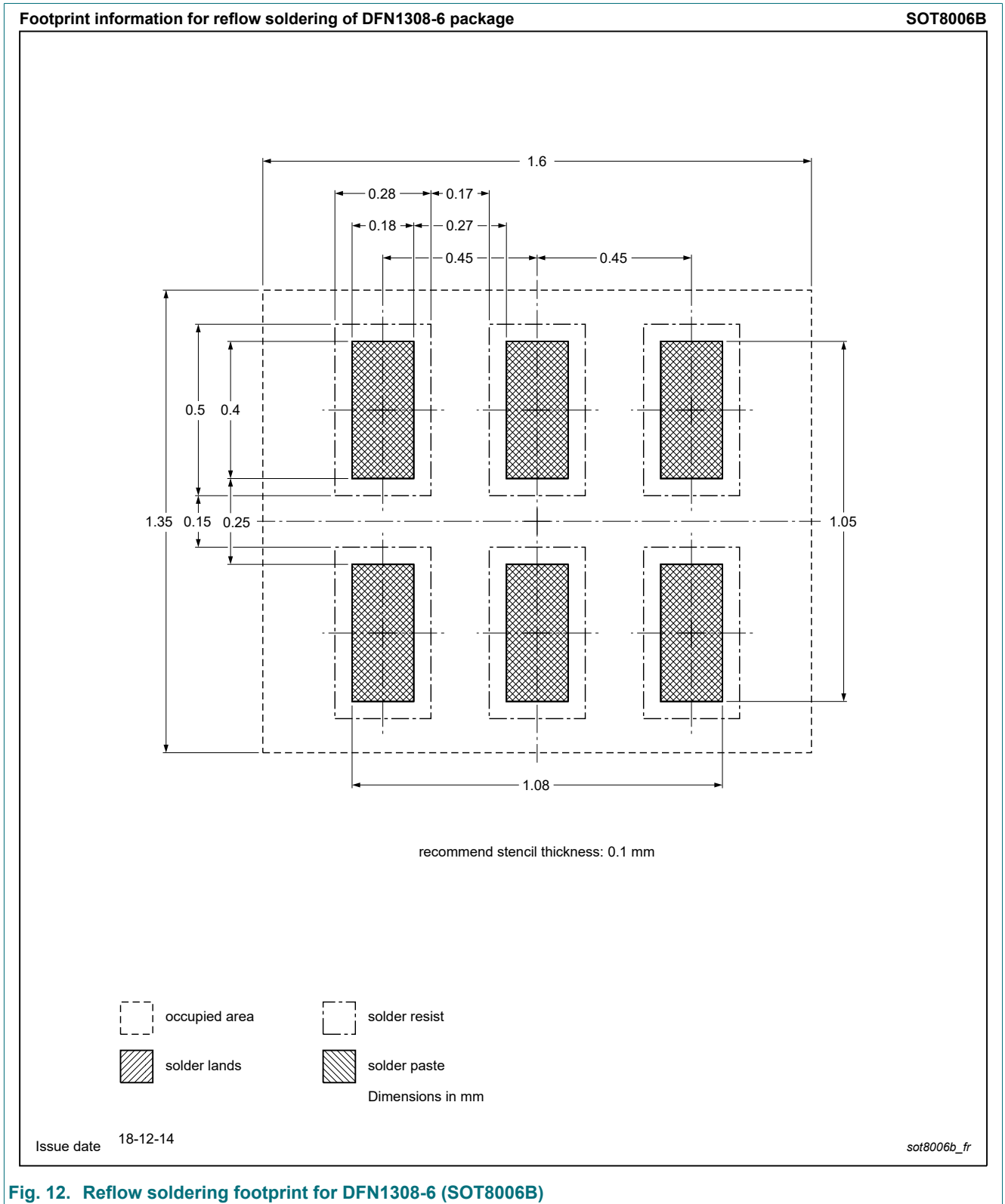


Fig. 12. Reflow soldering footprint for DFN1308-6 (SOT8006B)

13. Revision history

Table 7. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--------------|--------------------|---------------|------------|
| PESD3V3X4UHM v.1 | 20190212 | Product data sheet | - | - |

4-fold ESD protection array for SD-card protection

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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