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Kind regards,

Team Nexperia



PESD5V0V1BDSF

Very low capacitance bidirectional ESD protection diode

Rev. 1 — 17 April 2012

Product data sheet

1. Product profile

1.1 General description

Very low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DSN0603-2 (SOD962) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

1.2 Features and benefits

- Bidirectional ESD protection of one line
- Very low diode capacitance $C_d = 5.3$ pF
- ESD protection up to ± 25 kV according to IEC 61000-4-2
- Ultra small SMD package
- Optimized diode structure for ultra high ESD robustness

1.3 Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

1.4 Quick reference data


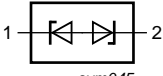
Table 1. Quick reference data

$T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-	-	5	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V	4	5.3	6	pF

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode (diode 1)	 <p>Transparent top view</p>	 <p>sym045</p>
2	cathode (diode 2)		



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0V1BDSF	DSN0603-2	leadless ultra small package; 2 terminals; body 0.6 × 0.3 × 0.3 mm	SOD962

4. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0V1BDSF	D

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{PP}	peak pulse power	$t_p = 8/20 \mu s$	[1] -	20	W
I_{PP}	peak pulse current	$t_p = 8/20 \mu s$	[1] -	2	A
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-55	+150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.

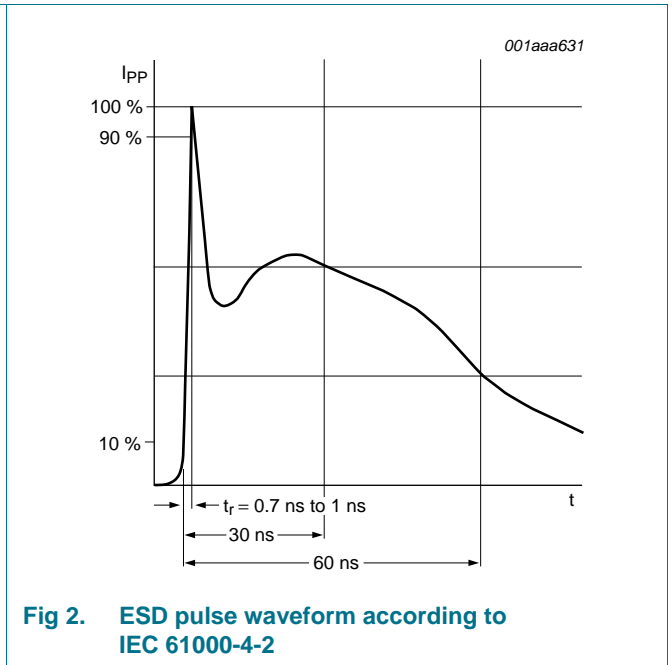
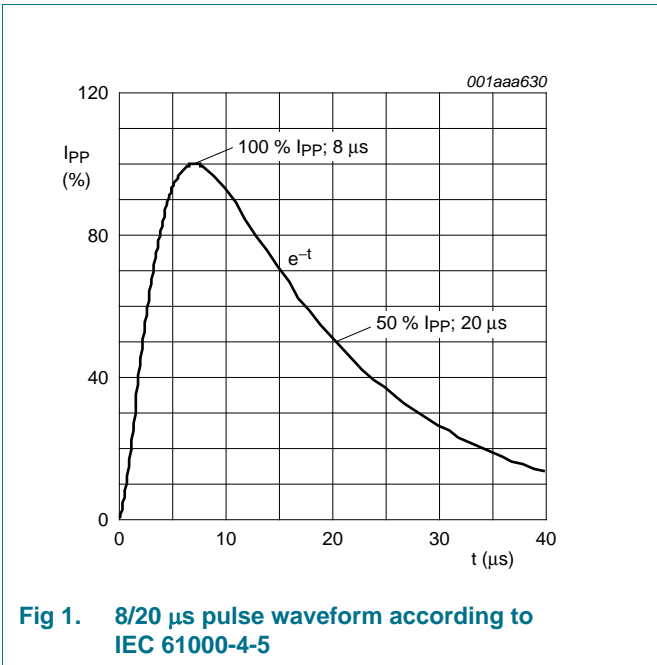
Table 6. ESD maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge) [1]	-	25	kV
		IEC 61000-4-2 (air discharge)	-	25	kV
		MIL-STD-883 (human body model)	-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

Table 7. ESD standards compliance

Standard	Conditions
IEC 61000-4-2, level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3B (human body model)	> 8 kV



6. Characteristics

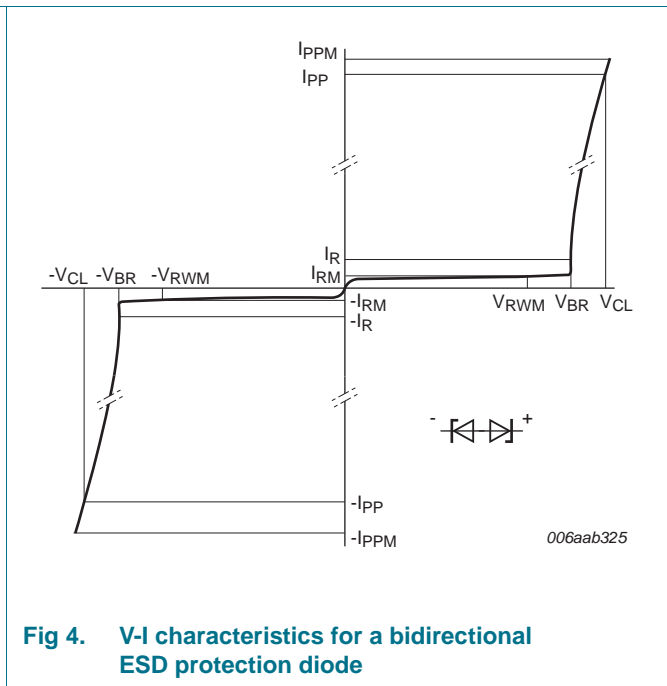
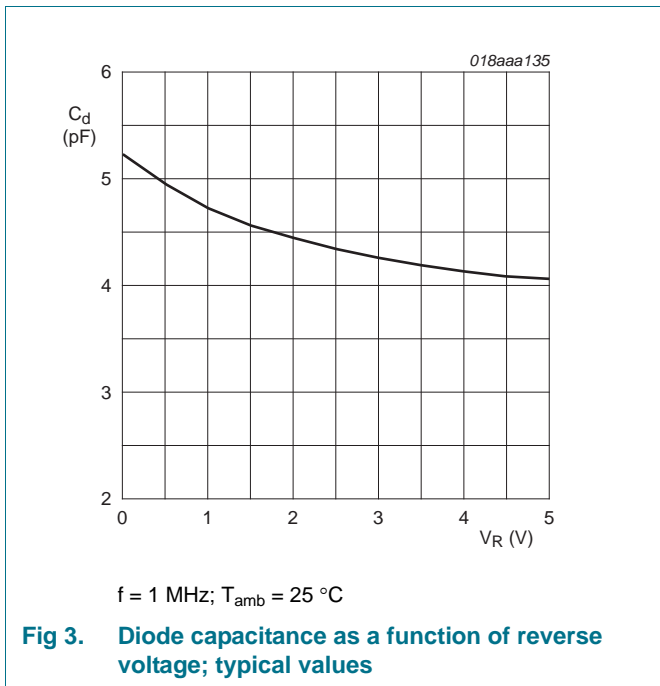
Table 8. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-	-	5	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}$	-	1	100	nA
V_{CL}	clamping voltage	$I_{PP} = 0.5\text{ A}$	[1]	-	11.5	V
		$I_{PP} = 1\text{ A}$	[1]	-	12.8	V
V_{BR}	breakdown voltage	$I_R = 1\text{ mA}$	6	-	10	V
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}$	4	5.3	6	pF
r_{dyn}	dynamic resistance		[2]	2.0	-	Ω

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100\text{ ns}$; square pulse; ANS/IESD STM5.1-2008.



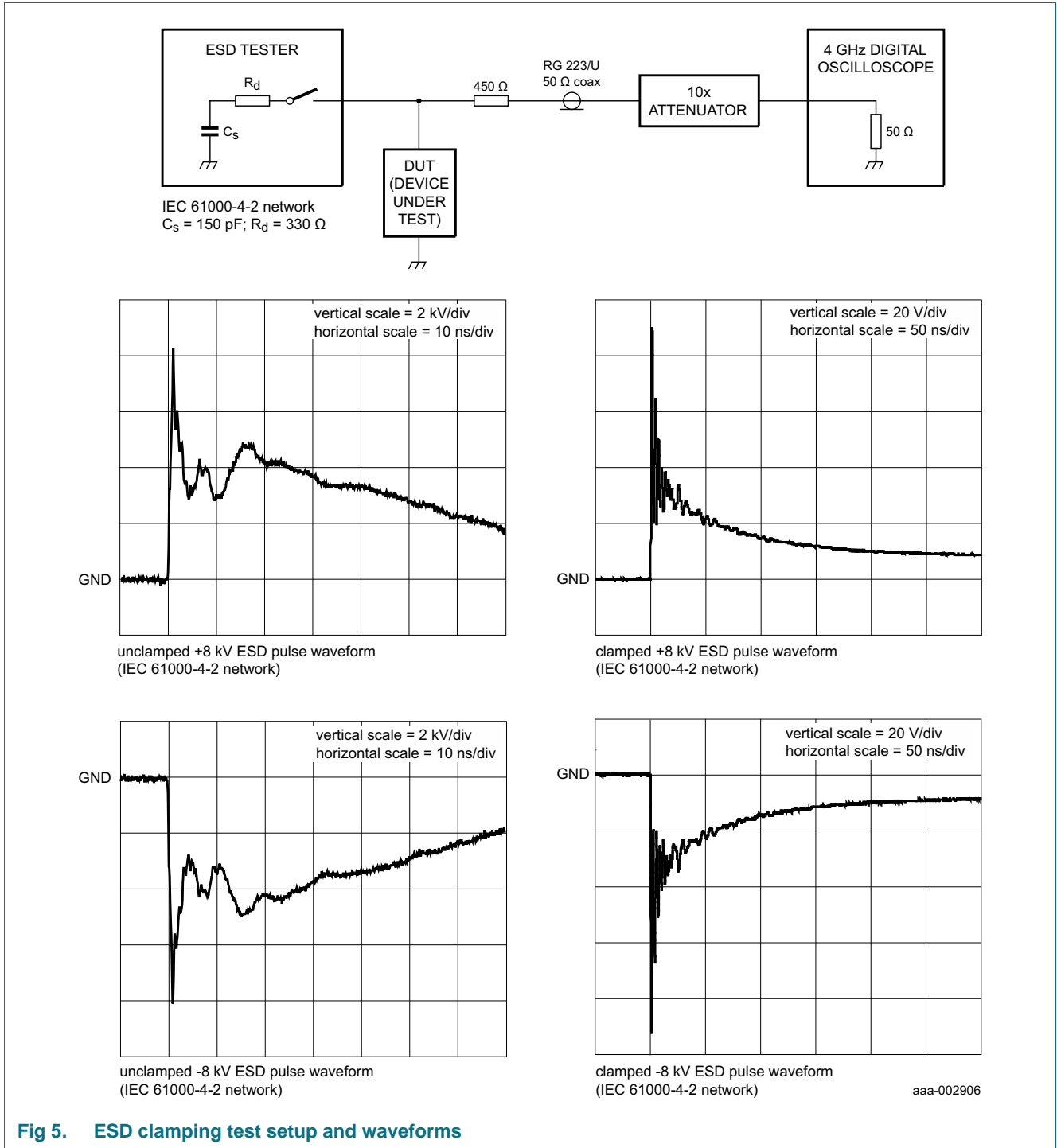


Fig 5. ESD clamping test setup and waveforms

7. Application information

The PESD5V0V1BDSF is designed for the protection of one data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative with respect to ground. It provides protection against surges with up to 20 W per line.

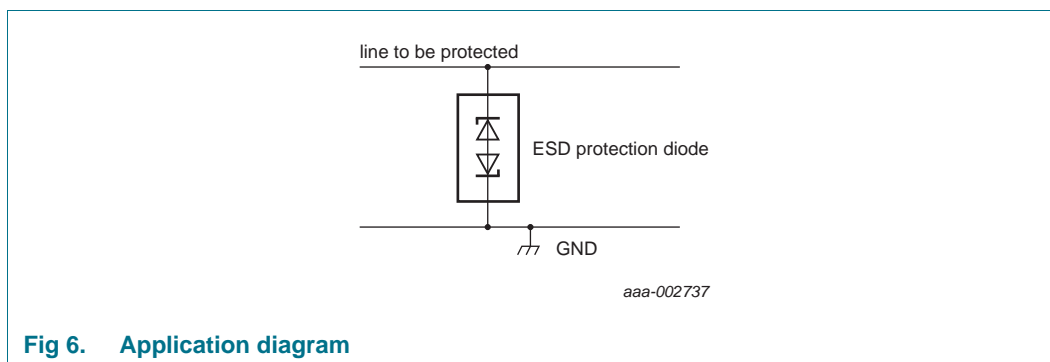


Fig 6. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

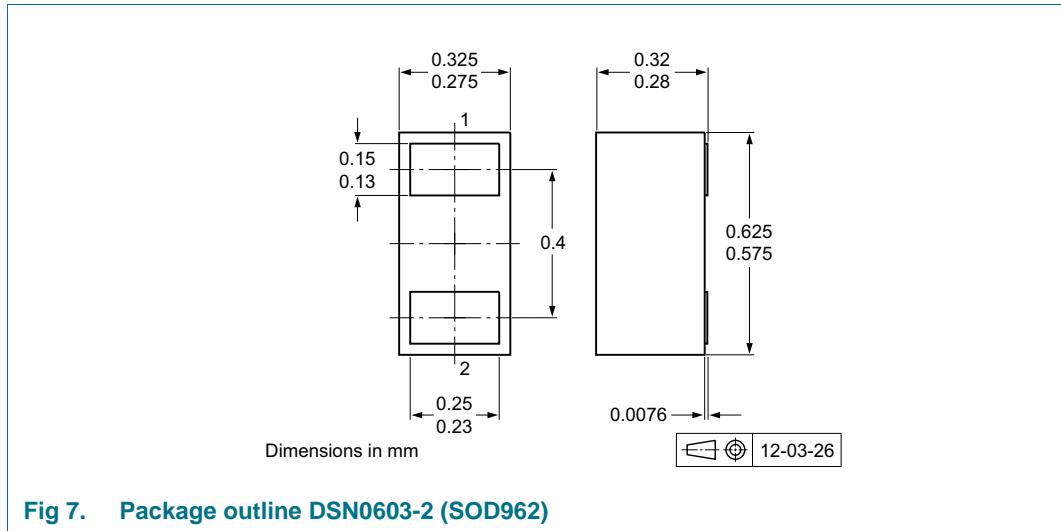


Fig 7. Package outline DSN0603-2 (SOD962)

9. Packing information

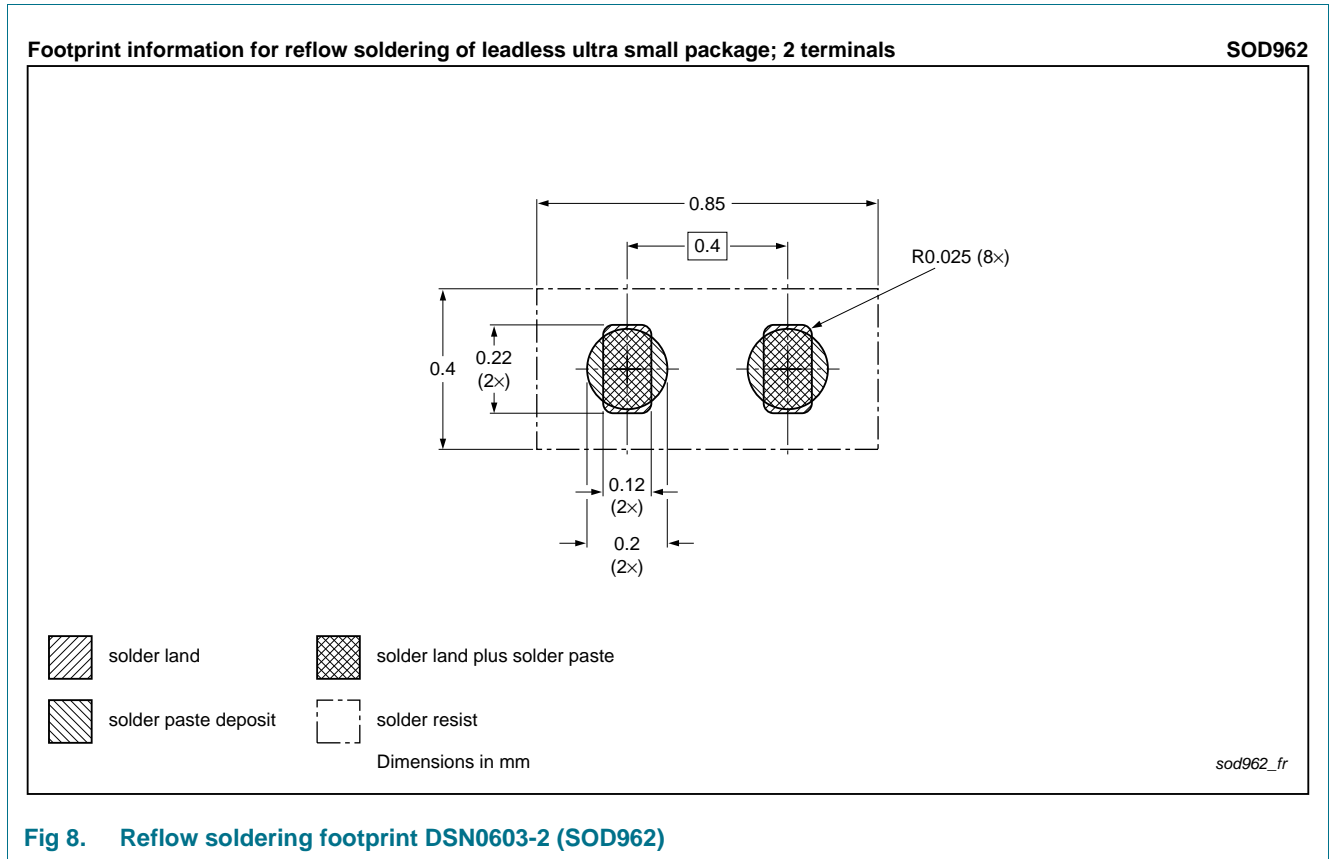
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity
			9000
PESD5V0V1BDSF	DSN0603-2 (SOD962)	2 mm pitch, 8 mm tape and reel	-315

[1] For further information and the availability of packing methods, see [Section 13](#).

10. Soldering



11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0V1BDSF v.1	20120417	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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