



PESD7V0H1BSF

Ultra low capacitance bidirectional ESD protection diode

9 April 2018

Product data sheet

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS Protection family. This device is housed in a DSN0603-2 (SOD962) leadless ultra small Surface-Mounted Device (SMD) package. The TrEOS Protection family is optimized for safeguarding very sensitive high-speed interfaces against ESD pulses with a high level of robustness.

2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low diode capacitance:
 - $C_d = 0.15$ pF at 1 MHz
 - $C_d = 0.13$ pF at 2.5 GHz
- ESD protection up to ± 15 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

ESD and surge protection for:

- ultra high-speed datalines
- very sensitive interface lines
- generic interface lines

in portable electronics, communication, consumer and computing devices.

4. Quick reference data


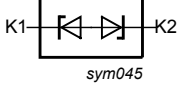
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--------------------------|---|-----|------|------|------|
| C_d | diode capacitance | $f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C | - | 0.15 | 0.19 | pF |
| | | $f = 2.5$ GHz; $V_R = 0$ V; $T_{amb} = 25$ °C | - | 0.13 | - | pF |
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25$ °C | - | - | 7 | V |

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5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------|--|--|
| 1 | K1 | cathode (diode 1) |  <p>Transparent top view</p> <p>DSN0603-2 (SOD962-2)</p> |  <p><i>sym045</i></p> |
| 2 | K2 | cathode (diode 2) | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|-----------|---|----------|
| | Name | Description | Version |
| PESD7V0H1BSF | DSN0603-2 | silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body | SOD962-2 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|--------------|--------------|
| PESD7V0H1BSF | G |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|----------------------------|---------------------------------|----------------------------------|-----|-----|-----|------|
| I_{PPM} | rated peak pulse current | $t_p = 8/20 \mu s$ | [1] | - | 7 | A |
| T_j | junction temperature | | | - | 150 | °C |
| T_{amb} | ambient temperature | | | -40 | 125 | °C |
| T_{stg} | storage temperature | | | -65 | 150 | °C |
| ESD maximum ratings | | | | | | |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [2] | - | 15 | kV |
| | | IEC 61000-4-2; air discharge | [2] | - | 15 | kV |

[1] According to IEC 61000-4-5 and IEC 61643-321.

[2] Device stressed with ten non-repetitive ESD pulses.

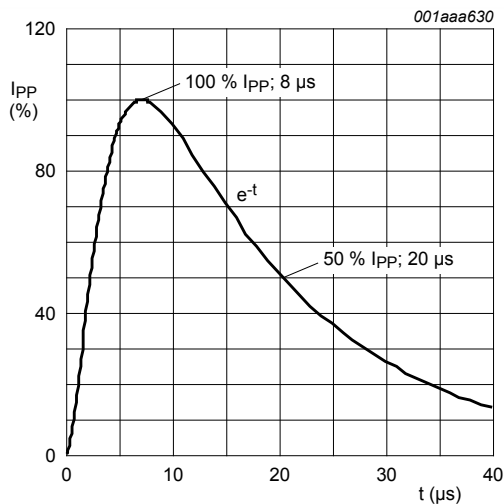


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

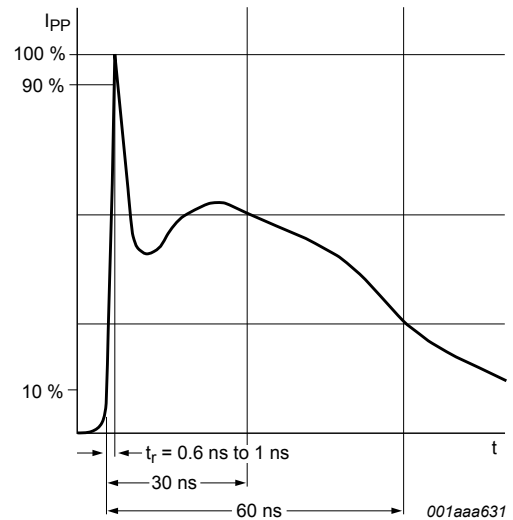


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--------------------------|---|-----|------|------|----------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | - | 7 | V |
| V_{BR} | breakdown voltage | $I_R = 0.1\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | 7.5 | 9 | 11 | V |
| I_{RM} | reverse leakage current | $V_{RWM} = 7\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 1 | 50 | nA |
| C_d | diode capacitance | $f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 0.15 | 0.19 | pF |
| | | $f = 2.5\text{ GHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 0.13 | - | pF |
| V_{CL} | clamping voltage | $I_{PPM} = 7\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ }^{\circ}\text{C}$ [1] | - | - | 5 | V |
| | | $I_{PP} = 8\text{ A}; t_p = \text{TLP}; T_{amb} = 25\text{ }^{\circ}\text{C}$ [2] | - | 4.4 | - | V |
| | | $I_{PP} = 16\text{ A}; t_p = \text{TLP}; T_{amb} = 25\text{ }^{\circ}\text{C}$ [2] | - | 6.3 | - | V |
| R_{dyn} | dynamic resistance | $I_R = 10\text{ A}; T_{amb} = 25\text{ }^{\circ}\text{C}$ [2] | - | 0.25 | - | Ω |

[1] According to IEC 61000-4-5 and IEC 61643-321.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100\text{ ns}$; square pulse; ANSI / ESD STM5.5.1-2008.

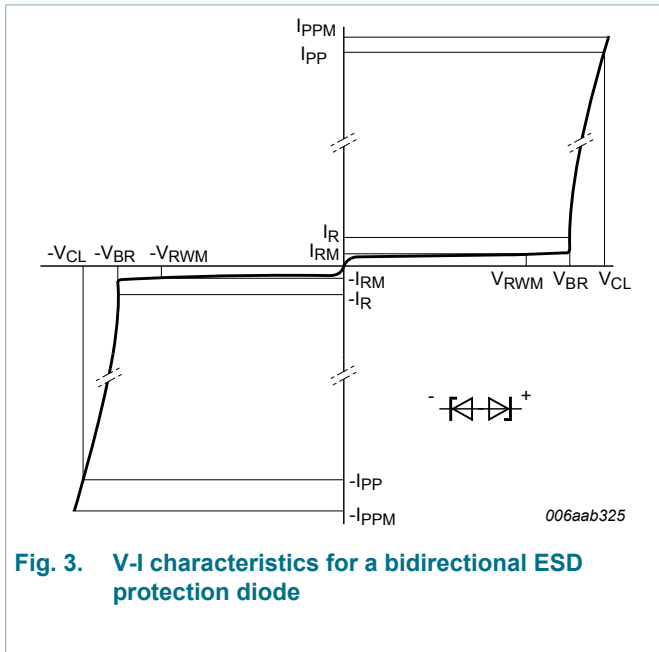


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

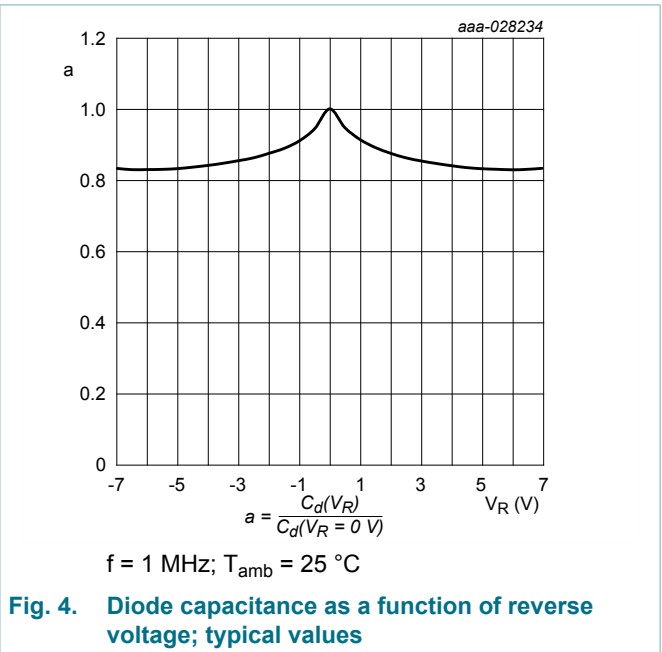


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

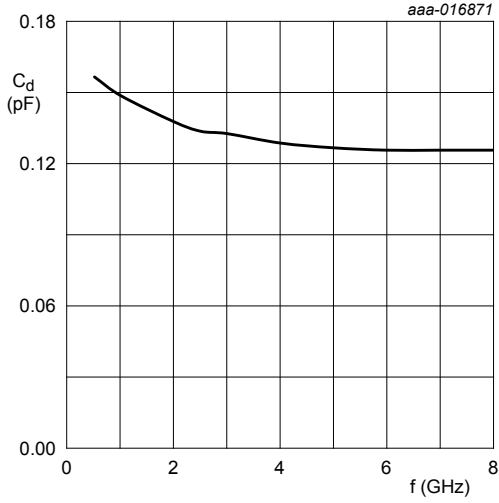


Fig. 5. Diode capacitance as a function of frequency; typical values

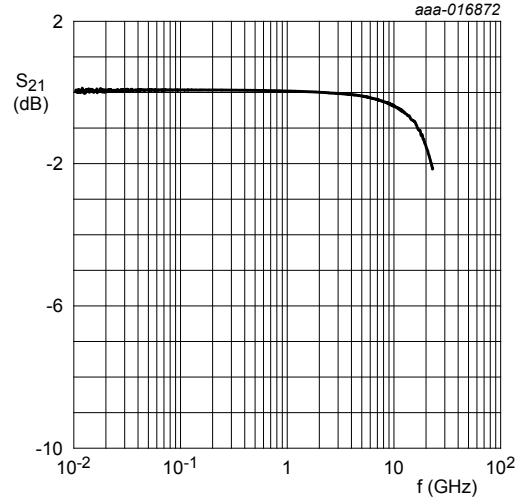
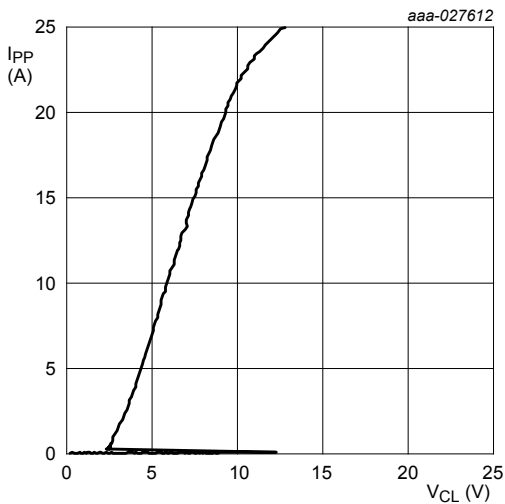
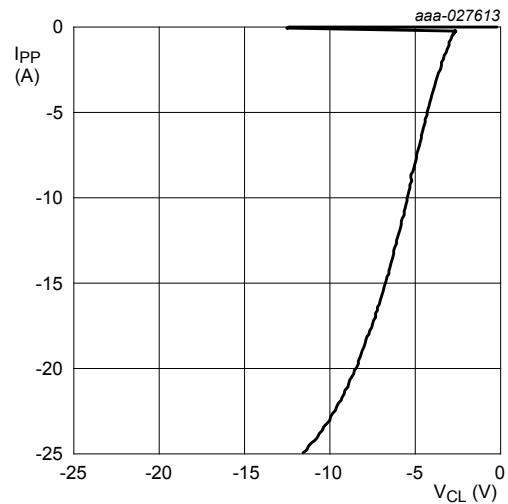


Fig. 6. Insertion loss; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 7. Dynamic resistance with positive clamping voltage



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 8. Dynamic resistance with negative clamping voltage

Ultra low capacitance bidirectional ESD protection diode

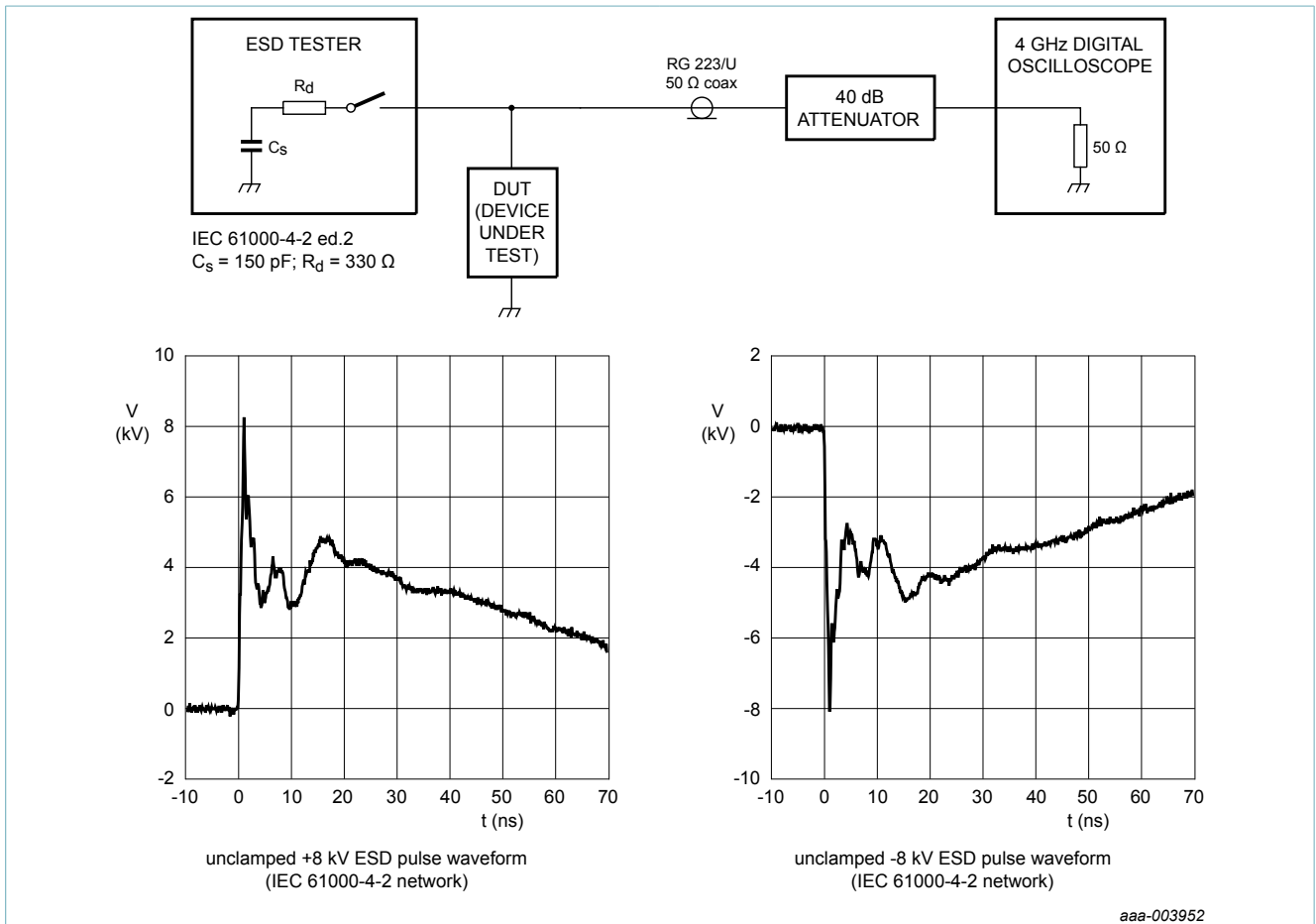


Fig. 9. ESD clamping test setup and waveforms

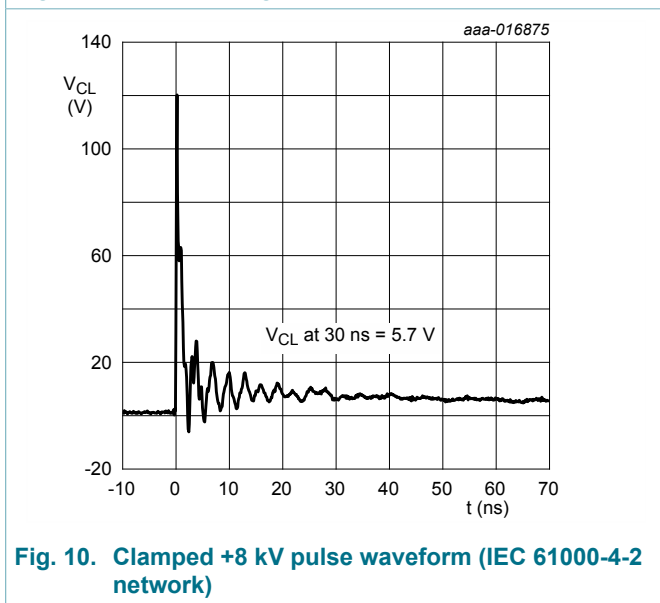


Fig. 10. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

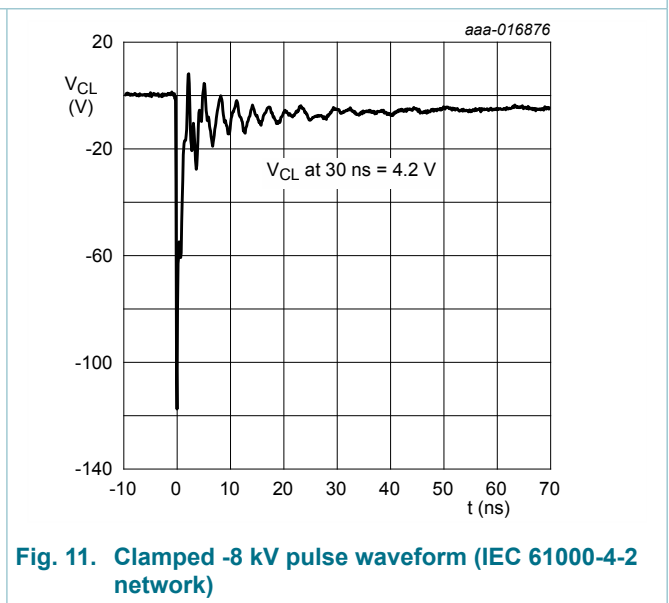


Fig. 11. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground. The device is not designed to be used on lines connected to a DC supply.

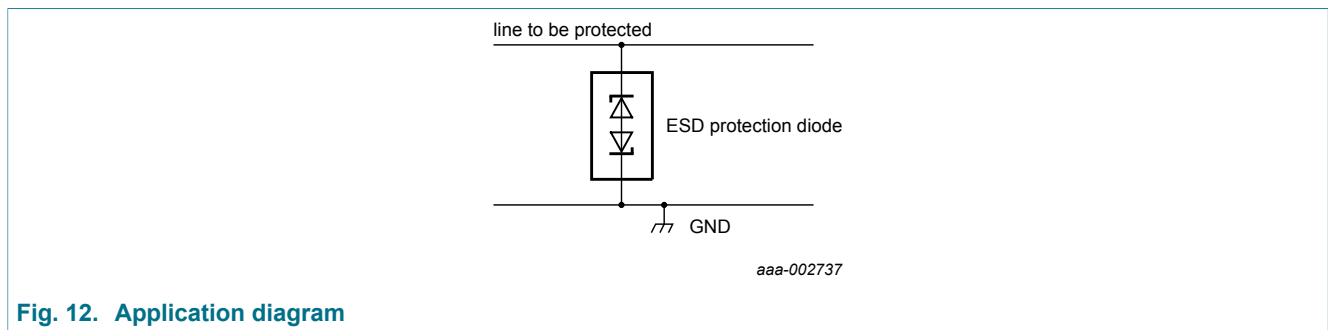


Fig. 12. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

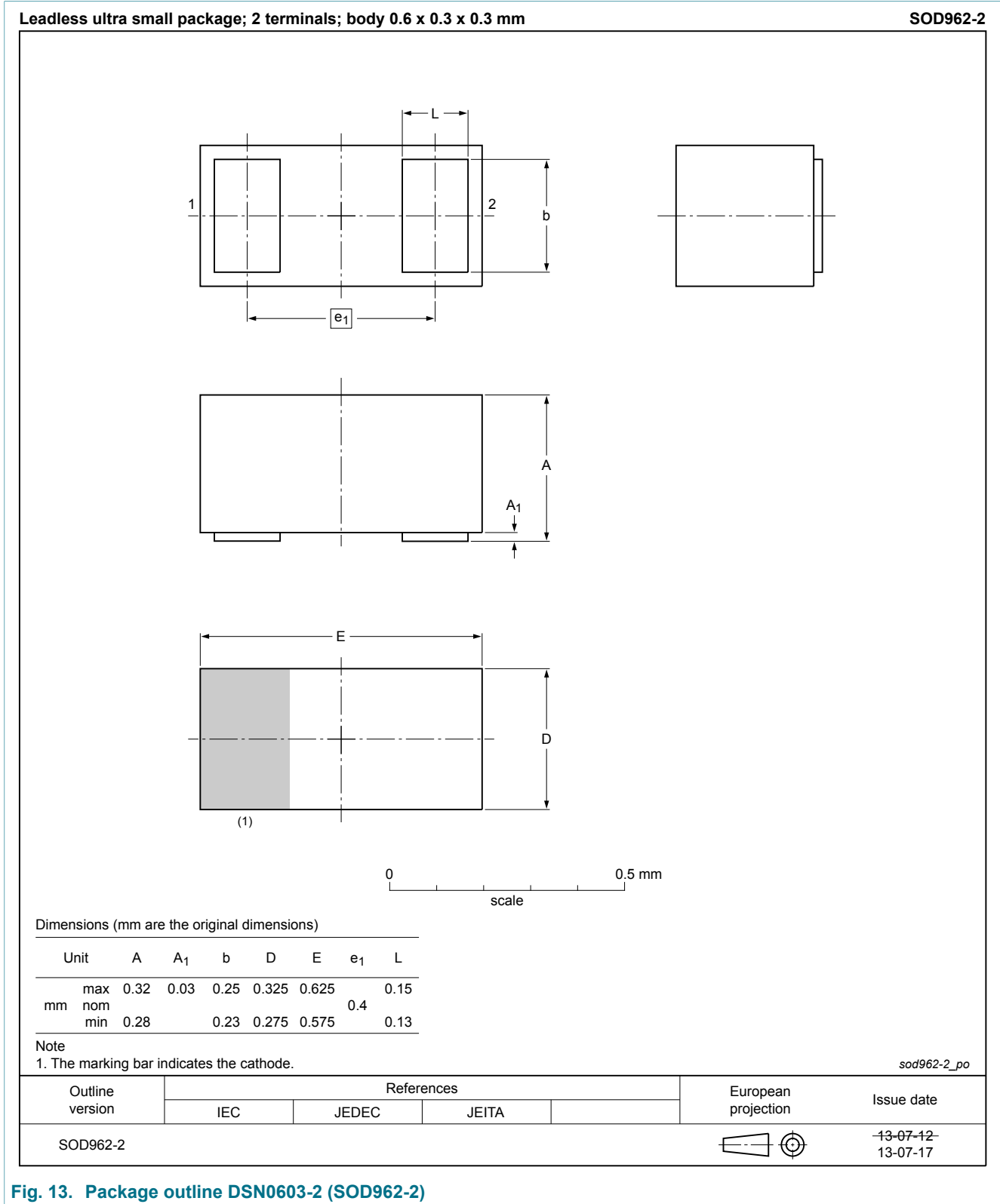
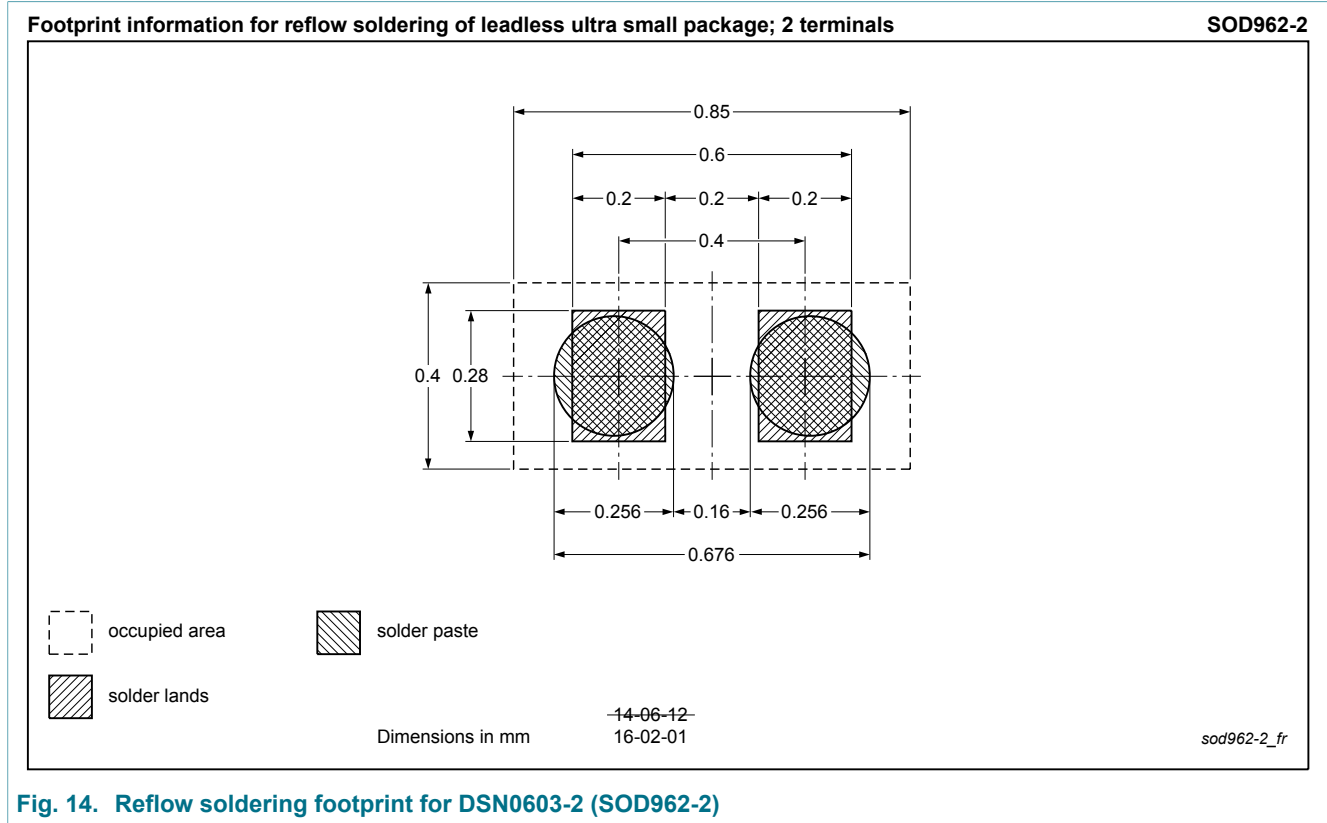


Fig. 13. Package outline DSN0603-2 (SOD962-2)

12. Soldering



13. Revision history

Table 7. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--------------|--------------------|---------------|------------|
| PESD7V0H1BSF v.1 | 20180409 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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15. Contents

| | |
|----------------------------------|----|
| 1. General description..... | 1 |
| 2. Features and benefits..... | 1 |
| 3. Applications..... | 1 |
| 4. Quick reference data..... | 1 |
| 5. Pinning information..... | 2 |
| 6. Ordering information..... | 2 |
| 7. Marking..... | 2 |
| 8. Limiting values..... | 3 |
| 9. Characteristics..... | 4 |
| 10. Application information..... | 7 |
| 11. Package outline..... | 8 |
| 12. Soldering..... | 9 |
| 13. Revision history..... | 10 |
| 14. Legal information..... | 11 |

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