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Kind regards,

Team Nexperia



# PH2625L

N-channel 25 V 2.8 mΩ logic level MOSFET in LPAK

Rev. 3 — 21 December 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology

### 1.2 Features and benefits

- Low thermal resistance
- Low threshold voltage
- Optimized for use in DC-to-DC converters
- Very low switching and conduction losses

### 1.3 Applications

- DC-to-DC converters
- Notebook computers
- Switched-mode power supplies
- Voltage regulators

### 1.4 Quick reference data

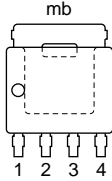
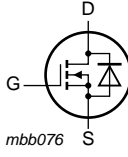
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	25	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	100	A
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	2	2.8	mΩ
		$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	3	4.1	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	7.3	-	nC
$Q_{G(tot)}$	total gate charge	see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	32	-	nC



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LPAK; Power-SO8)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PH2625L	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

## 4. Limiting values

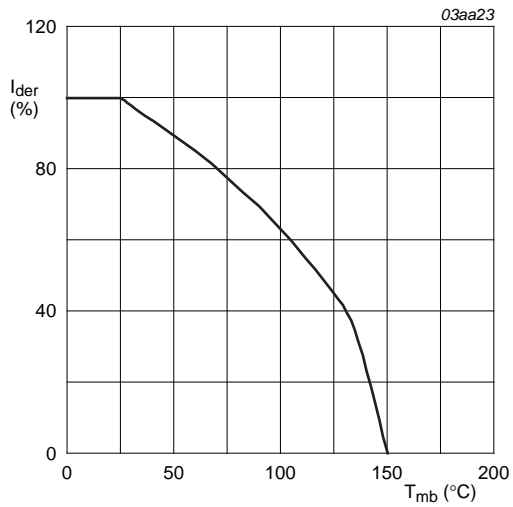
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	25	V	
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	63	A	
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	100	A	
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	300	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	62.5	W	
$T_{stg}$	storage temperature		-55	150	°C	
$T_j$	junction temperature		-55	150	°C	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	52	A	
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	156	A	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	unclamped; $t_p = 0.01\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $I_D = 7.1\text{ A}$ ; $V_{sup} \leq 25\text{ V}$	<a href="#">[1][2]</a>	-	2.5	mJ
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 71\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; unclamped; $t_p = 0.1\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	250	mJ	

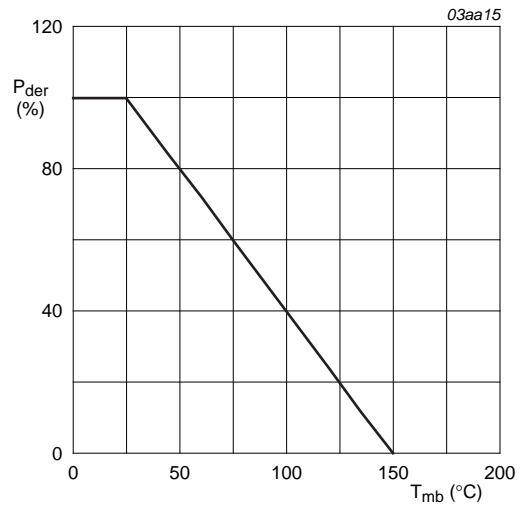
[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



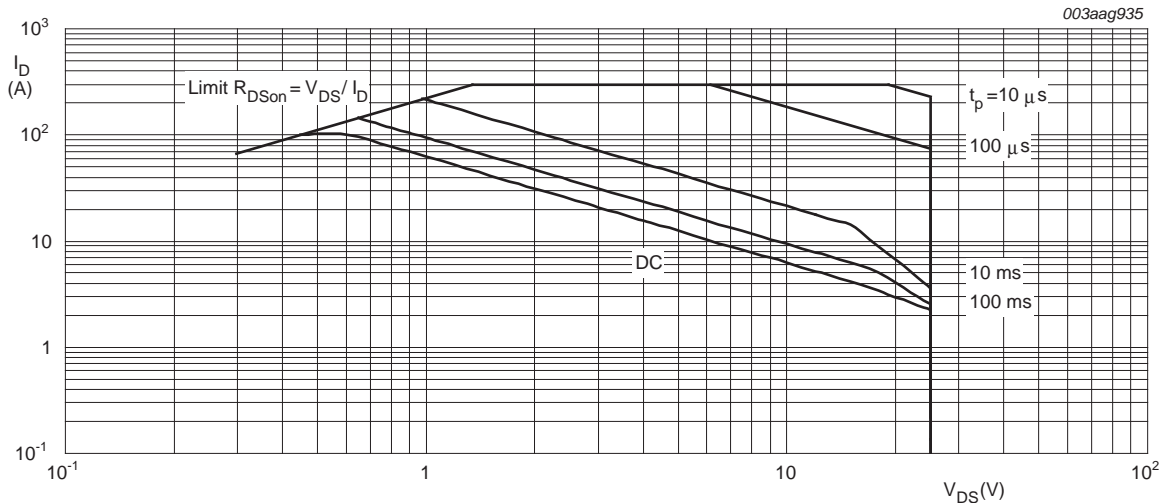
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W

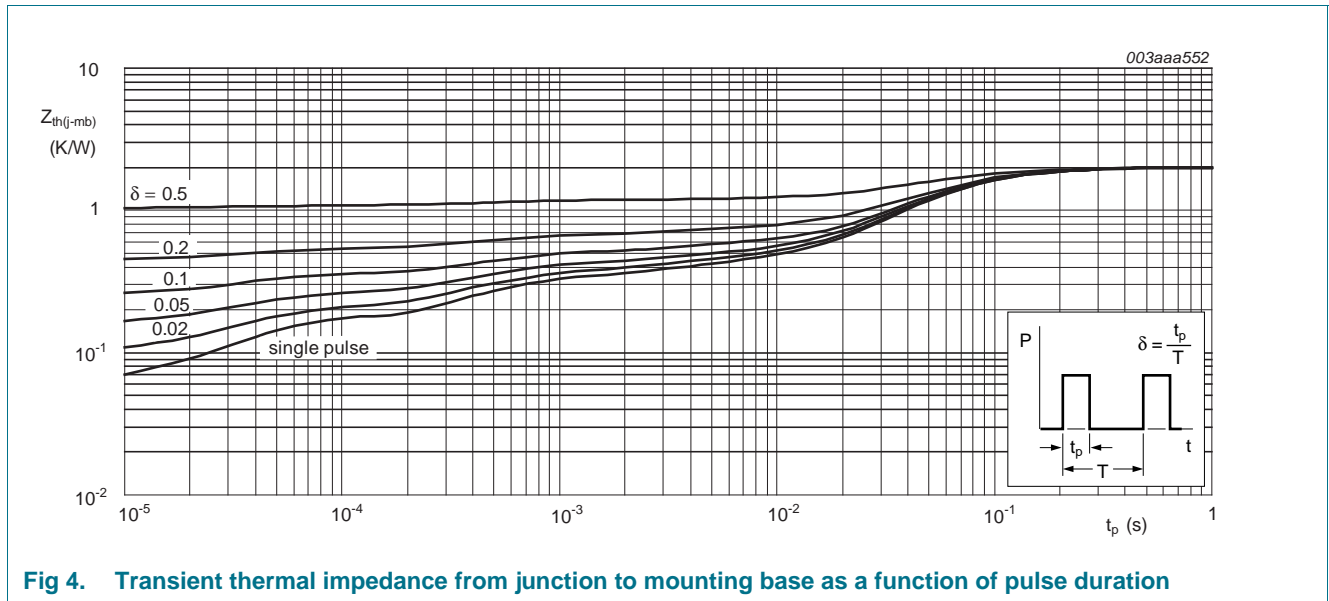


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	2.2	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	1	1.5	2	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.06	1	$\mu A$
		$V_{DS} = 25 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -16 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	3.2	4.3	mΩ
		$V_{GS} = 4.5 V$ ; $I_D = 25 A$ ; $T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	4.8	6.6	mΩ
		$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	2	2.8	mΩ
		$V_{GS} = 4.5 V$ ; $I_D = 25 A$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	3	4.1	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.5	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A$ ; $V_{DS} = 12 V$ ; $V_{GS} = 4.5 V$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	32	-	nC
		$I_D = 0 A$ ; $V_{DS} = 0 V$ ; $V_{GS} = 4.5 V$	-	26	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 A$ ; $V_{DS} = 12 V$ ; $V_{GS} = 4.5 V$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	9.6	-	nC
$Q_{GS1}$	pre-threshold gate-source charge		-	6	-	nC
$Q_{GS2}$	post-threshold gate-source charge		-	3.6	-	nC
$Q_{GD}$	gate-drain charge		-	7.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A$ ; $V_{DS} = 12 V$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	2.2	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12 V$ ; $V_{GS} = 0 V$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	4308	-	pF
		$V_{DS} = 0 V$ ; $V_{GS} = 0 V$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$	-	4830	-	pF
$C_{oss}$	output capacitance	$V_{DS} = 12 V$ ; $V_{GS} = 0 V$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	1137	-	pF
$C_{rSS}$	reverse transfer capacitance		-	439	-	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.48\ \Omega; V_{GS} = 4.5\text{ V};$	-	41	-	ns
$t_r$	rise time	$R_{G(ext)} = 4.7\ \Omega$	-	52	-	ns
$t_{d(off)}$	turn-off delay time		-	67	-	ns
$t_f$	fall time		-	30	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	47	-	ns
$Q_r$	recovered charge	$V_{DS} = 25\text{ V}$	-	22	-	nC

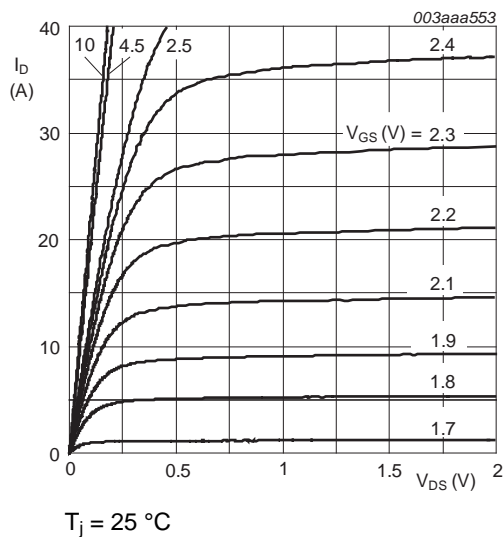


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

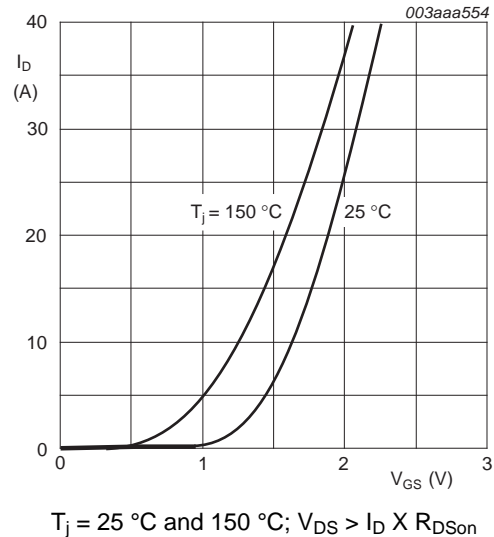
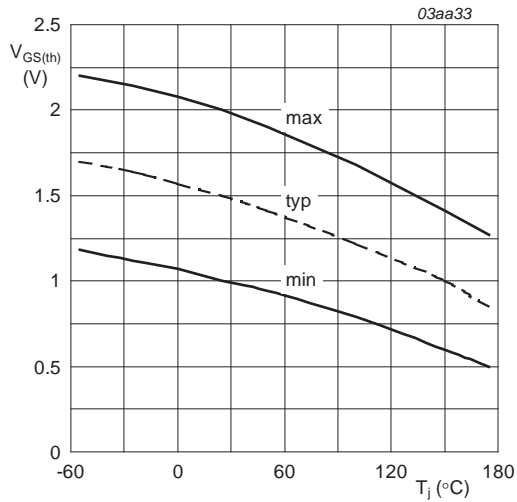


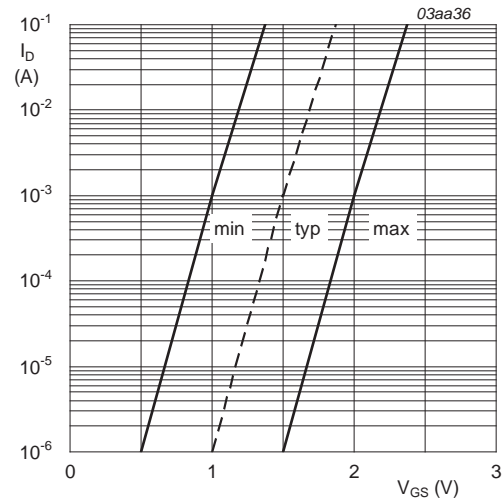
Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values





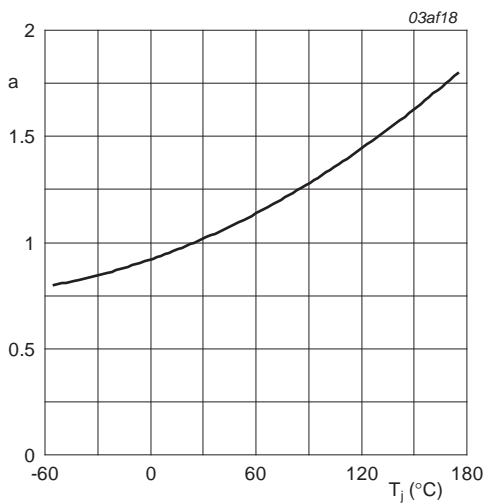
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

Fig 7. Gate-source threshold voltage as a function of junction temperature



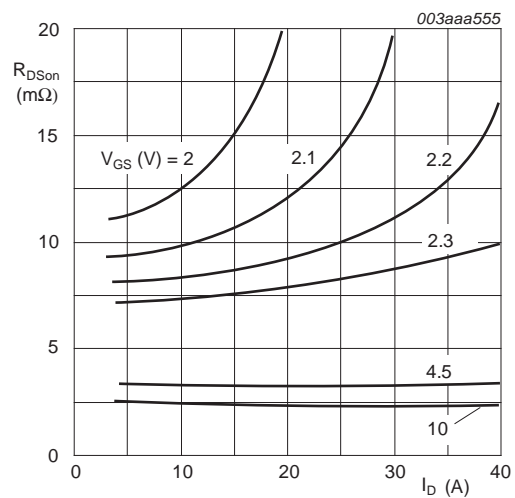
$$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$$T_j = 25\text{ °C}$$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

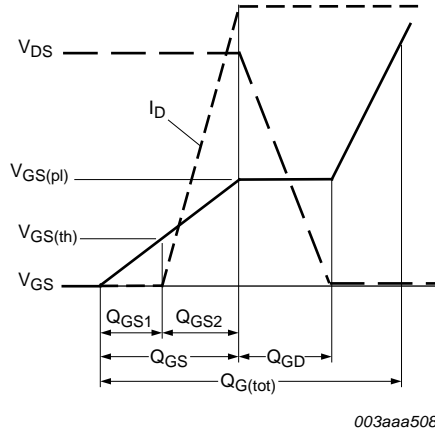
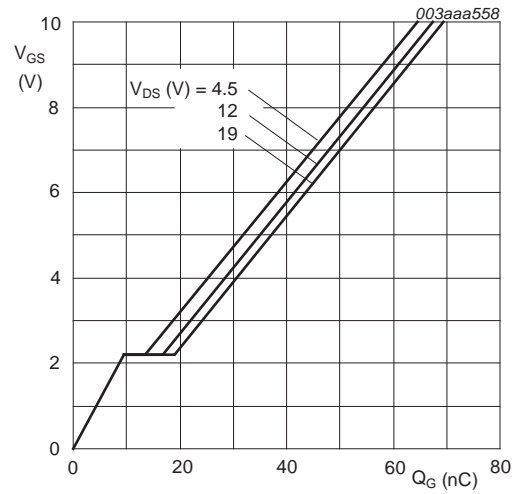
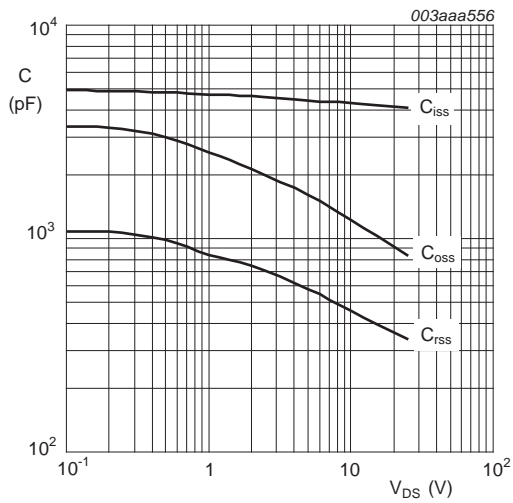


Fig 11. Gate charge waveform definitions



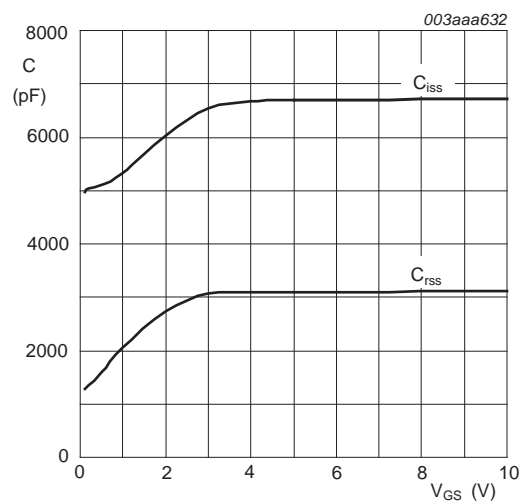
$I_D = 25\text{ A}$ ;  $V_{DS} = 4.5\text{ V}$ ,  $12\text{ V}$  and  $19\text{ V}$

Fig 12. Gate-source voltage as a function of gate charge; typical values



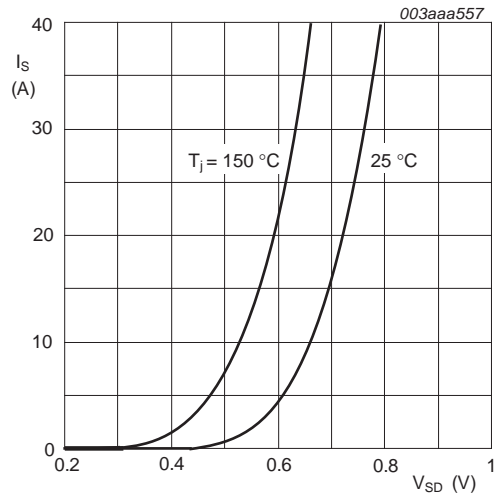
$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

Fig 14. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



$T_j = 25\text{ °C}$  and  $150\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

7. Package outline

Plastic single-ended surface-mounted package (LPAK; Power-SO8); 4 leads

SOT669

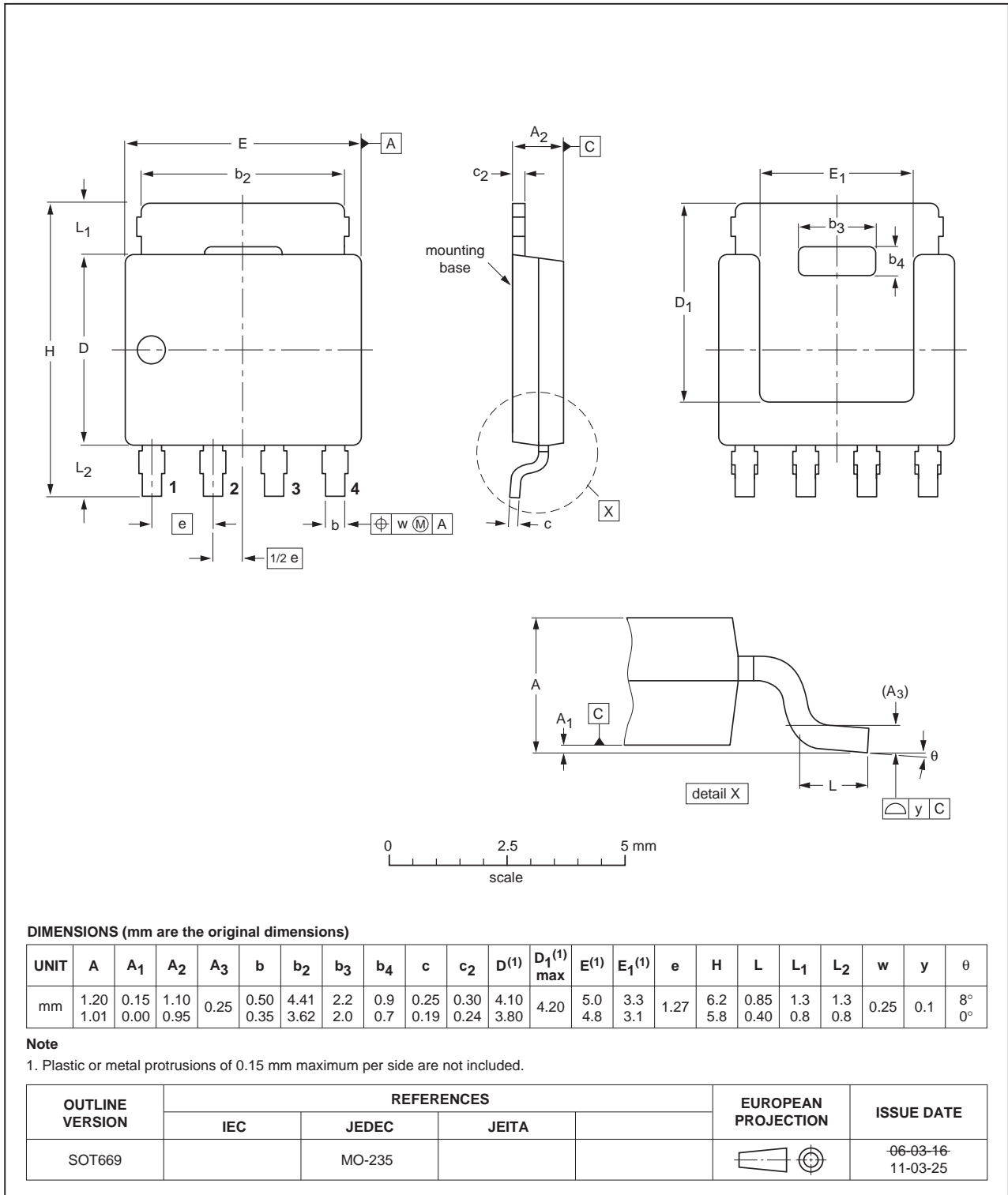


Fig 16. Package outline SOT669 (LPAK; Power-SO8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH2625L v.3	20111221	Product data sheet	-	PH2625L_2
Modifications:				
				<ul style="list-style-type: none"><li>• Status changed from preliminary to product.</li><li>• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>
PH2625L_2 (9397 750 12306)	20050224	Preliminary data sheet	-	PH2625L-01

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 10. Contact information

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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